Multi-sensor Read-out Circuit with Temperature, Capacitance and Voltage Sensing Functionalities

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Multi-sensor Read-out Circuit with Temperature, Capacitance and Voltage Sensing Functionalities

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Introduction

This thesis describes the design of a multi-sensor read-out circuit which combines temperature, capacitance and voltage sensing functionalities. The goal of this work is to design a read-out circuit which can be used in combination with capacitive and voltage mode transducers. In addition, the read-out circuit is facilitated with a temperature measuring. This is based on measuring the temperature-dependent base-emitter voltage of substrate PNPs (BJTs), and can be used to cancel the cross-sensitivity to temperature. The read-out circuit is sharing the same hardware for all the 3 modes, thus reducing area consumption.

The motivation of this work is described in this chapter, followed by an overview of prior art. At the end of this chapter, the organization of the thesis is given.

1.1 Motivation

Sensors are widely used in our daily life. Among them, capacitive sensors are important which can be used to sense pressure [1], humidity [2], and proximity [3], etc. These sensors digitize the variation of a capacitive transducer by the help of an analog-to-digital converter (ADC). This variation then translates to the physical properties (i.e., pressure or humidity).

However, many capacitive sensors also have obvious cross sensitivity to temperature, which means that temperature variation will also introduce capacitance change, causing errors in real measurement. To compensate for this cross-sensitivity, usually another temperature sensor is used to measure the ambient temperature simultaneously. Instead of using two separate sensor read-out circuits, one read-out circuit combining temperature and capacitance sensing functionalities will have an advantage in chip area and it is a better choice if there is no obvious disturbance between these functionalities.
Moreover, the reference voltage generators are usually ignored in most ADC publications, but the reference voltage design is critical for the ADC performance. A temperature-independent reference voltage benefits the ADC in terms of accuracy and PSRR. Therefore, an energy-efficient ADC with built-in reference voltage is required.

Since there is already an ADC digitizing the capacitance and temperature, it also benefits from the temperature functionality. The base-emitter voltage of substrate PNPs can be used to build the reference voltage and the accurate temperature measurement can compensate for the temperature dependency of the reference voltage (described in chapter 4). So this circuit can also sense an input voltage without an accurate external reference voltage and no additional circuit is needed to generate the reference voltage because the substrate-PNP circuit is re-used.

This design needs to have the following properties:

- Accurate temperature measurement
- High resolution capacitance measurement
- Accurate built-in reference voltage for voltage measurement

1.2 Background overview

Nowadays, capacitance-to-digital converter (CDC) can be implemented in different kinds of ways to meet different requirements. The design in reference [2] uses a 3rd order ΔΣ modulator which employs current-efficient OTA based on current-starved cascoded inverters and it achieves 12.5-bit resolution in 0.8ms conversion time. Reference [4] presents a CDC based on incorporating a capacitive sensor and a capacitor array into successive approximation register (SAR) technique which achieves 6.8-bit resolution in 3.8µs conversion time. In some more recent designs, Reference [5] describes a design combining 9b asynchronous SAR logic and incremental ΔΣ modulator to reach 15.4-bit resolution in 230µs conversion time. Iterative delay-chain discharge technique is used to achieve a relatively large input capacitance range and obtains 9.5-bit resolution in 19.06µs conversion time in reference [6]. Reference [7] proposes a wide-range CDC combining correlated-double-sampling approach with a differential asynchronous SAR ADC. This design achieves 14-bit resolution in 4ms conversion time.

The target for the CDC mode is high resolution with high energy efficiency. The CDC functionality is implemented by adding it to an existing temperature-to-digital converter (TDC) as mentioned before. The superior accuracy, resolution and power-supply sensitivity characteristics of the TDC also benefits the CDC functionality added to it [8]. The target specifications for the CDC design is listed in Table 1.1.
In respect of the ADC functionality, there are some designs with an on-chip reference voltage generator. Reference [9] describes a similar design by adding the ADC functionality to an existing TDC design with the help of a pre-scaler. A dynamic voltage reference with temperature drift of less than 1.7ppm/°C is obtained. Reference [10] presents a SAR ADC with duty-cycled reference generation which achieves 108ppm/°C reference temperature drift, 10-bit resolution and 80kS/s sample rate.

For ADC mode of this design, the main target is a built-in reference with low temperature coefficient and at the same time, high resolution and good power efficiency should be achieved. Table 1.2 shows the specifications for ADC mode.

**Table 1.2 Target specifications for ADC mode**

<table>
<thead>
<tr>
<th>ADC mode</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>1.6-2.0V</td>
</tr>
<tr>
<td>Supply current</td>
<td>4.6µA</td>
</tr>
<tr>
<td>Area</td>
<td>&lt;0.2mm²</td>
</tr>
<tr>
<td>Temperature range</td>
<td>-70~125°C</td>
</tr>
<tr>
<td>Input range</td>
<td>0~V&lt;sub&gt;dd&lt;/sub&gt;</td>
</tr>
<tr>
<td>Resolution</td>
<td>100µV</td>
</tr>
<tr>
<td>Temperature drift</td>
<td>2ppm/°C</td>
</tr>
</tbody>
</table>

1.3 Thesis organization

Chapter 2 explains the principle of digitizing the temperature based on substrate PNPs. The detailed design techniques of the existing TDC, including the temperature sensing front-end and ΔΣ modulator are presented.

Chapter 3 explores the principle of digitizing the capacitance. The way of adding CDC functionality to the existing TDC design is shown and the design techniques used in CDC mode are also discussed.

Chapter 4 describes a new zoom-in scheme for digitizing the input voltage with negligible additional hardware resources and time consumption. The detailed ADC mode circuit is shown.
Chapter 5 demonstrates the block diagram including the core circuit and all peripheral circuits. The complete circuit diagram combining TDC, CDC and ADC modes is given as well. The noise analysis for the three modes follows. The layout of the circuit is shown and the post-layout simulation results for each mode are given respectively.

Finally, chapter 6 summarizes the contributions of the thesis. The future plan for the measurements and the improvements of the design is given.
Integrated TDCs are currently used for temperature measurement and compensation in many SoC situations. TDCs are built based on temperature dependency of thermistors [11], MOS transistors [12] and bipolar junction transistors (BJTs) [13]. BJT-based TDCs attract more attention due to its high accuracy and compatibility with modern CMOS technology (substrate PNPs).

The starting point of this thesis is an accurate BJT-based CMOS TDC [8], which achieves an inaccuracy of 60mK (±3σ) from -70°C to 125°C. Moreover, it has high energy efficiency (i.e., 7.3pJ°C² resolution FoM) and good power-supply sensitivity (i.e., 0.01°C/V).

2.1 Temperature-sensing front-end

2.1.1 Principle of operation

The base-emitter voltage of a bipolar transistor can be written as

\[ V_{BE} = \frac{kT}{q} \ln \left( \frac{I_C}{I_S} \right) \]  

(2.1)

where \( k \) is Boltzmann’s constant, \( T \) is the absolute temperature, \( q \) is the charge of an electron, \( I_C \) is the current flowing into the collector of the bipolar transistor and \( I_S \) is the saturation current of the transistor. This voltage is complementary to absolute temperature (CTAT) and the temperature coefficient is about -2mV/K with a small curvature according to experiments [17].

Two voltages are needed to feed into an ADC for digitization purposes. One way to do so is to digitize a proportional to absolute temperature (PTAT) voltage with respect to a
nominally constant reference voltage \([14]\). So usually two bipolar transistors biased by different currents are used to generate two base-emitter voltages as

\[
V_{BE1} = \frac{kT}{q} \ln\left(\frac{I_c}{I_S}\right)
\]  
(2.2)

\[
V_{BE2} = \frac{kT}{q} \ln\left(\frac{pI_c}{I_S}\right)
\]  
(2.3)

Their difference can be derived as

\[
\Delta V_{BE} = V_{BE2} - V_{BE1} = \frac{kT}{q} \ln(p)
\]  
(2.4)

where \(p\) is the ratio of two collector currents (chosen to be 5 in the design). So \(\Delta V_{BE}\) is a PTAT voltage.

Figure 2.1 illustrates the basic principle of the temperature-sensing front-end. The PTAT voltage \(\Delta V_{BE}\) is quite small which needs to be amplified and then linearly combined with CTAT voltage \(V_{BE1}\), resulting in a temperature independent reference voltage as follows

\[
V_{REF} = V_{BE1} + \alpha \Delta V_{BE}
\]  
(2.5)

where \(\alpha\) is the amplification factor. An ADC is connected to the temperature-sensing front-end to digitize the ratio between \(\alpha \Delta V_{BE}\) (PTAT) and reference voltage \(V_{REF}\). The digital reading then has a linear relationship with temperature and can be expressed as
2.1 Temperature-sensing front-end

\[ \mu = \frac{\alpha \Delta V_{BE}}{V_{BE1} + \alpha \Delta V_{BE}} \]  \hspace{1cm} (2.6)

Due to the linear relationship, a digital output of temperature in degrees Celsius can be obtained by scaling the linear function as

\[ D_{out} = A\mu - B \]  \hspace{1cm} (2.7)

where \( A \) and \( B \) are scaling coefficients: \( A \approx 600 \) and \( B \approx 273 \) [14].

Alternatively, as in [13], the ADC may digitize \( X = V_{BE}/\Delta V_{BE} \), which is enough to calculate \( \mu \) in the same manner by noting that \( \mu = \alpha/(\alpha + X) \). This way avoids the reference voltage generation circuit.

![Figure 2.2 Principle of ratiometric measurement between \( V_{BE} \) and \( \Delta V_{BE} \): (a) ratio \( X \) between \( V_{BE} \) and \( \Delta V_{BE} \); (b) linearized function of \( \mu \) constructed from ratio \( X \)](image)

Figure 2.2 Principle of ratiometric measurement between \( V_{BE} \) and \( \Delta V_{BE} \): (a) ratio \( X \) between \( V_{BE} \) and \( \Delta V_{BE} \); (b) linearized function of \( \mu \) constructed from ratio \( X \)

Figure 2.2 illustrates principle of the ratiometric measurement in which the ratio \( X = V_{BE}/\Delta V_{BE} \) is measured. As shown in Figure 2.2(a), this ratio is a monotonic but non-linear function of temperature instead of a linear function. It varies from 29 to 6 in the temperature range from -70\(^\circ\)C to 125\(^\circ\)C. The PTAT ratio \( \mu \) can be constructed from ratio \( X \) as

\[ \mu = \frac{\alpha \Delta V_{BE}}{V_{BE1} + \alpha \Delta V_{BE}} = \frac{\alpha}{X + \alpha} \]  \hspace{1cm} (2.8)

As a result, the \( \alpha \) is now a calibration parameter, which is arbitrarily chosen in the digital backend. The resulting \( \mu \) then translates to degrees Celsius as in equation (2.7).
2.1.2 Temperature-sensing front-end design

Figure 2.3 shows the simplified circuit implementation of the temperature-sensing front-end. The bipolar core consists of two substrate PNPs biased by two different currents $I_{bias}$ (160nA) and $5I_{bias}$.

The pre-bias circuit in Figure 2.3 uses an amplifier to force the difference between $V_{BE}$ of QLB and QRB, which are biased at different current densities, over a resistor $R_b$. It then generates a bias current as follows:

$$ I_{bias} = \frac{\Delta V_{BE,bias}}{R_b} = \frac{kT}{qR_b} \ln(m) \quad (2.9) $$

where $m$ is the ratio between the two bias currents in the pre-bias circuit (chosen to be 5 as well). This current is then copied to the bipolar core, to bias the sensing PNPs $Q_L$ and $Q_R$. As a result, the bias current is independent of supply variation and robust over process and voltage variations.

The opamp in the pre-bias circuit uses a folded-cascode structure with open-loop gain of 82dB over the process variations. Therefore, it minimizes the errors associated with the limited loop-gain. A set of choppers is also used to minimize the offset of the opamp [16].

Biased by this current, the base-emitter voltage of the bipolar transistors in the bipolar core can be written regardless of non-idealities as

$$ V_{BE,ideal} = \frac{kT}{q} \ln \left( \frac{\Delta V_{BE,bias}}{R_bI_S} \right) = \frac{kT}{q} \ln \left( \frac{kT \ln(m)}{qR_bI_S} \right) \quad (2.10) $$
Additionally, this PTAT bias current also reduces the curvature of $V_{BE}$ [17], which will benefit the accuracy of temperature measurement.

Figure 2.4 shows the detailed circuit implementation of the temperature-sensing front-end. The techniques used in the circuit will be discussed respectively.

**Symmetrical layout**

The PNPs in the bias circuit and the bipolar core are inter-digitated in the layout. The symmetrical layout mitigates the mismatch between the PNPs. As a result, the dominant sources of inaccuracy are then the spread in the PNPs' saturation current $I_s$ and in the nominal value of $R_b$ which can be corrected by a single PTAT trim [8].

**Dynamic error cancellation**

The ratio of the bias currents in the pre-bias circuit and in the bipolar core should be well-defined, which means the unit current in the current mirror should match each other well. Otherwise, mismatch between the unit current will directly translate to the error of $\Delta V_{BE}$. It is an non-PTAT error which cannot be corrected by a single PTAT trim [14]. According to [15], the current ratio has to be accurate to $\pm 0.011\%$ to limit the temperature error within $\pm 0.01^\circ C$. Precise layout alone cannot meet this accuracy requirement. So a dynamic element matching (DEM) scheme is used to average out mismatches.

Two banks of six unit currents are used to bias the pre-bias circuit and the bipolar core, and each current can go to one of the two PNPs. The DEM scheme is that one unit current goes to $Q_L$ ($Q_{LB}$) with the others going to $Q_R$ ($Q_{RB}$), and during the clock cycles of the following $\Delta \Sigma$ modulator (shown in Section 2.2), the current going to $Q_L$ ($Q_{LB}$) is alternated sequentially. The required averaging is performed by the integrator of the $\Delta \Sigma$ modulator [18].
Figure 2.5 illustrates the monte-carlo simulation results of the proposed DEM scheme, assuming there is 0.5% mismatch between the current sources. Black dash lines indicate the ±0.011% limit for ±0.01°C inaccuracy. It is obvious that after 80 clock cycles of DEM, the relative inaccuracy of the current sources is reduced within the range expected, which represents 3.2ms conversion time in this design.

Furthermore, the two current mirror banks are swapped periodically to make sure that $I_{bias}$ in the pre-bias circuit is accurately copied to the bipolar core, which additionally reduces the mismatch between current mirrors.

**$\beta_F$-compensating scheme**

The substrate PNPs are biased via their emitter current with the collector connected to ground because the technology is single-well, the PNPs are intrinsically grounded at the collector side. The transistor’s forward current-gain $\beta_F$ affects its collector current, so equation (2.1) can be re-written as

$$V_{BE} = \frac{kT}{q} \ln \left( \frac{I_C}{I_S} \right) = \frac{kT}{q} \ln \left( \frac{I_{bias}}{I_S} \frac{\beta_F}{\beta_F + 1} \right)$$

(2.11)

If $\beta_F$ is high (e.g. >100), the resulting effect on $V_{BE}$ is reproducible. However, in advanced technology nodes its value is as low as 5, and highly process dependent. Figure 2.6 shows its change over the bias current variation.
Figure 2.6 The forward current-gain of substrate PNPs as a function of emitter current in 0.16µm CMOS process

Then $\Delta V_{BE}$ generated by the bipolar core can be written as

$$
\Delta V_{BE} = \frac{kT}{q} \ln(p \times \frac{\beta_F(5I)}{\beta_F(5I) + 1} \times \frac{\beta_F(I) + 1}{\beta_F(I)})
$$

(2.12)

As a result, the error caused in $\Delta V_{BE}$ is now process spread and temperature dependent, which makes $\Delta V_{BE}$ less reproducible and causes errors in temperature measurement.

To mitigate the effect of the forward current-gain spread, the bias current is chosen in the flattest region of $\beta_F$ curve (160nA). This method mitigates the error in $\Delta V_{BE}$ caused by the variation of $\beta_F$. Moreover, a resistor with nominal value of $R_b = R_b/5$ is added in series with the base of one bipolar transistor in the bias circuit (see Figure 2.4). So the following equation can be derived assuming that the opamp has infinite gain.

$$
R_b \times I_{bias} - \frac{R_b}{5} \times \frac{5I_{bias}}{\beta_F + 1} = \Delta V_{BE, bias}
$$

(2.13)

So a $\beta_F$-dependent bias current is generated as

$$
I_{bias} = \frac{\beta_F + 1\Delta V_{BE,bias}}{\beta_F R_b}
$$

(2.14)

Substituting this current in equation (2.11), the $\beta_F$-dependent term in $V_{BE}$ is cancelled (assuming ideal matching), so the generated $V_{BE}$ is now independent of the forward current-gain.
Moreover, a switch $S_{\beta}$ (see Figure 2.4) is used to turn on and off the $\beta_F$-compensation scheme. And a resistor $R$ biased by $I_{bias}$ is used. When the $\beta_F$-compensation scheme is on, the voltage across the resistor is

$$V_{\beta, on} = \frac{\beta_F + 1}{\beta_F} \frac{\Delta V_{BE,bias}}{R_b} R \tag{2.15}$$

When the $\beta_F$-compensation scheme is off, the voltage across the resistor is

$$V_{\beta, off} = \frac{\Delta V_{BE,bias}}{R_b} R \tag{2.16}$$

The ratio between the two voltages is an indication of the value of $\beta_F$.

### 2.2 Incremental zoom ADC

In order to build a temperature-to-digital converter, an ADC is needed to digitize the ratio $X = \frac{V_{BE}}{\Delta V_{BE}}$. In this design, the ADC is a 2nd order zoom-ADC which is a 2-step SAR, $\Delta\Sigma$ ADC. In the first coarse step, the ADC is configured to a 5-bit SAR ADC and in the second fine step, the ADC is configured to a 2nd order $\Delta\Sigma$ ADC.

#### 2.2.1 ADC architecture

![Diagram showing temperature dependency of $X = n + \mu'$ from -70°C to 125°C with integer $n$ ranging from 6 to 29 while fraction $\mu'$ ranging from 0 to 1.]

Figure 2.7 Temperature dependency of $X = n + \mu'$ from -70°C to 125°C with integer $n$ ranging from 6 to 29 while fraction $\mu'$ ranging from 0 to 1.
2.2 Incremental zoom ADC

Figure 2.7 shows the principle of how the ‘zoom’ works. The ratio \( X = \frac{V_{BE}}{\Delta V_{BE}} \) is divided into integer part \( n \) and fractional part \( \mu' \). \( n \) is determined by five steps of SAR, using a binary search. Once the integer \( n \) is determined, the references of the ADC are chosen as \( n \) and \( (n + 1) \). In this narrower range, the fractional part \( \mu' \) is measured with high resolution.

\[
X = \frac{V_{BE}}{\Delta V_{BE}}
\]

\( \mu' \) is divided into integer part \( n \) and fractional part \( \mu' \).

Once the integer \( n \) is determined, the references of the ADC are chosen as \( n \) and \( (n + 1) \). In this narrower range, the fractional part \( \mu' \) is measured with high resolution.

(a) 

Figure 2.8 Architecture of zoom ADC during (a) the coarse step and (b) the fine step

Figure 2.8 illustrates the architecture of the zoom ADC in two steps. During the coarse step, a clocked comparator compares \( V_{BE} \) and \( k \cdot \Delta V_{BE} \) where \( k \) is an integer number from 1 to 31 realized by a capacitive ratio. A five-step successive approximation then finds \( n \). In the following fine step, the ADC is configured to a 2nd-order \( \Delta \Sigma \) ADC with two references set to \( n \cdot \Delta V_{BE} \) and \( (n + 1) \cdot \Delta V_{BE} \). The fractional part of ratio \( X \) is measured by the \( \Delta \Sigma \) conversion with high resolution.

In practice, the reference range is chosen to be \( (n - 1) \cdot \Delta V_{BE} \) and \( (n + 1) \cdot \Delta V_{BE} \) instead of \( n \cdot \Delta V_{BE} \) and \( (n + 1) \cdot \Delta V_{BE} \). Because if ratio \( X \) is near integer \( n \), the input of the \( \Delta \Sigma \) ADC is almost zero which leads to poor signal-to-noise ratio (SNR) performance while if ratio \( X \) is near integer \( (n + 1) \), the input is full range and the ADC is overloaded which also leads to poor SNR performance. Doubling the input range makes sure that the input is roughly in the middle of the range. And it also avoids wrong decision in the coarse step when there is an error in the gain factor \( k \).

An additional guard-band step is used in the coarse step to guarantee that the input lies in the middle of the range. In the guard-band step, \( V_{BE} \) is compared to \( (n + 0.5) \cdot \Delta V_{BE} \), and the references are then set to \( (n - 1) \cdot \Delta V_{BE} \) and \( (n + 1) \cdot \Delta V_{BE} \) depending on the result. This step makes sure that the input signal can only vary from \( 1/4 \) to \( 3/4 \) of the reference range.

The advantage of such kind of ‘zoom’ is that higher resolution is obtained in the same conversion time compared with normal \( \Delta \Sigma \) ADC.
Figure 2.9 Architecture of the proposed ΔΣ ADC during the fine step

Figure 2.9 shows the architecture of the ΔΣ ADC during the fine step. A 2\textsuperscript{nd}-order feedforward with one bit comparator architecture is chosen for a shorter conversion time to achieve the same resolution compared with 1\textsuperscript{st} order ΔΣ ADC. Moreover, the over-all loop gain is achieved by two integrators so the requirement for each OTA is relaxed, leading to a more energy-efficient design.

2.2.2 Switched-capacitor circuitry implementation

The integrator of the ΔΣ ADC is realized by the switched-capacitor (SC) circuit as shown in Figure 2.10 (single-ended as an example).

Figure 2.10 Switched-capacitor circuitry of TDC

If the bitstream (bs) of the ΔΣ modulator is 1, Δ\(V_{BE}\) is sampled on \((n + 1)C_s\) as a reference while if the bitstream is 0, Δ\(V_{BE}\) is sampled on \((n - 1)C_s\) as a reference. In the first clock phase \(\varphi_1\), the input voltage \(V_{BE}\) is sampled on a capacitor \(C_s\) (120fF) and is thus converted to a charge of \(C_sV_{BE}\). The reference node is grounded in \(\varphi_1\). In the second clock phase \(\varphi_2\), due to sharp potential drop of the input node from \(V_{BE}\) to 0, a charge of \(C_sV_{BE}\) is needed to bring the virtual ground node of the OTA back to 0 potential. This charge is supplied by the integration capacitor \(C_{int}\) and the capacitors sampling Δ\(V_{BE}\).
The latter one can supply a charge of \((n \pm 1)C_s\Delta V_{BE}\), so the charge supplied by \(C_{int}\) is 
\[C_s[V_{BE} - (n \pm 1)\Delta V_{BE}]\], which leads to a potential change of the OTA’s output node from 
0 to \(C_s[V_{BE} - (n \pm 1)\Delta V_{BE}]/C_{int}\). The integrator coefficient is defined by the ratio of the 
sampling and integration capacitor which is 0.5 in this design:

\[
\alpha_{SC} = \frac{C_s}{C_{int}} \tag{2.17}
\]

This integration scheme can sample and integrate \(V_{BE}\) and \((n \pm 1)\Delta V_{BE}\) simultaneously
in one clock cycle instead of using two clock cycles sampling \(V_{BE}\) and \(- (n \pm 1)\Delta V_{BE}\)
respectively, which halves the conversion time.

Moreover, clock phases \(\phi_1\) and \(\phi_2\) should be non-overlapping clocks to avoid the case
that switches are all closed at the same moment, as shown in Figure 2.11.

![Figure 2.11 Non-overlapping clocks](image)

In the real design, a fully differential architecture is implemented to mitigate even order
harmonics and improve SNR. The detailed integration scheme is shown in Figure 2.12.

![Figure 2.12 (a) Integration scheme for the fully differential architecture; (b) Waveform of one clock cycle](image)

The voltage \(k \cdot \Delta V_{BE}\) (\(k\) is determined in the coarse step and set to be \((n - 1)\) or \((n + 1)\)
based on the bitstream) is realized by using multiple unit capacitors \(C_s\) in parallel.
sampling $\Delta V_{BE}$ simultaneously. $V_{BE}$ and $k \cdot \Delta V_{BE}$ are sampled with opposite polarity to realize the subtraction. The polarities of both input voltages are swapped during $\varphi_2$, and thus the output voltage of the OTA is proportional to $(V_{BE} - k \cdot \Delta V_{BE})$ which is small due to the subtraction, leading to a relaxed requirement for the output swing of the OTA design, as shown in Figure 2.12.

Figure 2.13: Simplified circuit diagram of proposed incremental zoom ADC

Figure 2.13 shows the simplified circuit diagram of the incremental zoom ADC. Because the ratio $X = V_{BE} / \Delta V_{BE}$ reaches 29 at -70°C, 30 capacitors are used in the capacitor DAC to sample $\Delta V_{BE}$ with one extra capacitor sampling $V_{BE}$ and one for safe, so there are 32 capacitors in the DAC in total. The capacitors which are not used in the DAC are connected to $V_{BE,d}$ generated by a dummy BJT to avoid floating capacitors. For each capacitor in the DAC, there are three switches connecting it to one of the three voltages: $V_{BE}$, $\Delta V_{BE}$ and $V_{BE,d}$ (not shown in the figure).

There are delayed versions of clock phases $\varphi_{1d}$ and $\varphi_{2d}$, which have about 20ns delay after $\varphi_1$ and $\varphi_2$ fall to 0 respectively. So the switches controlled by delayed clocks open later and thus these switches cannot inject charge into the integration capacitors [22], which leads to better accuracy performance.

A ‘SAR/SD’ signal is used to bypass the second integrator in the coarse step, where $V_{BE}$ is compared to $k \cdot \Delta V_{BE}$ and the integration capacitor $C_{int}$ is reset after every comparison. Once the value of $k$ is determined, the ADC is configured to a 2nd order ΔΣ ADC and the bitstream is sent off-chip. The temperature is obtained after filtering, calibration (thermal calibration or voltage calibration) and polynomial fit [13], which are not discussed here.

Mismatch between the sampling capacitors $C_{s1} \cdots C_{s32}$ will cause errors to the capacitive ratios $(n \pm 1)$, making them less reproducible. In order to mitigate this kind of errors, DEM is applied by alternating the capacitors used in successive cycles of the ΔΣ modulator and mismatches are then averaged out.
In order to remove the OTA offset and 1/f noise, system-level chopping and correlated double sampling (CDS) are used. The input chopper swaps the input polarities in two successive ΔΣ conversions and the output chopper is realized in the digital backend. The system offset is then removed by averaging the two digital outputs.

### 2.2.3 Design of the OTA and the comparator

Due to the charge cancellation between $V_{BE}$ and $-k \cdot \Delta V_{BE}$ and feedforward topology of the ADC, the differential output voltage of the OTAs is small (~60mVpp), relaxing the requirements for the OTA design. So a more power-efficient OTA architecture can be chosen.

![Figure 2.14 Three kinds of OTA structures](image)

Figure 2.14 shows three kinds of OTA choices. Folded-cascode and telescopic OTAs are commonly used because of their reasonable output swing and high DC gain. However, since the output swing requirement in this design is relaxed, the OTA with higher energy-efficiency is preferred.

The input transistors of the inverter-based OTA share the same bias current so the overall $g_m$ is doubled compared with conventional folded-cascode and telescopic OTAs, which doubles the energy-efficiency. So the inverter-based OTA is chosen in this design.

![Figure 2.15 Current reuse OTA structure](image)
Figure 2.15 illustrates the inverter-based cascode OTA used in this design. Cascode transistors increase the DC gain of the OTA. Switched-capacitor common-mode feedback circuitry is used to force the output at common-mode potential.

The OTA of the first integrator achieves about 100dB DC gain, 2.1MHz GBW and 86° phase margin, with only 480nA current consumption. While the second OTA is a ¼ scaled version of the first one since errors introduced by the second integrator are attenuated by the gain of the first one. The second OTA consumes 120nA current in total.

Figure 2.16 Circuit diagram of the comparator (a) Pre-amplifier; (b) Dynamic latch

The comparator is implemented as a dynamic latch preceded by a pre-amplifier which also prevents the kickback to the output of the second integrator [14], as shown in Figure 2.16. The pre-amplifier is made with a three cascaded amplifiers. Each of these amplifiers has a gain defined by the ratio of a PMOS load to a PMOS input device. The pre-amplifier has a gain of 27 and consumes 170nA at room temperature.
Capacitance-to-digital converter
based on switched-capacitor circuitry

A CDC converts the capacitance of a capacitive sensing element into digital value. The digital value then translates to real world properties. A capacitive sensor system usually consists of a capacitive sensing element, a sensor interface and the digital backend, as shown in Figure 3.1 [19].

![Figure 3.1 Diagram of a capacitive sensor system](image)

The basis of a capacitive sensing element is a parallel-plate capacitor with area $A$ and plate distance $d$. Its capacitance can be expressed as ($d$ is much smaller than $A$ so that the effect of the non-uniform electric field at the edges can be ignored)

$$C = \varepsilon \frac{A}{d}$$  \hspace{1cm} (3.1)

where $\varepsilon$ is the dielectric constant of the material between the two electrodes. A capacitive sensing element can be obtained by modulating one of the three parameters [19]. By modulating the dielectric constant $\varepsilon$, humidity sensors, gas sensors, DNA sensors, etc. can be realized. By modulating the area $A$, angular detectors and displacement sensors can be obtained. In pressure sensors, the distance $d$ is modulated. If the measurand to capacitance modulation is a known function (e.g., by a calibration step), the CDC’s output can then translate to the measurand.
Figure 3.2 Capacitance change as a function of pressure change

Figure 3.2 illustrates the example of a pressure sensor [1]. The capacitance of the sensing element has a monotonic relationship with the pressure and it has a large baseline capacitance (0.95 pF in the example). In most cases, the capacitance variation is small compared to the baseline capacitance. This large capacitance contains no information but limits the input range and increases energy consumption of the CDC.

3.1 Capacitance-sensing interface

Because of the slow variation of capacitance in pressure sensor application, the incremental zoom ADC presented in the previous chapter is reused to sense the capacitance. The CDC then benefits from the high energy efficiency and resolution, while its large baseline capacitance is cancelled by the zoom principle.

(a)                                                                                   (b)

Figure 3.3 Architecture of the zoom CDC during (a) the coarse step and (b) the fine step
3.1 Capacitance-sensing interface

Figure 3.3 shows the zoom principle of the CDC in capacitance domain. During the coarse step, successive approximation logic is used to find the integer part \( n \) of the ratio \( X_c = C_{\text{sensor}} / C_s \) (where \( C_s \) is the unit capacitor). If \( kC_s > C_{\text{baseline}} \), this method also cancels the baseline capacitance. The two references for the following fine step are set to \( (n - 1)C_s \) and \( (n + 1)C_s \) respectively based on the bitstream. As in TDC mode, the fine step is a 2\textsuperscript{nd}-order \( \Delta \Sigma \) conversion which can measure the fractional part of the ratio \( X_c \) with high resolution. Similarly, a guard-band step is used to make sure that the input capacitance is in the middle of the reference capacitance range (i.e., \((n - 1)C_s \) and \((n + 1)C_s \)).

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{fig3.4.pdf}
\caption{Switched-capacitor circuitry of CDC}
\end{figure}

Switched-capacitor circuitry is also used here to implement the zoom CDC as shown in Figure 3.4 (single-ended circuit as an example). The capacitive sensing element \( C_{\text{sensor}} \) as well as the reference capacitors are charged by the supply voltage \( V_{dd} \). The reference capacitor is realized by using \((n \pm 1)\) unit capacitors in parallel. The charge proportional to the sensing capacitance \( C_{\text{sensor}} \) is then balanced by the charge proportional to the reference capacitances \((n \pm 1)C_s\) during the successive cycles of the \( \Delta \Sigma \) conversion, which means the average integrated charge tends to zero (charge balancing principle).

The value of \( C_{\text{sensor}} \) can be calculated from the bitstream. Assuming that the length of the bitstream is \( N \), the average value of the bitstream is \( x \).

Due to the charge balancing principle of the \( \Delta \Sigma \) modulator, the capacitance is calculated as

\[
xNV_{dd}[C_{\text{sensor}} - (n + 1)C_s] + (1 - x)NV_{dd}[C_{\text{sensor}} - (n - 1)C_s] = 0
\]

\[
x[C_{\text{sensor}} - (n + 1)C_s] + (1 - x)[C_{\text{sensor}} - (n - 1)C_s] = 0
\]

So the capacitance of the capacitive sensing element is
\[ C_{sensor} = (n - 1)C_s + 2xC_s \]  

(3.4)

The first part \((n - 1)C_s\) can be seen as the baseline capacitance, which is determined in the coarse step. The second part \(2xC_s\) is the high resolution part, which is determined in the fine step.

In the real design, a fully-differential circuitry is used as shown in Figure 3.5.

![Figure 3.5 Integration scheme of a fully-differential CDC in clock phase (a) \(\phi_1\); (b) \(\phi_2\)](image)

Due to the fully differential architecture, two sensing capacitors are needed. The polarity of the input supply voltage is swapped during \(\phi_2\) and the output voltage of the OTA is proportional to \((C_{sensor} - kC_s)\). If there is a mismatch between the two sensing capacitors, the output voltage is then proportional to \((C_{sensor,p} + C_{sensor,n} - 2kC_s)\) which is equivalent to measuring an average capacitance of \((C_{sensor,p} + C_{sensor,n})/2\). If the monotonic relationships between capacitance and measurand of the two sensing capacitors are well known, the value of measurand can still be obtained from the measured average capacitance. Moreover, since the average capacitance is measured, in practice it can also measure the capacitance of one capacitive sensor by connecting a constant capacitor which nominally equals to \(C_{sensor}\) instead of using two equal capacitive sensors.
3.2 Transistor-level circuit design

Two on-chip test capacitors (~2pF) are used for the test purposes of the read-out circuit. This helps to test the read-out circuit without any sensing capacitors, and also brings the test capacitors with minimum parasitics. There are also pins for the off-chip external capacitors and a signal 'ext' is used to choose between the internal capacitors and the external capacitors.

A 'mode' signal is used to switch between TDC mode and CDC mode. When 'mode' is high, the circuit is configured in TDC mode as shown in Figure 2.13 with the two sensing capacitors disconnected from the virtual ground node of the OTA and grounded. When 'mode' is low, the circuit is configured in CDC mode with the two sensing capacitors connected to the virtual ground node of the OTA. The voltage $V_{BE}$ feeding into the modulator is replaced by the supply voltage $V_{dd}$ to charge the sampling capacitors (switches are not shown in the figure).

The sampling capacitors $C_{b1} \cdots C_{b32}$ in the DAC are used to form the reference capacitance in CDC mode. There are 32 fring capacitors in the DAC, which can build a capacitance reference ranging from 0 to $120\text{fF} \times 32 = 3.84\text{pF}$. So in principle, up to 3.84pF capacitance can be measured. The unused capacitors in the DAC are connected to $V_{BE,d}$ generated by the dummy BJT similarly to TDC mode.
When the circuit is in TDC mode, the differential output voltage of the first OTA is
\[ 2(V_{BE} - k \cdot \Delta V_{BE})C_s/C_{int} \] whose maximum value is \( 2 \times 1.5 \times \Delta V_{BE}C_s/C_{int} \approx 60 \text{mV}_{pp} \) (when the ratio \( V_{BE}/\Delta V_{BE} \) is at the margin of the guard-band decision). When the circuit is in CDC mode, the output voltage of the first OTA is \[ 2V_{dd}(C_{sensor} - k C_s)/C_{int} \] whose maximum value is \( 2V_{dd} \times 1.5 \times C_s/C_{int} \approx 2.7 \text{V}_{pp} \) (when the ratio \( C_{sensor}/C_s \) is at the margin of the guard-band decision) which is outside of the OTA output swing range. In order to reduce the output voltage swing of the first OTA, an extra capacitor is added in parallel to the integration capacitor in CDC mode. In this design, the extra capacitance is chosen to be 2pF, leading to an output voltage of 290mV_{pp}.

System-level chopping is also used here by swapping the input polarities in two successive conversions and by averaging the two digital outputs, the offset is thus removed. Two separate choppers are added to the sensing capacitors instead of one shared chopper, to reduce routing distance in the symmetrical layout.

![Figure 3.7 CDC mode clock signals generation blocks](image)

Four separate clock signals ‘\( \varphi_{1,CDC1} \)’, ‘\( \varphi_{2,CDC1} \)’, ‘\( \varphi_{1,CDC2} \)’, ‘\( \varphi_{2,CDC2} \)’ are generated by digital blocks as shown in Figure 3.7. In CDC mode, ‘\( \varphi_{1,d} \)’ and ‘\( \varphi_{2,d} \)’ are chosen as clock signals so the integration scheme of CDC mode can operate (see Figure 3.5). In TDC mode, the system-level chopping signals are chosen to control these switches, grounding the input of the sensing capacitors. This method prevents the meaningless charging and discharging of the sensing capacitors in TDC mode and saves some power while only consuming a little additional digital resources.
The reference capacitance is built by the unit capacitors and the zoom step divides the total input range into several sub-ranges as shown in Figure 3.8. If there is mismatch between the unit capacitors, when the input capacitance varies from one sub-range to another, discontinuities will appear in the measurement result due to the errors in the gain factor. To mitigate the discontinuity, dynamic element matching logic is realized in the DAC by alternating the capacitors used in successive cycles of ΔΣ modulator.

There are two common DEM algorithms [20]: single-pointer barrel shifting DEM (see Table 3.1) and double-pointer barrel shifting DEM (see Table 3.2) (assuming, for illustration, that $2C_s$ and $4C_s$ are chosen as references). The single-pointer algorithm sequentially chooses the capacitors in the DAC as the sampling capacitors, while the double-pointer algorithm chooses the capacitors in two separate sequences depending on the bitstream.

Table 3.1 Single-pointer barrel shifting DEM algorithm

<table>
<thead>
<tr>
<th>bitstream</th>
<th>Capacitors chosen</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>$C_1, C_2$</td>
</tr>
<tr>
<td>1</td>
<td>$C_3, C_4, C_5, C_6$</td>
</tr>
<tr>
<td>1</td>
<td>$C_7, C_8, C_9, C_{10}$</td>
</tr>
<tr>
<td>0</td>
<td>$C_{11}, C_{12}$</td>
</tr>
<tr>
<td>1</td>
<td>$C_{13}, C_{14}, C_{15}, C_{16}$</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>0</td>
<td>$C_1, C_2$</td>
</tr>
</tbody>
</table>

Table 3.2 Double-pointer barrel shifting DEM algorithm

<table>
<thead>
<tr>
<th>bitstream</th>
<th>Capacitors chosen</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>$C_1, C_2$</td>
</tr>
<tr>
<td>1</td>
<td>$C_1, C_2, C_3, C_4$</td>
</tr>
<tr>
<td>1</td>
<td>$C_5, C_6, C_7, C_8$</td>
</tr>
<tr>
<td>0</td>
<td>$C_3, C_4$</td>
</tr>
<tr>
<td>1</td>
<td>$C_9, C_{10}, C_{11}, C_{12}$</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>0</td>
<td>$C_1, C_2$</td>
</tr>
</tbody>
</table>
Figure 3.9 INL of capacitance measurement (a) without DEM; (b) with DEM

Figure 3.9 illustrates the effect of DEM logic assuming there is 3% random mismatch between the unit capacitors. Obvious discontinuities are observed without DEM and by applying DEM (double-pointer barrel shifting algorithm), the integral non-linearity (INL) is reduced by a factor of 500.

The switches connecting the sensing capacitors and the virtual ground nodes of OTA are critical because the first stage of the ΔΣ modulator is more sensitive than the second stage. Any leakage current flowing into the virtual ground nodes will affect the integration accuracy. There should be enough isolation between the external pins and virtual ground nodes to minimize external interference. So the switches are designed in a 'T' configuration as shown in Figure 3.10.

Figure 3.10 Switch realization (a) single NMOS switch; (b) 'T' configuration switch

In TDC mode, the ‘mode’ signal is high and the left terminal of the switch is grounded. The leakage current is large due to the large drain-source voltage drop on transistor M1 (common mode voltage) if the single NMOS switch is chosen, as shown in Figure 3.10(a). If the switch is in 'T' configuration as shown in Figure 3.10(b), the drain-source voltage of transistor M6 is almost zero so the leakage current is reduced to a large extent.
Figure 3.11 Leakage current of two kinds of switches

Figure 3.11 shows the leakage current of these two kinds of switches when temperature changes. The leakage current of the single NMOS switch is about 50 times larger than the leakage current of the ‘T’ switch at high temperature.
Capacitance-to-digital converter based on switched-capacitor circuitry
Voltage-sensing realization with built-in temperature-related reference

After one temperature measurement, the temperature $T$ is known. Hence $V_{BE}$ and $\Delta V_{BE}$ can both be calculated according to the formula

$$\Delta V_{BE} = \frac{kT}{q} \ln(p) \quad (4.1)$$

$$V_{BE} = X \cdot \Delta V_{BE} \quad (4.2)$$

Combining the calculated voltages and the $\Delta \Sigma$ modulator, a high resolution ADC that digitizes an external voltage $V_{ext}$ relative to a bandgap reference voltage can be implemented. One method to feed $V_{ext}$ into the modulator is to replace $V_{BE}$ by $V_{ext}$ [9].

The voltage can be obtained from the measured ratio $X_{voltage}$ as

$$V_{ext} = X_{voltage} \cdot \Delta V_{BE} \quad (4.3)$$

However, the range of $V_{BE}$ is quite narrow so a pre-scaler is needed to scale the input voltage (0~$V_{dd}$) to the range of $V_{BE}$, which consumes circuit resources and energy. Additionally, the accuracy of the scaling ratio will directly affect the accuracy of the ADC.

Another method to extend the reference range is to sample the reference multiple times to balance the input in the charge domain. Assuming that the input voltage is 1.8V and minimum $\Delta V_{BE}$ is 29mV at -70°C. The total reference range is then $32 \times 29$ mV = 0.93V. Sampling $k \Delta V_{BE}$ twice and the input voltage once is equivalent to doubling the reference range. This method saves some circuit resources but takes longer conversion time.

A third method is to increase the number of the capacitors in the DAC to extend the reference range. $\Delta V_{BE}$ is 29mV at -70°C so the number should be at least 63 to cover 1.8V input. This method consumes additional circuit resources but saves conversion time.

Using $V_{BE}$ (~630mV at room temperature) to build the reference is also a candidate.
Three capacitors are needed to sample $V_{BE}$ in principle. However, the sub-range after zooming is then much larger compared with using $\Delta V_{BE}$ to build the reference, degrading the benefit of the zoom step.

Here a new double-zoom scheme is presented to measure the input voltage with negligible additional circuitry and conversion time.

4.1 Double-zoom scheme

There are two voltages: $V_{BE}$ (ranging from ~800mV to ~400mV) and $\Delta V_{BE}$ (ranging from ~29mV to ~56mV) in the temperature range from -70°C to 125°C. The first step is to use a multiple of $V_{BE}$ to subtract a large part of the input voltage. The second step is zooming into a smaller range of $2\Delta V_{BE}$ similarly to the zoom step in TDC mode. Then the normal $\Delta\Sigma$ conversion operates to obtain a high resolution measurement. The principle of the double-zoom scheme is shown in Figure 4.1.

![Figure 4.1 Principle of the double-zoom scheme](image)

The extreme condition that most capacitors in the DAC are used happens at -70°C. When the input voltage is $V_{dd}$, at most 2 capacitors are needed to sample $V_{BE}$ and 30 capacitors are needed to sample $\Delta V_{BE}$, so 32 capacitors in the DAC are enough for sampling the reference voltage.

In order to realize this double-zoom scheme, the circuit should have three steps as shown in Figure 4.2.
During the first zoom step, the clocked comparator compares the input voltage and $M \cdot V_{BE}$ ($M$ is the gain factor). The SAR logic adjusts the gain factor until the value $m$ is found for which $mV_{BE}$ is smaller than $V_{ext}$ while $(m + 1)V_{BE}$ is larger than $V_{ext}$. The ratio of the input voltage to $V_{BE}$ is less than 6 so at most 3 comparisons are needed. Then a voltage of $mV_{BE}$ is always subtracted from the input voltage and $N \cdot \Delta V_{BE}$ ($N$ is the gain factor) is compared to the residue voltage until the integer $n$ is found. This step is similar to the coarse step of TDC mode with $V_{BE}$ replaced by the residue voltage $(V_{ext} - V_{BE})$. Because of the first zoom step, this residue voltage is within the range of $V_{BE}$ so the second zoom step can operate properly. After that, the ΔΣ conversion operates normally with two references set to $[mV_{BE} + (n + 1)\Delta V_{BE}]$ and $[mV_{BE} + (n - 1)\Delta V_{BE}]$. A guard-band step is also needed here to determine the sub-range.

The double-zoom scheme can measure the input voltage with only one additional SAR conversion of 3 clock cycles which is negligible and no additional circuit resources. At the same time, it can also zoom into the sub-range of $2\Delta V_{BE}$ so the performance should be comparable to the other methods.

4.2 Voltage-sensing circuit design

The SC circuitry based integration scheme for ADC mode shown in Figure 4.3 is slightly different from that in TDC mode.
A set of $m$ unit capacitors is always used to sample $V_{BE}$, subtracting a large part of the input voltage. $(n - 1)$ or $(n + 1)$ capacitors are chosen depending on the bitstream to sample $\Delta V_{BE}$, balancing the residue voltage. The output voltage of the OTA during $\phi_2$ is proportional to $[V_{ext} - mV_{BE} - (n \pm 1)\Delta V_{BE}]C_s/C_{int}$.

The value of the input voltage can be calculated from the bitstream. Assuming that the length of the bitstream is $N$ and the average value of the bitstream is $x$, the following equations can be derived according to charge balancing principle.

\begin{align*}
    xNC_s[V_{ext} - mV_{BE} - (n + 1)\Delta V_{BE}] + (1 - x)NC_s[V_{ext} - mV_{BE} - (n - 1)\Delta V_{BE}] &= 0 \quad (4.4) \\
    x[V_{ext} - mV_{BE} - (n + 1)\Delta V_{BE}] + (1 - x)[V_{ext} - mV_{BE} - (n - 1)\Delta V_{BE}] &= 0 \quad (4.5)
\end{align*}

So the input voltage is expressed as

$$V_{ext} = mV_{BE} + (n - 1)\Delta V_{BE} + 2x\Delta V_{BE} \quad (4.6)$$

In this equation, $mV_{BE}$ is determined by the first zoom step. $(n - 1)\Delta V_{BE}$ is determined by the second zoom step while $2x\Delta V_{BE}$ is the high-resolution part obtained from the \(\Delta\Sigma\) conversion.
4.2 Voltage-sensing circuit design

In practice, a fully-differential circuitry is used to implement the integration scheme as shown in Figure 4.4. The two BJT-generated voltages $V_{BE}$ and $\Delta V_{BE}$ have the same polarity and both have opposite polarity to the input voltage to realize the balancing in charge domain. The input voltage, $V_{BE}$ and $\Delta V_{BE}$ are swapped during different clock phases.

Figure 4.4 Integration scheme of a fully-differential ADC in clock phase (a) $\varphi_1$; (b) $\varphi_2$

![Figure 4.4 Integration scheme of a fully-differential ADC in clock phase](image)

Figure 4.5 Simplified diagram of the circuit in ADC mode

Figure 4.5 illustrates the circuit diagram of ADC mode.

Three separate system-level chopping signals are used to swap the polarities of the input voltage, $V_{BE}$ and $\Delta V_{BE}$ for more freedom. In TDC mode, $V_{BE}$ and $\Delta V_{BE}$ have opposite polarity to realize the subtraction while in ADC mode, $V_{BE}$ and $\Delta V_{BE}$ have the same polarity to realize the addition.
Additional clock signals ‘\(\varphi_{1,ADC1}\)’, ‘\(\varphi_{1,ADC2}\)’, ‘\(\varphi_{2,ADC1}\)’ and ‘\(\varphi_{2,ADC2}\)’ are generated using additional digital blocks as shown in Figure 4.6. In ADC mode, clock signals ‘\(\varphi_{1,d}\)’ and ‘\(\varphi_{2,d}\)’ are chosen to operate the integration scheme of the input voltage while in the other modes, system-level chopping signals are chosen to keep these signals static and ground the input to avoid charge transfer from the input voltage. The MUX blocks swapping \(V_{BB}\) and \(\Delta V_{BB}\) during different clock phases are not shown in the figure.

DEM logic is also used here to average out the mismatches between the unit capacitors in the DAC.

Two additional capacitors are used to sample the input voltage instead of the capacitors in the DAC. This is because using the capacitors in the DAC will add 64 switches connecting the input voltage to each capacitor and 32 additional control signals are needed to control these switches as well. This would require substantial circuit resources and more importantly, the external interference from the input voltage may degrade the accuracy of TDC mode. The two additional capacitors are only used in ADC mode and they are not involved in DEM operation of the DAC. As a result, the mismatch of these two capacitors will not be averaged out. Assuming that the value of the two additional capacitors (average capacitance) is \((C_s + \Delta C)\), the charge transferred is then \(V_{ext}(C_s + \Delta C)\). The capacitors in the DAC has a capacitance of \(C_s\) due to the DEM logic. So the measured voltage is then \(V_{ext}(C_s + \Delta C)/C_s\). A constant gain error expressed in equation (4.8) appears because of the mismatch.

\[
V_{measured} = V_{ext}(1 + \frac{\Delta C}{C_s}) \tag{4.7}
\]

\[
\delta_{gain} = \frac{\Delta C}{C_s} \tag{4.8}
\]

This constant gain error can be removed by a single-point calibration. One method of calibration is applying an accurate voltage \(V_{accurate}\) to the input and obtaining one output \(V_{measured}\), the gain error can be derived as
4.2 Voltage-sensing circuit design

\[
\delta_{gain} = \frac{V_{measured}}{V_{accurate}} - 1
\]  (4.9)

Another method is measuring the capacitance of the additional capacitors by replacing the input voltage and \(V_{BE}\) with supply voltage \(V_{dd}\) and the measurement result is a direct indication of the capacitance ratio. Assuming the average value of the bitstream is \(x\), the gain error can be calculated as

\[
xV_{dd}[C_s + \Delta C - (n + 1)C_s] + (1 - x)V_{dd}[C_s + \Delta C - (n - 1)C_s] = 0 \tag{4.10}
\]

\[
\delta_{gain} = \frac{\Delta C}{C_s} = 2x + n - 2 = 2x - 1 \tag{4.11}
\]

The mismatch is small so \(\Delta C \approx 0\), \(n = 1\) and at most 2 capacitors in the DAC are used to build the reference. This method does not need the accurate external voltage and utilizes part of the CDC mode circuit. An additional control signal ‘voltage_cal’ is used to configure the circuit in this calibration mode (switches are not shown in the Figure).
Voltage-sensing realization with built-in temperature-related reference
Chip-level design and simulation results

In this chapter, the block diagram of the chip is given and then the detailed core circuit which combines the three sensing modes is discussed. After that, the noise performance for each sensing mode is analysed. The layout of the design and the post-layout simulation results evaluating the circuit are shown.

5.1 Block diagram

Figure 5.1 Block diagram of the chip
Figure 5.1 illustrates the block diagram of the chip including all peripheral circuits.

The chip can be configured in TDC, CDC and ADC modes to measure the temperature, the capacitance and the voltage. There are additional calibration modes for temperature measurement and voltage measurement.

The TDC front-end block consists of the BJT circuit generating the voltages $V_{BE}$ and $\Delta V_{BE}$ and the CDC front-end consists of the switches associated with the external sensing capacitors and the two on-chip test capacitors.

The incremental zoom ADC is used to measure the input signal and the output bitstream is sent off-chip. The inputs of the comparator ‘outp’ and ‘outn’ are sent off-chip as analog test bus ‘atb0’ and ‘atb1’ for test purposes. Analog voltage ‘vR_out’ is the voltage across the resistor $R$ (see Figure 2.4) to sense the value of the current-gain $\beta_F$.

A differential input voltage $V_{cat}$ is used to replace $V_{BE}$ for voltage calibration purposes in TDC mode. A differential input voltage $V_{ext}$ is the input voltage to be measured in ADC mode.

All control signals are stored in three shift registers. The detailed information is listed in Table 5.1.

<table>
<thead>
<tr>
<th>Table 5.1 Control signals stored in the shift registers</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Register 1</strong></td>
</tr>
<tr>
<td>Bit &lt;0&gt; mode1</td>
</tr>
<tr>
<td>Bit &lt;1&gt; mode2</td>
</tr>
<tr>
<td>Bit &lt;2&gt; start_up</td>
</tr>
<tr>
<td>Bit &lt;3,4,5,24,26&gt; dum&lt;4:0&gt;</td>
</tr>
<tr>
<td>Bit &lt;6&gt; bank_swap</td>
</tr>
<tr>
<td>Bit &lt;7,9,11,28,30,32&gt; dem2&lt;5:0&gt;</td>
</tr>
<tr>
<td>Bit &lt;8,10,12,29,31,33&gt; dem1&lt;5:0&gt;</td>
</tr>
<tr>
<td>Bit &lt;13&gt; vR_out_en</td>
</tr>
<tr>
<td>Bit &lt;14&gt; test_en</td>
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<td>Bit &lt;15&gt; eval_sel</td>
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<tr>
<td>Bit &lt;17&gt; vcal_en</td>
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<tr>
<td>Bit &lt;18&gt; vbe_hl</td>
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</table>
5.1 Block diagram

<table>
<thead>
<tr>
<th>Bit</th>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;19&gt;</td>
<td>vR_en</td>
<td>Select the voltage across resistor R as the input signal</td>
</tr>
<tr>
<td>&lt;20&gt;</td>
<td>sys_chop1</td>
<td>System level chopping signal that swaps the polarity of $V_{BE}$</td>
</tr>
<tr>
<td>&lt;21&gt;</td>
<td>sys_chop2</td>
<td>System level chopping signal that swaps the polarity of $\Delta V_{BE}$</td>
</tr>
<tr>
<td>&lt;22&gt;</td>
<td>sys_chop3</td>
<td>System level chopping signal that swaps the polarity of $V_{ext}$</td>
</tr>
<tr>
<td>&lt;23&gt;</td>
<td>ota_chop</td>
<td>Control signal for the choppers of the opamp in the bias circuit</td>
</tr>
<tr>
<td>&lt;25&gt;</td>
<td>sar_sd</td>
<td>Configure the circuit in coarse phase or fine phase</td>
</tr>
<tr>
<td>&lt;27&gt;</td>
<td>beta_en</td>
<td>Add series resistor $R_{bias}/5$ to bias circuit</td>
</tr>
<tr>
<td>&lt;34&gt;</td>
<td>vR_on</td>
<td>Turns on the current through Resistor R</td>
</tr>
<tr>
<td>&lt;35&gt;</td>
<td>voltage_cal</td>
<td>Configure the circuit in calibration mode of voltage sensing</td>
</tr>
</tbody>
</table>

Register 2

<table>
<thead>
<tr>
<th>Bit</th>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;31:0&gt;</td>
<td>vbe_s &lt;31:0&gt;</td>
<td>Control signals for the switches connecting $V_{BE}$ to the capacitors in the DAC</td>
</tr>
</tbody>
</table>

Register 3

<table>
<thead>
<tr>
<th>Bit</th>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;31:0&gt;</td>
<td>dvbe_s &lt;31:0&gt;</td>
<td>Control signals for the switches connecting $\Delta V_{BE}$ to the capacitors in the DAC</td>
</tr>
</tbody>
</table>

Two mode signals are needed for four measurement modes as shown in Table 5.2.

<table>
<thead>
<tr>
<th>mode1</th>
<th>mode2</th>
<th>Measurement mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>TDC mode</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>ADC mode</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>CDC mode with external capacitors</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>CDC mode with on-chip test capacitors</td>
</tr>
</tbody>
</table>

The values of some of the control signals depend on the bitstream. Instead of loading the signals in every clock cycle in order to change their values depending on the current value of the bitstream, two options for each signal are loaded before the conversion. The value of the bitstream is used to select which value is used in every clock cycle. This helps to increase the sampling frequency and reduces the activity of the shift registers during the conversion. It comes at the cost of doubling the size of the shift registers. The clock generation block generates the non-overlapping clocks and their delayed versions. A load signal is used to load the shift registers in the time interval when $\varphi_1$ and $\varphi_2$ are both low.

Two separate supply voltages VDD_A and VDD_D are used for analog supply and digital supply respectively. Supply VDD_E and VSS_E are for the padring.
5.2 Transistor-level circuit diagram

Combining all sensing modes, the transistor-level circuit diagram is shown in Figure 5.2 (excluding the temperature-sensing front-end and the peripheral circuits).

![Transistor-level circuit diagram for all modes](image)

The signal ‘CDC’ is generated by combinatorial logic from signals ‘mode1’ and ‘mode2’. It is high when the circuit is in CDC mode and low in the other modes. The signal ‘CDC_cal’ is generated from signals ‘CDC’ and ‘voltage_cal’. It is high in CDC mode or during the calibration step of ADC mode to measure the sampling capacitance $C_s$ (see Section 4.2) and low in the other modes.

5.3 Noise analysis

In this section, both quantization noise and thermal noise of the circuit are analysed and system-level simulation results based on the noise analysis are given.

The quantization noise of the ΔΣ modulator introduced by the comparator is shaped to higher frequencies by the 2nd order noise shaping. In incremental case, the measurand varies slowly so the input can be seen a low frequency signal. After low-pass filtered, the high frequency quantization noise is filtered out. So in this design, the thermal noise is the dominant one that limits the resolution performance.
5.3 Noise analysis

According to [21], the total noise power of a switched-capacitor circuitry can be expressed as

\[ \overline{v_n^2} = \frac{kT}{C} \left( \frac{7}{3} + 2\rho \frac{1}{1 + \rho} \right) \]  

(5.1)

where \( C \) is the sampling capacitance and \( \rho = 2R_{on}g_m, R_{on} \) is the on-resistance of the switch and \( g_m \) is the transconductance of the OTA. In this design, the settling speed is limited by the OTA instead of the switches, which means \( g_m \ll 1/R_{on} \). So \( \rho \ll 1 \) and then the noise power is \( \overline{v_n^2} = \frac{7kT}{3C} \). This noise is sampled on the sampling capacitors, resulting in a noise charge of \( \sqrt{\frac{7}{3}kTC} \).

5.3.1 TDC mode

In TDC mode, assuming that the length of the bitstream is \( N \) and the average value is \( x \). Then there are \( xN \) times of using \( (n + 1)C_s \) to sample \( \Delta V_{BE} \) and \( (1 - x)N \) times of using \( (n - 1)C_s \). One extra \( C_s \) is used to sample \( V_{BE} \) in every clock cycle so it’s used for \( N \) times. The total rms noise charge can be expressed as

\[ Q_{\text{noise}} = \sqrt{\frac{7}{3}kTN[C_s + x(n+1)C_s + (1-x)(n-1)C_s]} \]

\[ = \sqrt{\frac{7}{3}kTN}[2x + n] \]  

(5.2)

Because of the charge balancing principle, the integrated noise charge equals the signal charge integrated after a certain time of conversion, which can be written as

\[ -Q_{\text{noise}} = Q_{\text{signal}} \]

\[ -Q_{\text{noise}} = xNC_s[V_{BE} - (n + 1)\Delta V_{BE}] + (1-x)NC_s[V_{BE} - (n - 1)\Delta V_{BE}] \]  

(5.4)

So the decimated value \( x \) can be derived as

\[ x = \frac{V_{BE} - (n - 1)\Delta V_{BE}}{2\Delta V_{BE}} + \frac{Q_{\text{noise}}}{2NC_s\Delta V_{BE}} \]  

(5.5)

The noise component in the decimated value is

\[ \sigma_x = \frac{Q_{\text{noise}}}{2NC_s\Delta V_{BE}} = \sqrt{\frac{7}{3}kTN}[2x + n] \]

(5.6)

This noise component is proportional to \( \sqrt{1/NC_s} \) so larger sampling capacitors and longer conversion time reduce the thermal noise while consuming more area and longer time. The relationship between the temperature resolution and conversion time is expected to be a straight line with a slope of -0.5 in logarithmic coordinate. The temperature resolution is expected to reach 16mK after 125 clock cycles (5ms conversion time).
The system-level simulations for TDC mode circuit have been done with the ΔΣ modulator model shown in Figure 5.3.

![ΔΣ modulator model in TDC mode](image)

The two references in the model are chosen to be ±1 \((n ± 1)ΔV_{BE}\) in the real design) so the input signal \(i_n\) is the normalized input voltage which is expressed as

\[
i_n = \frac{V_{BE} - nΔV_{BE}}{ΔV_{BE}}
\]  

(5.7)

In every clock cycle, the noise voltage can be written as

\[
v_n = \sqrt{\frac{7}{3}kT[C_s + (n ± 1)C_s]/C_s}
\]  

(5.8)

The number of sampling capacitors used depends on the bitstream. So the normalized noise in the model is expressed as

\[
\text{noise} = \frac{\sqrt{7/3kT[C_s + (n ± 1)C_s]}}{ΔV_{BE}C_s}
\]  

(5.9)

![24000-point FFT plot of the bitstream in TDC mode](image)

Figure 5.4 illustrates the Fast Fourier Transform (FFT) plot of the bitstream in TDC mode. A slope of 40dB/dec is observed at higher frequencies and low frequency thermal noise level is around -85dB which can translate to about 18mK temperature resolution in 200Hz noise bandwidth.
5.3 Noise analysis

Figure 5.5 shows how the noise of the temperature measurement changes with conversion time (It is obtained by using 30 samples of the bitstream in certain conversion time and calculating their standard deviation). When conversion time is shorter than about 2ms, the quantization noise is the dominant noise component and the relationship can be expressed as $A/t^2$, where $A$ is a constant and $t$ is conversion time. When conversion time is longer than 2ms, the thermal noise is the dominant one and the relationship can be expressed as $B/t^{0.5}$, where $B$ is a constant.

5.3.2 CDC mode

In CDC mode, the supply voltage is sampled on the sensing capacitor and the sampling capacitors, so the noise charge can be derived similarly to TDC mode as

$$Q_{\text{noise}} = \sqrt{\frac{7}{3}kTN[C_{\text{sensor}} + x(n + 1)C_s + (1 - x)(n - 1)C_s]}$$

$$= \sqrt{\frac{14}{3}kTN C_{\text{sensor}}}$$

(5.10)

where $C_{\text{sensor}} = (n - 1)C_s + 2xC_s$ according to equation (3.4).

Due to the charge balancing principle, the decimated value can be derived as

$$-Q_{\text{noise}} = xNV_{dd}[C_{\text{sensor}} - (n + 1)C_s] + (1 - x)NV_{dd}[C_{\text{sensor}} - (n - 1)C_s]$$

$$\Rightarrow x = \frac{C_{\text{sensor}} - (n - 1)C_s}{2C_s} + \frac{Q_{\text{noise}}}{2NV_{dd}C_s}$$

(5.11)

(5.12)

The noise component in the decimated value is

$$\sigma_x = \frac{Q_{\text{noise}}}{2NV_{dd}C_s} = \frac{\sqrt{\frac{14}{3}kTN C_{\text{sensor}}}}{2NV_{dd}C_s}$$

(5.13)
According to equation (5.13), the capacitance resolution is expected to reach 4.9aF after 500 clock cycles (20ms conversion time) which meets the specifications.

The system-level simulations of CDC mode have been done by adding the thermal noise into the ΔΣ modulator model shown in Figure 5.6.

![ΔΣ modulator model in CDC mode](image)

The coefficient of the first integrator is changed to 0.05 because of the extra capacitor added to the integration capacitor (see Section 3.2). The two references in the model are chosen to be \(\pm 1 ((n \pm 1)C_s \text{ in the real design}) \) so the input signal \(in\) is the normalized input capacitance which is expressed as

\[
\text{in} = \frac{C_{\text{sensor}} - nC_s}{C_s}
\]  

(5.14)

In every clock cycle, the noise voltage can be written as

\[
\nu_n = \sqrt{\frac{7}{3}kT(C_{\text{sensor}} + (n \pm 1)C_s)/C_s}
\]  

(5.15)

The number of sampling capacitors used depends on the bitstream. So the normalized noise in the model is expressed as

\[
\text{noise} = \sqrt{\frac{7}{3}kT(C_{\text{sensor}} + (n \pm 1)C_s)}
\]  

(5.16)

Compared to the normalized noise in TDC mode, \(V_{dd}\) is about 43 times of \(\Delta V_{BE}\) at room temperature while the sampling capacitors in CDC mode is approximately doubled due to the sensing capacitor. So the noise level of CDC mode is expected to be reduced by 29dB compared to the noise level in TDC mode.
5.3 Noise analysis

Figure 5.7 24000-point FFT plot of the bitstream in CDC mode

Figure 5.7 illustrates the FFT plot of the bitstream in CDC mode. A thermal noise level of about -110dB is obtained which can translate to 5aF capacitance resolution in 50Hz noise bandwidth.

Figure 5.8 Capacitance measurement noise vs. conversion time

Figure 5.8 shows the plot of capacitance measurement noise vs. conversion time. When the conversion time is shorter than 15ms, the quantization noise is the dominant noise component while when the conversion time is longer than 15ms, the thermal noise is the dominant one. The capacitance resolution reaches 5aF when the conversion time is 20ms which is in agreement with the noise analysis.
5.3.3 ADC mode

In ADC mode, the difference to TDC mode is that several capacitors are needed to sample $V_{BE}$. Assuming that $m$ capacitors are used to sample $V_{BE}$, $(n + 1)$ or $(n - 1)$ capacitors are used to sample $\Delta V_{BE}$, the length of the bitstream is $N$ and the average value is $x$. There is always one extra capacitor sampling the input voltage. So the noise charge can be expressed as

$$Q_{\text{noise}} = \sqrt{\frac{7}{3} kT} N \left[ (m + 1) C_s + x(n + 1) C_s + (1 - x)(n - 1) C_s \right]$$

$$= \sqrt{\frac{7}{3} kT} N C_s (2x + n + m) \quad (5.17)$$

The decimated value can be derived by applying the charge balancing principle as

$$-Q_{\text{noise}} = x N C_s [V_{\text{ext}} - m V_{BE} - (n + 1) \Delta V_{BE}] + (1 - x) N C_s [V_{\text{ext}} - m V_{BE} - (n - 1) \Delta V_{BE}]$$

$$x = \frac{V_{\text{ext}} - m V_{BE} - (n - 1) \Delta V_{BE}}{2 \Delta V_{BE}} + \frac{Q_{\text{noise}}}{2 N C_s \Delta V_{BE}} \quad (5.18)$$

The noise component in the decimated value is

$$\sigma_x = \frac{Q_{\text{noise}}}{2 N C_s \Delta V_{BE}} = \frac{\sqrt{\frac{7}{3} kT} N C_s (2x + n + m)}{2 N C_s \Delta V_{BE}} \quad (5.20)$$

Because in most cases $m$ is small, ADC mode is expected to have the same noise level as TDC mode. The voltage resolution is expected to reach 98µV after 125 clock cycles (5ms conversion time) which meets the specifications.

The system-level simulations have been done with the same ΔΣ modulator model shown in Figure 5.3. The two references are set to ±1 ($m V_{BE} + (n \pm 1) \Delta V_{BE}$ in the real design). The normalized input is expressed as

$$in = \frac{V_{\text{ext}} - m V_{BE} - n \Delta V_{BE}}{\Delta V_{BE}} \quad (5.21)$$

The normalized noise is expressed as

$$\text{noise} = \frac{\sqrt{\frac{7}{3} kT} \left[ C_s + m C_s + (n \pm 1) C_s \right]}{\Delta V_{BE} C_s} \quad (5.22)$$
5.3 Noise analysis

Figure 5.9 24000-point FFT plot of the bitstream in ADC mode

Figure 5.9 illustrates the FFT plot of the bitstream in ADC mode. A thermal noise level of about -85dB is obtained similarly to the level in TDC mode which can translate to 100µV voltage resolution in 200Hz noise bandwidth.

Figure 5.10 Voltage measurement noise vs. conversion time

Figure 5.10 shows the plot of voltage measurement noise vs. conversion time. When the conversion time is shorter than 2ms, the quantization noise is the dominant noise component while when the conversion time is longer than 2ms, the thermal noise is the dominant one. The voltage measurement resolution reaches 90µV in 5ms conversion time which is in agreement with the noise analysis.
5.4 Layout

The layout of the design is shown in Figure 5.11. The core occupies an area of 689µm×286µm=0.2mm² exclude the two test capacitors. The whole chip including the bond-pad and the seal-ring occupies an area of 1160µm×871µm=1.01mm² which is slightly larger than the existing TDC design (0.98mm²).

The chip has been taped out in NXP C14 technology (160nm process), and will be packaged in a 28-pin ceramic DIL package.

5.5 Transistor-level simulation results

In this section, the transistor-level post-layout simulation results for the three sensing modes are given and the performances of the circuit are evaluated.

5.5.1 TDC mode

The TDC mode circuit consumes 4.6µA current from a 1.8V supply including 2.7µA consumed by the temperature-sensing front-end (0.96µA consumed by the bias circuit, 0.96µA consumed by the bipolar core and 0.8µA consumed by the dummy BJT) which is the same as the TDC design presented in chapter 2. Most importantly, the TDC mode circuit should have comparable performance to the existing TDC design. A critical error source introduced by the addition of the other modes is shown in Figure 5.12.
5.5 Transistor-level simulation results

Figure 5.12 Leakage current flowing into the BJT front-end

In TDC mode, the CDC mode clock signals ‘\(\phi_{1,CDC1}\)’, ‘\(\phi_{2,CDC1}\)’, ‘\(\phi_{1,CDC2}\)’, ‘\(\phi_{2,CDC2}\)’ are static. The switch controlled by ‘CDC_cal’ is off, disconnecting the supply voltage from the sampling capacitors. However, leakage current along the red path in Figure 5.12 will flow into the temperature-sensing front-end, which affects the bias current of the PNPs, causing errors in the voltages \(V_{BE}\) and \(\Delta V_{BE}\). These errors have been simulated and are shown in Figure 5.13.

\[V_{BE2}\] is connected to the zoom ADC in the simulation so the leakage current mainly causes an error in \(V_{BE2}\) while \(V_{BE1}\) remains almost the same. The error is low (~1μV) at
low temperature but it increases a lot to ~10μV at high temperature.

The errors in $V_{BE}$ and $\Delta V_{BE}$ will translate to an error in temperature measurement. According to $X = V_{BE}/\Delta V_{BE}$, its derivative can be expressed as

$$dX = \frac{1}{\Delta V_{BE}} dV_{BE} - \frac{V_{BE}}{(\Delta V_{BE})^2} d\Delta V_{BE}$$  \hspace{1cm} (5.23)

According to equation (2.8), the derivative of $\mu$ can be expressed as

$$d\mu = \frac{-\alpha}{(\alpha + X)^2} dX$$  \hspace{1cm} (5.24)

According to equation (2.7), the derivative of $D_{out}$ can be expressed as

$$dD_{out} = A d\mu$$  \hspace{1cm} (5.25)

So the error of the temperature measurement is calculated and plotted in Figure 5.14.

![Figure 5.14 Calculated temperature measurement error](image)

Figure 5.14 Calculated temperature measurement error (a) without polynomial fit; (b) with 3rd order polynomial fit

Figure 5.14(a) shows the calculated temperature error due to the inaccuracy of $V_{BE}$ and $\Delta V_{BE}$ introduced by the addition of the other modes. At high temperatures, an error of more than 20mK is introduced which will degrade the temperature measurement performance. However, there is a necessary polynomial fit step in the temperature measurement by using a fixed polynomial obtained from batch-calibration [8]. After a 3rd order polynomial fit, the temperature error can be reduced to less than 2.5mK which is negligible compared with 60mK accuracy (shown in Figure 5.14(b)). This estimation is effective if the leakage current is systematic (They don’t spread a lot from sample to sample so the batch-calibration can work).
5.5 Transistor-level simulation results

Figure 5.15 24000-point FFT plot of the bitstream in TDC mode

Figure 5.15 illustrates the FFT plot in TDC mode at room temperature (27°C) obtained from transient simulation. A thermal noise level of -85dB is obtained which is in-line with the system-level simulation result. It also confirms the correctness of the noise analysis.

Figure 5.16 Temperature resolution vs. conversion time

Figure 5.16 shows the simulated temperature resolution vs. conversion time at room temperature. The quantization noise dominates in shorter conversion time while the thermal noise dominates in longer conversion time. A temperature resolution of 14mK is obtained in 5ms conversion time. The result is in-line with the system-level simulation result where 16mK resolution is obtained in 5ms conversion time. Moreover, the transistor-level simulation results are also in agreement with the measurement results of the TDC design presented in chapter 2.
The simulation results confirm that negligible influences are introduced by the modifications. The performance of TDC mode is expected to be comparable to the existing TDC design.

### 5.5.2 CDC mode

When the circuit is configured in CDC mode, it draws 4.6µA current from a 1.8V supply voltage which is the same as TDC mode.

![Figure 5.17 24000-point FFT plot of the bitstream in CDC mode](image)

Figure 5.17 shows the FFT plot of CDC mode circuit measuring the on-chip 2pF test capacitor. A thermal noise level of -110dB is obtained which is the same as the system-level simulation.

![Figure 5.18 Capacitance resolution vs. conversion time](image)
5.5 Transistor-level simulation results

Figure 5.18 shows the relationship between capacitance resolution and conversion time. 4aF capacitance resolution is obtained in 20ms conversion time which is in-line with the system-level simulation where 5aF resolution is obtained in 20ms conversion time.

The following Figure of Merit (FoM) is used to compare the energy efficiency of different CDCs

\[
ENOB = 20 \log \left( \frac{C_{\text{range}}}{2 \sqrt{2} C_{\text{resolution}}} \right) - 1.76
\]

\[
FoM = \frac{\text{Power} \times \text{Conv. Time}}{2^{ENOB}}
\]

where ENOB is the effective number of bits.

The optimal FoM is obtained at the boundary of the quantization-noise dominant region and the thermal-noise dominant region. In this design, 4aF resolution is obtained in 20ms conversion time. The capacitance range is 3.84pF and the circuit draws 4.6μA current from a 1.8V supply. So the FoM is 0.6pJ/conv-step which is 4 times of the state-of-the-art (see Table 6.1).

Moreover, increasing the clock frequency means shorter settling time for the signals, resulting in larger settling errors. However, in most CDC applications, a calibration step is always needed due to the large parasitic capacitances. So the accuracy is not the most important specification. Simulation has been done by doubling the clock frequency to 50kHz.

![24000-point FFT plot of the bitstream in CDC mode](image)

Figure 5.19 shows the FFT plot of CDC mode with a 50kHz frequency clock. The thermal noise level remains at -110dB.
5aF resolution is obtained in 10ms conversion time according to Figure 5.20 which results in a FoM of 0.37pJ/conv-step. A factor of ~2 is obtained by doubling the clock frequency.

Figure 5.21 illustrates the power-supply sensitivity of the CDC mode circuit measuring the 2pF on-chip test capacitor. When the supply voltage is larger than 1V, the circuit is functional with a maximum capacitance error of 22fF. When the supply voltage is lower than 1V, the circuit is not functional. In the specification supply range (1.6~2.0V), the power-supply sensitivity is about 3fF/V.

5.5.3 ADC mode

In ADC mode, the circuit also consumes 4.6µA current from a 1.8V supply.
5.5 Transistor-level simulation results

Figure 5.22 24000-point FFT plot of the bitstream in ADC mode

Figure 5.22 shows the FFT plot of ADC mode. The thermal noise level is -85dB which is in agreement with the system-level simulation. It also confirms that the noise performances of TDC and ADC modes are similar.

Figure 5.23 Voltage resolution vs. conversion time

According to Figure 5.23, 85µV resolution is obtained in 5ms conversion time which is in agreement with the system-level simulation where 90µV resolution is obtained in 5ms conversion time. The full range of the input voltage is 0~V_{dd}. So the resolution is equivalent to 14 bits.
Figure 5.24 shows the power-supply sensitivity of the ADC mode circuit measuring a 0.9V input voltage. The circuit is functional when the supply voltage is larger than 1.3V with a maximum voltage error of 250µV. When the supply voltage is lower than 1.3V, the circuit is not functional. In the specification supply range (1.6~2.0V), the power-supply sensitivity is about 75µV/V which is equivalent to 82.5dB power-supply rejection ratio (PSRR).

The inaccuracy of the temperature measurement (60mK (±3σ)) will translate to errors in $V_{BE}$ and $\Delta V_{BE}$. Since $V_{BE}$ and $\Delta V_{BE}$ are correlated according to equation $V_{BE} = X\Delta V_{BE}$. Assuming that the temperature error comes fully from the inaccuracy of $V_{BE}$, the inaccuracy of the voltage measurement can be estimated.

Figure 5.25(a) illustrates the inaccuracy of $V_{BE}$ translated from 60mK temperature error according to equation (5.25), (5.24) and (5.23) which reaches 350µV at -70°C. The inaccuracy of $V_{BE}$ then translates to the voltage measurement error according to equation (4.6) and the external voltage is assumed to be 1.8V (shown in Figure 5.25(b)).
Discontinuities are observed because the sub-range of the first zoom step changes (see Section 4.1). As a result, the number of capacitors used to sample $V_{BE}$ changes. Maximum 770µV voltage measurement inaccuracy is obtained at 125°C.

In practice, most of the voltage measurements happen at room temperature. The calibration of temperature measurement mainly takes place at room temperature as well. So the inaccuracy of the temperature at room temperature is small. As a result, the inaccuracy of the voltage measurement introduced by the temperature error is expected much lower than the calculation (i.e., when the temperature error is 20mK, the inaccuracy of the voltage measurement is then 160µV at room temperature).
Conclusion

6.1 Thesis contribution

A multi-sensor interface with temperature, capacitance and voltage sensing functionalities has been presented in this thesis. The circuit can be configured in different modes to measure ambient temperature, the capacitance of an external capacitive sensor, or an external voltage. The contributions of the thesis are summarized below:

- Capacitance sensing and voltage sensing functionalities have been added to the existing TDC design. The simulation results show that all sensing modes are functional.
- The error sources introduced to TDC mode have been analysed and simulated. The results show that the performance of the temperature measurement is expected to be comparable to the existing TDC design.
- The CDC mode circuit can achieve a FoM of 0.37pJ/conv-step according to the simulations. Table 6.1 compares the performance of this design with the prior-art CDCs.

Table 6.1 Performance summary of thesis design and the state-of-the-art CDCs

<table>
<thead>
<tr>
<th>Technology</th>
<th>This work</th>
<th>[20]</th>
<th>[2]</th>
<th>[6]</th>
<th>[5]</th>
<th>[7]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>1.8V (1.6V)</td>
<td>1.8V</td>
<td>1.2V</td>
<td>1.0V</td>
<td>1.4V</td>
<td>1.2V</td>
</tr>
<tr>
<td>Supply current</td>
<td>4.6µA</td>
<td>3µA</td>
<td>8.6µA</td>
<td>1.84µA</td>
<td>24µA</td>
<td>0.13µA</td>
</tr>
<tr>
<td>Area</td>
<td>0.2mm²</td>
<td>0.18mm²</td>
<td>0.28mm²</td>
<td>2.6mm²</td>
<td>0.46mm²</td>
<td>0.49mm²</td>
</tr>
<tr>
<td>Conversion time</td>
<td>10ms</td>
<td>30ms</td>
<td>0.8ms</td>
<td>0.019ms</td>
<td>0.23ms</td>
<td>4ms</td>
</tr>
<tr>
<td>Input range</td>
<td>0~3.84pF</td>
<td>0~1.8pF</td>
<td>0.5~1.0pF</td>
<td>0~10nF</td>
<td>0~24pF</td>
<td>2.5~75.3pF</td>
</tr>
<tr>
<td>Resolution</td>
<td>5aF</td>
<td>6aF</td>
<td>70aF</td>
<td>12.3fF</td>
<td>0.16fF</td>
<td>6fF</td>
</tr>
<tr>
<td>ENOB</td>
<td>17.8bit</td>
<td>16.4bit</td>
<td>12.5bit</td>
<td>8.0bit</td>
<td>15.4bit</td>
<td>11.8bit</td>
</tr>
<tr>
<td>FoM</td>
<td>0.37pJ/conv</td>
<td>1.77pJ/conv</td>
<td>3.9pJ/conv</td>
<td>0.14pJ/conv</td>
<td>0.18pJ/conv</td>
<td>0.18pJ/conv</td>
</tr>
</tbody>
</table>
A new double-zoom scheme is proposed to measure an external voltage with negligible additional circuit resources and conversion time. The performance of the circuit in ADC mode is summarized in Table 6.2.

Table 6.2 Performance of ADC mode circuit

<table>
<thead>
<tr>
<th>ADC mode performance</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>1.6~2.0V</td>
</tr>
<tr>
<td>Supply current</td>
<td>4.6µA</td>
</tr>
<tr>
<td>Area</td>
<td>0.2mm²</td>
</tr>
<tr>
<td>Temperature range</td>
<td>-70~125°C</td>
</tr>
<tr>
<td>Input range</td>
<td>0~Vdd</td>
</tr>
<tr>
<td>Conversion time</td>
<td>5ms</td>
</tr>
<tr>
<td>Resolution</td>
<td>90µV (14bit)</td>
</tr>
<tr>
<td>Inaccuracy</td>
<td>770µV</td>
</tr>
<tr>
<td>PSRR</td>
<td>82.5dB</td>
</tr>
</tbody>
</table>

6.2 Future work

Measurements need to be done on the chip to evaluate the performance of the different sensing modes.

In TDC mode

- The relationship between the temperature resolution and conversion time should be calculated from the bitstream.
- The accuracy of the temperature measurement should be determined by sweeping the temperature from -70°C to 125°C.
- The power-supply sensitivity should be investigated.
- The thermal calibration and voltage calibration methods should both be evaluated.

In CDC mode

- The relationship between the capacitance resolution and conversion time should be calculated from the bitstream by measuring the test capacitors.
- The resolution at different clock frequencies should be measured to find the frequency range at which the chip achieves its optimal energy efficiency.
- The power-supply sensitivity should be investigated.
- Two matched pressure sensors will be connected to the chip as the external capacitors. The INL will be approximated by slowly changing the pressure, which will slowly change the capacitance of the pressure sensors, thus demonstrating whether there are any discontinuities between the sub-ranges of the zoom CDC.
- Additional measurements can be done to compensate the temperature cross-sensitivity of a temperature-dependent capacitive sensor to demonstrate the value of combined temperature and capacitance sensing.
6.2 Future work

In ADC mode

- The relationship between the voltage resolution and conversion time should be calculated from the bitstream.
- The signal-to-noise ratio (SNR) should be measured by DC sweeping the input voltage.
- The power-supply sensitivity should be investigated.
- The DNL and INL should both be measured by applying an input voltage sweeping from 0 to V_{dd}.
- The temperature drift of the reference voltage should be measured by applying a fixed input voltage and sweeping the temperature from -70°C to 125°C. The measured voltage error is an indication of the reference drift.

There are several possibilities to further improve the design.

- A more power-efficient design can be used to reduce the power consumption.
- 3rd order ΔΣ modulator can be implemented to reach the same resolution level in shorter conversion time.
- An option that the temperature-sensing front-end is disconnected from the supply in CDC mode can be added. The current consumption is then reduced to 1.9μA, resulting in a FoM of 0.15pJ/conv-step which is competitive to the state-of-the-art CDCs.
References


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Wei Wu
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