An Ultra Low Power Fully Integrated Sensor Interface IC for Pacemaker

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Abstract

When the heart does not function properly, an artificial pacemaker is needed to correct the heart beat. However, more functionality at limited budget requires less power per function. Therefore, the power consumption of the pacemaker has to be reduced. The analog to digital converter in the pacemaker consumes the largest amount of power in the front-end, called the sense amplifier. Hence, an ultra low power ADC is . In this work, the IECG signal is filtered by band pass filter 50mHz-100Hz. Then, the signal output of the filter is converted to current by transconductance cell(Gm). The output of the Gm-cell is digitized by a Current Successive Approximation ADC. Circuit Simulation predict the overall system consumes the lowest power,416nW reported when compared with the state of the art.

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1 Introduction

In this chapter, a background about the functionality of the heart is introduced. An overview of the pacemaker is presented. ECG signal is explained briefly. In order to have good understanding of low power circuit design, different aspects of weak inversion operation of CMOS transistors are explained. Finally, the motivation and outline of the thesis is presented.

1.1 Background

The heart as electrophysiological system controls the speed and rhythm of the heart beat. An electrical signal goes from the top of the heart to the bottom with each heartbeat. In the sinoatrial node (SA node) the cells generats electrical signals with a frequency of about 70 beats/min . These cells (pacemaker cells) directly control the heart rate. The electrical signal is triggering the rhythmic contractions of the heart muscle. The whole heart takes about 100ms to be excited. It takes the heart, at rest ,180ms to conduct from the sinus node to the atrio-ventricular node (AV) as shown in Fig. 1[1].

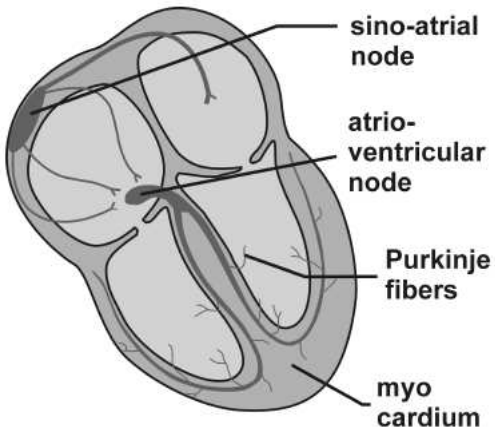

Figure 1: The four-chamber system of the heart and the excitatory and conductive system[1]

The Alrio vertical conduction time (AVCT) is controlled by the autonomous nervous system (ANS). If the body goes through physical or emotional stress, the heart rate increases.

1.1.1 Pacemaker & ECG

- Pacemaker

A pacemaker is a medical device that delivers low-energy electrical pulses to correct abnormal the heart beat, via the electrodes connected to the heart muscles, as shown in Fig. 2 [2]. The main functionality of the artificial pacemaker is to regulate the heart rate as the heart's natural pacemaker is too slow or absent [3].

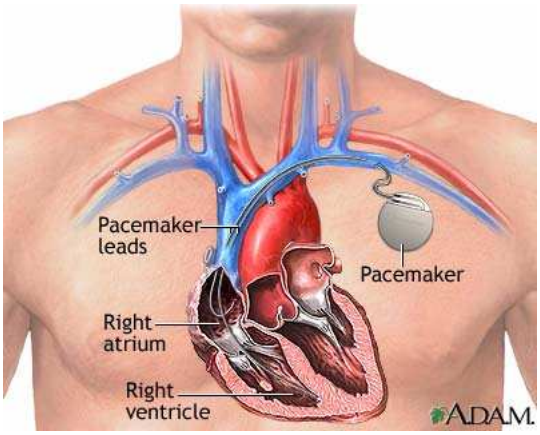

Figure 2: Pacemaker inside the patient's' chest[2]

A pacemaker consists of a battery, usually a lithium battery, processor (generator) , wires with electrodes connected to the heart. The generator is placed below the chest wall above the muscles. A metal box contains the battery and the processor. The metal box is fabricated with titanium in order for the body not to be rejected [4].

The processor ,which is a IC, sends the electrical pulses to the heart to correct the beat. The chip is programmed to send the correct type of pulses to the heart. Also, the IC chip records the activity of the heart in order for the doctor or specialist to tune the pacemaker to perform sufficiently depending on the heart rhythm.

- ECG

The pacemaker needs to monitor the heart beat in order to supply the right pulls. A recording of a human heart beat is known as Electrocardiograph (ECG) and is shown in Fig. 3 [5].

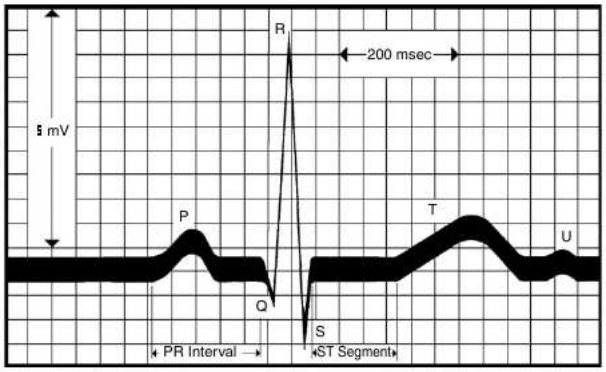

Figure 3: Frequency vs Amplitude for ECG Signal[5]

The ECG can be measured by placing electrodes on the skin. Electrodes are placed in different sides of the heart in order to measure the different activities of the heart. If there are any damages or abnormal rhythm, the ECG gives clear indication about the overall rhythm of the heart[6].

From Fig. 3 , an ECG signal has subsequent waves which are labeled P, Q, R, S and T. The waves originate from the depolarization and repolarization of the muscles in the heart. In this thesis, QRS complex and T wave are considered as required by the pacemaker. The signal which are detected by the electrode are

converted to digital by ADC inside the pacemaker. The Internal ECG signal has frequency-band (50m~100Hz) and amplitude 5mV[5]. To filter the IECG with low noise and an utral low power, transistors have to opearte in weak inversion.

1.1.2 Weak Inversion CMOS

In weak inversion, QI(inversion layer charge) is an exponential function of gate voltage as show in Fig. 4 [7]. Also, QI is much less than the depletion region charge (QB)[7, 8].

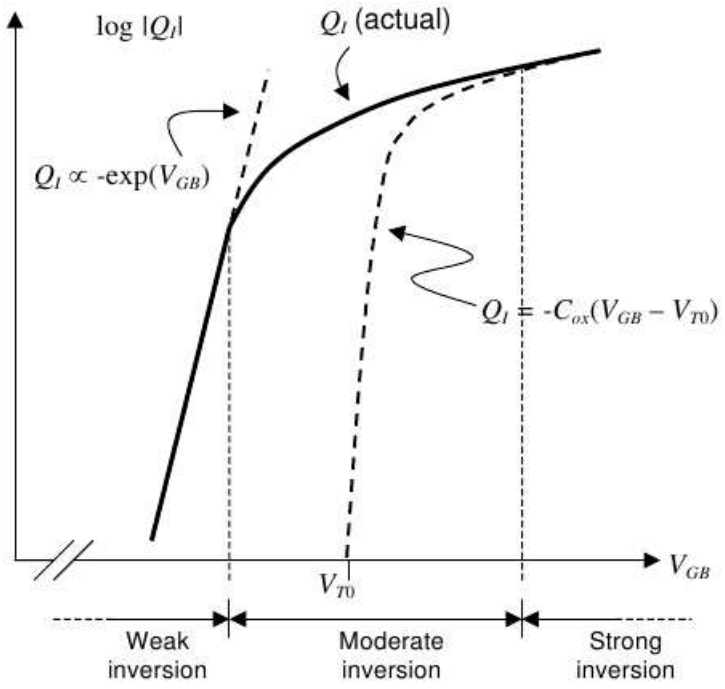

Figure 4: Region of Operations of a Transistor[7]

In weak inversion, currents flows by diffusion, not drift, because the channel does not have enough charge to generate a significant electric field which pulls electrons from the source to the drain.

Drain current and gm are expressed by Equ. 24,25. The MOSFET in weak inversion behaves very similar to bipolar transistor[7, 8, 9, 10]

$$I_D = \frac{W}{L} I_{DO} \exp(\frac{\kappa Vg - Vs}{V_T}) \text{ for } V_{DS} \geq 4V_T \tag{1}$$

Where I_D is the drain current, W is width, L is length, I_{DO} is zero-bias current, V_g is gate voltage, Vs is the source voltage, V_T is thermal voltage, κ is gate coupling coefficient.

$$g_m = \frac{I_D}{nKT/q} \tag{2}$$

Where K is $1.38 \,.\, 10^{-23}$J/K (Boltzmann's constant), q is $1.60 \,.\, 10^{-19}$ C (elementary charge), T is temperature, n is sub-threshold slope.

As noticed in Equ. 24, I_D changed as V_{gs} increased. Also, gm is function of drain current and n(sub-threshold slope). To keep a MOSFET in saturation V_{DS} should be greater or equal to $4V_T$, approximately 100mV, as shown in Fig. 5 [7].

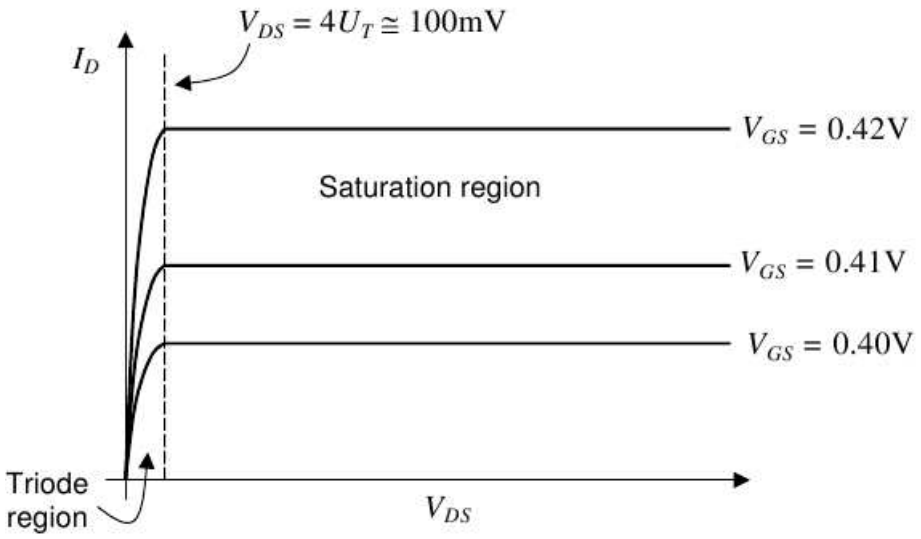

Figure 5: I_{DS} vs I_{DS} in Weak Inversion[7]

To have better understanding of the whole system, an accurate equations of the parasitic capacitance is needed. The parasitic capacitance in weak inversion are calculated as follows[11].

$$C_{gs} = C_{ox.} I_f \tag{3}$$

$$C_{gd} = C_{ox.} I_r \tag{4}$$

$$C_{gb} = C_{ox.} \frac{n-1}{n} \tag{5}$$

Where C_{gs} is gate-to-source capacitance, C_{gd} is gate-to-drain capacitance, C_{gb} gate-to-bulk capacitance, Cox is the gate oxide capacitance per unit area, I_f is forward normalized current, $I_r$is reverse normalized current and n is sub-threshold slope.

The value of sub-threshold slope(n) varies in different technologies. In this design, n is calculated by simulating single NMOS and PMOS. The fundamental minimum of n is 1. Also, the value of the n depends on the value of the current. The value of n for NMOS and PMOS is plotted in Fig. 6,7. Giving the operation current of the filter of 37nA, n_{NMOS} is equal to 1.62 and n_{PMOS} is equal to 1.945. The sub-threshold slope(n) is calculated by Equ. 25.

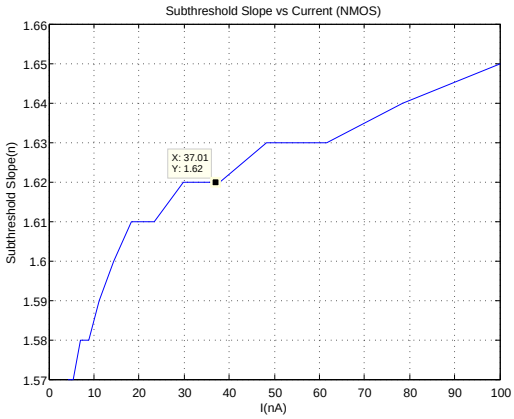

Figure 6: Drain Current vs sub-threshold slope of Single NMOS

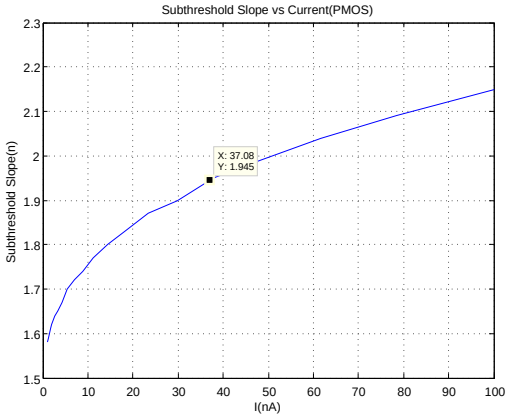

Figure 7: Drain Current vs sub-threshold slope of Single PMOS

As shown in Fig. 6,7, as the current increased the value of n increased.

1.2 Motivations

The life time of pacemaker is approximated to be around 5 to 10 years- an average of seven years [12]. However, more functionality at limited budget requires less power per function. Therefore, the power consumption of the pacemaker has to be reduced. The analog to digital converter in the pacemaker consumes the largest amount of power in the front-end, called the sense amplifier. Also, noise is major concern when an ultra power circuit design is needed. To achieve such low power, transistors operating in weak inversion have to be used. A current SAR ADC is proposed to reduce the power consumption. In this thesis, the input of the pacemaker is filtered and converted to current. The total simulated power consummation is approximately reduced by 50% when compared with the state of the art designs. In addition, because of the current DAC, the size of the pacemaker is smaller than other designs which implement a voltage DAC.

1.3 Thesis Outlines

In this thesis, Chapter 2 introduces the system level design and architecture. A literature review of the state of the art design is presented. Design methodology of the filter and ADC is explained in details. Matlab simulations are performed to show the advantages and disadvantages of the different system level design.

In chapter 3, a bandpass filter circuit is designed. Different topologies are discussed in great details. Noise and power are optimized to get the required performance. Several challenges like leakage and non linearity are presented and solved.

In chapter 4, voltage to current converter is designed using Gm-cell. The output current of the gm is chosen careful to minimized the power. The linearity of the gm is discussed. Different linearization techniques are explained briefly

with necessary simulations.

In chapter 5, the system and circuit design of the ADC is presented. Each block is discussed with all the different design challenges and trade off. Current mirror is presented in great details since it is essential element in the current SAR_ADC. Statics and dynamics performance are presented by simulation results with Monte Carlo and process corner.

In chapter 6, the whole system is connected to each other and simulated. Monte Carlo and process Conner simulations is performed to test the robustness of the overall system. Comparison between the recent state of the art design is presented.

In chapter 7, a summery of the thesis with future recommendations are introduced. Also, the design contributions are listed as points.

2 System Architecture & Design

In this chapter, an over view about the previous works is introduced. literature review about low pass filter and different type of ADC's is explained. Design methodology of the low pass filter and ADC's is explained in details. The system level design of this work is introduced with details about the system parameters. Matlab simulations of the ADC is introduced to verify the system level design performance.

2.1 literature Review

In order to construct a bio-signal interface for wearable or implanted biomedical devices, certain system requirements should be meet. Most of the advance system required the output to be digitized for more sufficient processing. The input signal should go through very low frequency pass filter to relax the requirements on the ADC. The main requirements of the ADC is to consume little power to facilitate its integration with low-power digital circuitry.

2.1.1 Very low Frequency pass Filter

A significant amount of research has been dedicated seeking ways to have very low frequency pass filter. The most conventional way to desing a very low frequency pass filter (50mHz~100Hz) is to have RC filter with large capacitor or large resistor which is not practical in low power low noise IC design. Large R and C consumes large amount of power and produc a lot of noise.

Another solution is to implement a Gm-C Filter. As state in the literature, two stage Gm cell are needed to implement a bandpass filter as shown in the Fig. 8 [13].

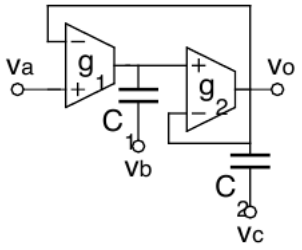

Figure 8: Gm-C Bandpass Filter

In Fig. 8, two active Gm-C stages has two poles to implement bandpass filter. The low cut off frequency and quality factor are calculated by Equ. 6,7 respectively.

$$\mathbf{Wo} = \sqrt{\frac{\mathbf{g_1 g_2}}{C_1 C_2}} \tag{6}$$

$$\mathbf{Q} = \sqrt{\frac{\mathbf{g_1}}{\mathbf{g_2}}}\frac{\mathbf{C2}}{\mathbf{C1}} \tag{7}$$

W_o and Q can be controlled the ration of C2,C1 and g1,g2. However, there are several drawback to the two stage design:

1-Complexity.

2-Higher power.

3-Lower DR.

4-Typical tolerances for both C and gm are in the range of +30%.

Finally, MOS connected diodes in parallel with capacitor could be used in the feedback of an amplifier as shown in Fig. 9[14]. More elaborate explanation will be in Chapter 3.

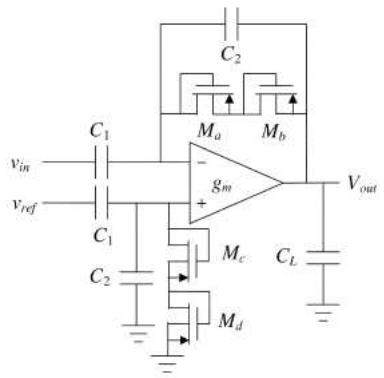

Figure 9: Very low Frequency Bandpass Filter using MOS connected Diodes.

2.1.2 Data Converters

In order to choose the desire type of the analog to digital converter, different types of ADC's have been studied. ADCs can be divided into nyquist-rate sampling and over-sampling converters. For example, Sigma-delta ADCs are used for high bit resolution and demand high clock frequency to over-sample the input signal. The over-sampling ADC consumes large power and requires complex circuitry. Therefore, Sigma-delta is eliminated for this work's requirements. Nyquist-rate ADC converters can be divided into three categories:

(1) Flash

(2) Pipeline

(3) Successive-Approximation

1-Flash ADC uses a voltage ladder with a comparator. At each step of the ladder, the input voltage is compare with a reference voltages. The ladders are implemented by resistors or capacitor. The output of comparators is fed into a digital encoder as shown in the Fig 10. For each additional bit, twice the amount of comparators are needed. Therefore, the power consumption is higher.

As a result, Flash ADC is usually used for low bit resolution and high-frequency applications.

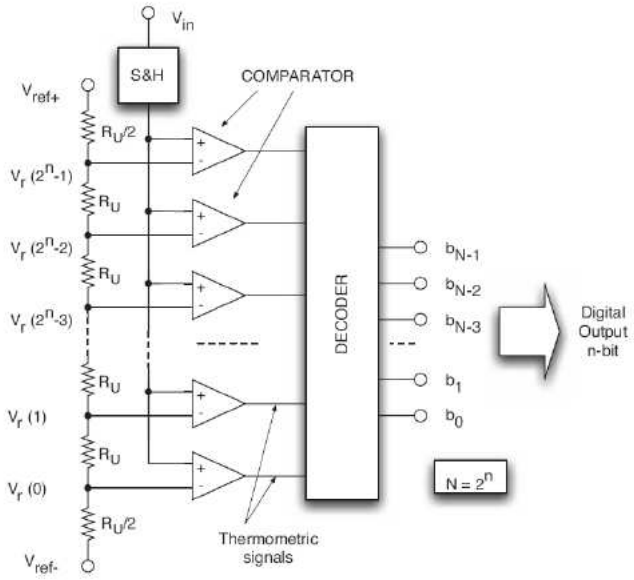

Figure 10: Flash ADC

2-Pipeline ADC uses two or more steps of subranging ADC. First, it performs a coarse quantization of the input. Second, it calculates the residue of the first step using DAC and subtractor. Third, it performs a fine quantization on the residue and adds it digitally to the output as shown in the Fig. 11. For each additional bit, one comparator is needed. Therefore, the power consumption would be higher. The power consumption of pipeline is less than Flash ADC. However, pipeline ADC require more design time than Flash ADC. As a result, Pipeline ADC usually used for high bit resolution and high frequency.

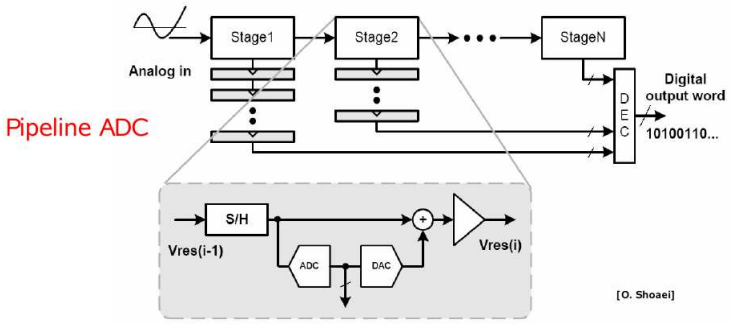

Figure 11: Pipeline ADC

3-Successive Approximation (SAR) performs the conversion over multiple clock periods by exploiting the knowledge of previous bits to compute the next bit. The method aims to reduce the circuit complexity and power consumption using a low conversion rate by allowing one clock period per bit (plus one for the input sampling). The sampled input compared with half of the full scale. Then throughout the clock periods, the next sampled is compared with the output of the DAC. The algorithm is controlled by Logic circuit as shown in Fig. 12[15].

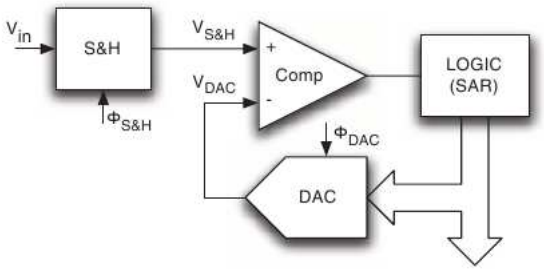

Figure 12: SAR_ADC

SNDR versus sampling frequency is plotted for different ADCs to know the

trade off as shown in Fig. 13 [16].

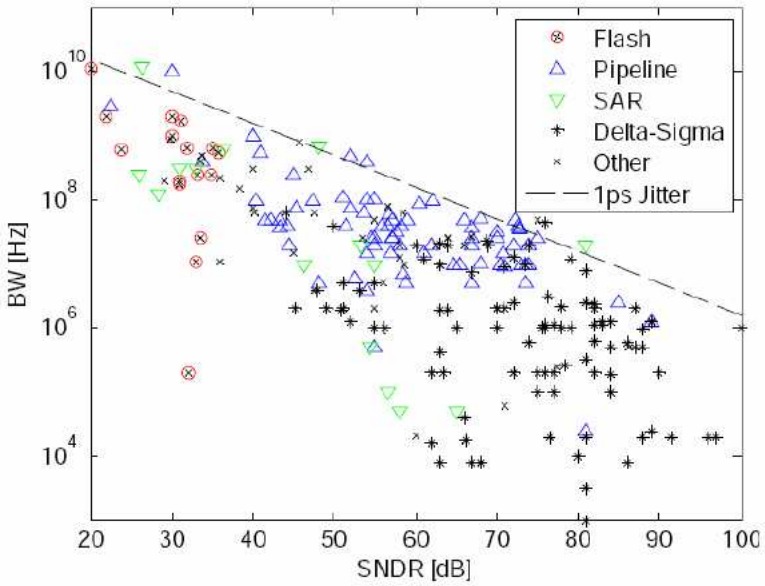

Figure 13: SNDR versus Sampling Frequency for different ADCs [16]

2.2 System Design and Architecture

Different filter implementations are discussed in this section. Also, different ADC's is explained to meet the requirements of the system. Advantages and disadvantages of two systems designs are discussed as well.

2.2.1 Filter Design Methodology

The value of R or C in RC low pass filter should be very big to filter such low frequency(50mHz~100Hz) according to Equ. 9,8.

$$\frac{Output\,(Filter)}{Input\,(Filter)} = \frac{1}{1+s\tau} \tag{8}$$

$$\mathbf{f_{low}} = \frac{\mathbf{1}}{\mathbf{2\pi RC}} \tag{9}$$

For low power low noise, R can not be very big because it would introduce a lot of noise. Also, C can not very big because it consumes a large ship area. For example, to filter an ECG signal, the value of the C would be around 3.2nF with R=1G or 318GΩ with C=10pF which are not practical in IC.

To solve this problem, the resistance or capacitance should be larger without enlarging the actual value of R or C. There are several methods to amplified capacitance or resistance. First, the gm of the Gm-C cell could be used instead of the R in the RC filter as in Equ. 11,10.

$$\tau = \frac{C}{g_m} \tag{10}$$

$$f_{3dB} = gm/2\pi C \tag{11}$$

gm could be control by the input current. However, as stated in 1.1.1, two Gm-C filter stages are needed to implement bandpass filter[13].

In[17][18], CMOS triode transconductor could produce gm down to hundreds of pA/V. Such transconductor could be used in gm-C filters with cut-off frequencies in the range of Hz and sub-Hz. The gm value is controlled by a transistor size and Vds. However, for the application of the design, filter proposed has relatively a large chip area, high noise, poor THD comparing to other techniques[19].

Second, the filter could be implemented by R, MOS Pseudoresistor elements[14], and a capacitor. In [20, 21], the value of the capacitance is amplified by Miller integrator as shown in Fig. 14[20].

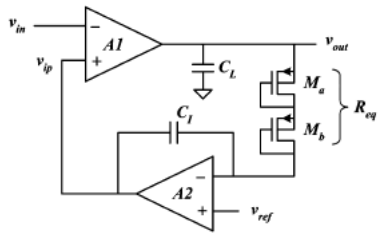

Figure 14: Bandpass Filter Implementing a Miller integrator

The Miller integrator is placed within its feedback path where A_2 provides a voltage gain . The active Miller integrator is made from a second amplifier. However, it suffers from input signal variations,non linearity. Also, two active elements are needed to implement the filter which increase the power consumption.

Harrison implements low-noise low-power single-ended operational transconductance amplifier (OTA) with capacitive feedback[14]. The low cut off frequency is calculated by Equ. 12 [14].

$$f_{low} = \frac{1}{2\pi CR - Pseudoresistor} \tag{12}$$

The key point to have a large R-Pseudoresistor is control gate voltage of the CMOS connected diode.

However, the MOS- bipolar resistance in [14] is highly dependent on the output signal level, which results in distortion and low-cutoff frequency variations.

Olsson et al . implemented MOS-bipolar pseudo-resistor by controlling the gate of NMOS pair in weak inversion.[22]. Horiuchi et al. reported gate controlled nFET biased in weak inversion[23]. Parthasarathy et al. presented PMOS connected diode and using the input capacitance of the OTA as the C in the RC low pass filter[21]. In the case of large signals, distortion will oc-

cur due to the degradation of the low frequency gain caused by the decrease of the pseudo-resistor. Mohseni et al. used gate voltage controlled NMOS pseudo-resistors with resistive feedback[24]. Resistive feedback is implemented by trimming laser resistor which is programmed only once. Also the resistive feedback could increase size and power consumption. Ming et al and Wise et al used voltage controlled PMOS NMOS with external circuit[25][26]. In conclusion, implementing a conventional RC filter is not practical and Gm-C cell suffers from low DR and high power . consumption. The Miller integrator suffers from input signal variations, non linearity. Implementing a low pass filter for ECG signal using Pseudoresistor is most suitable for this design.

Full details about the differences in implementing Pseudoresistor and the filter design will be discussed in Chapter 3.

2.2.2 ADC Design Methodology

ADC consumes the largest power in the pacemaker. The ADC required for ECG signal is 8 bit with 1Ks/s[27]. Comparing the different types of ADC in 2.1.2, Successive-approximation ADC consume the lowest amount of power because it does not have Operational Amplifier. Although, it is a low speed ADC, but it satisfied the ECG requirements. Most of the biomedical signals do not require more than 10 bit ADC. As a result, successive-approximation ADCs has recently become very attractive in energy- efficient moderate-resolution/moderate-speed applications[28, 29, 30, 19, 31, 32, 33]. In order to minimize the power as mush as possible, Current Mode Successive Approximation ADC is presented. The idea of current mode ADC is first introduced by Salama [34]. Current SAR_ADC is used for the fallowing reasons. First, the power consumption is proportional to the full scale current input. A full details analysis of the relationship are discuss in Chapter 5 [35]. Second, the chip area is much less since, no capacitor in sued in the DAC[34]. Current DAC using current sources

would be used. Although, there is constant power dissipation because of the use of constant current sources[36]. However, in weak inversion, the current is very small (nonocurrent) and if the full scale input current is chosen carefully, this effect is minimized.

In the literature, there are two Current Successive Approximation ADC proposed[37, 35]. The current DAC in the Current Successive Approximation ADC could be scaled down easily with technology. Chao et al used an Op-amp in his design which increases the power consumption. In general, there were not enough information or circuit performance in the proposed circuit. Iniewski el al.design consumes one of the lowest power, 560nW, reported in the literature. However, the design suffers from biasing problems in the current mirror which leads to less accuracy especially with very small reference current value. Also, there are numbers of redundant current mirror which can be eliminated to reduce the power and the error. A details analysis of the power consumption ,biasing and the proposed Current SAR is discuss in Chapter 5.

2.2.3 System Architecture

The goal is to design an implanted biomedical devices which filter the signal then digitized it using SAR ADC. In the literature, there are two system which consist of very low frequency pass filter fallowed by Voltage Successive Approximation ADC[19, 33]. The system proposed in this work consist mainly of a bandpass filter fallowed by gm cell to convert the voltage to current then Current SAR_ADC as shown in Fig. 15

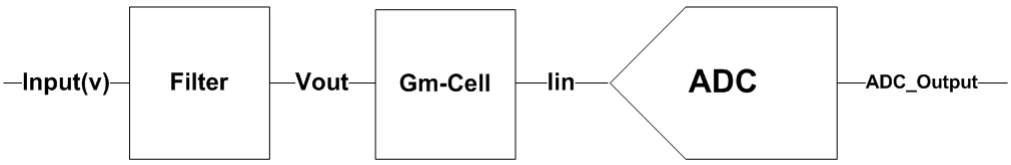

Figure 15: Overall System Architecture

There are two possibility of the proposed system. First, low pass filter fallowed by linearized operational transconductance amplifier fallowed by Current SAR as show in Fig. 16.

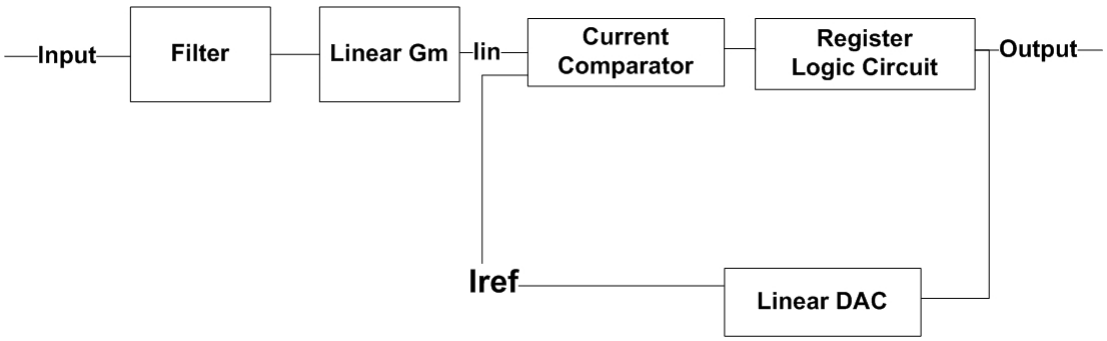

Figure 16: Overall System Architecture with linear DAC

Second, bandpass filter fallowed by operational transconductance amplifier without linearization. To solve the non-linearity of the Gm-cell ,non linear tangent hyperbolic current steering DAC inside the Current SAR_ADC is designed as illustrated in the Fig. 17.

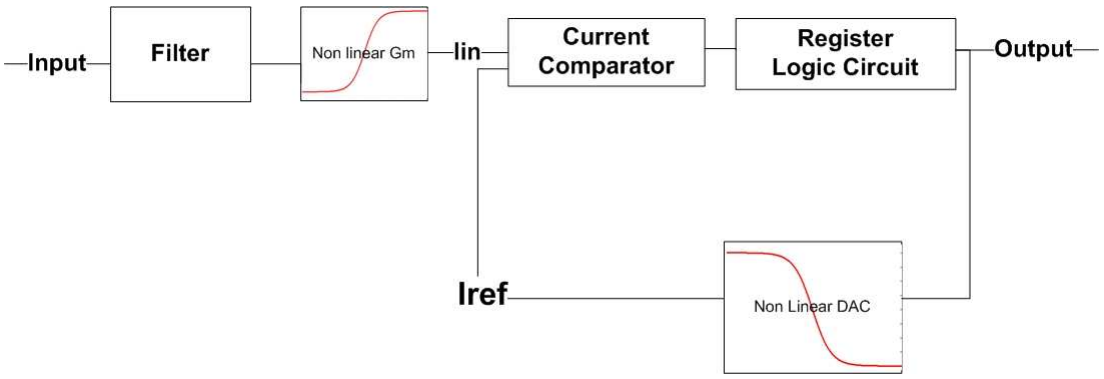

Figure 17: Overall System Architecture with linear Non linear DAC

Matlab simulations of the ADC is perform in sec. 2.3 to show the differences and potentials between the two systems.

2.3 ADC-Matlab Simulation

A more elaborate explanation of the functionality of the conventional SAR ADC in presented in this section using Matlab simulations. Each block of the ADC is modeled by Matlab code. The code could be used for different resolutions and sampling rate. The SAR algorithm could be changed as well. The comparator is modeled as a subtractor. The input of the comparator is the actual output of the Gm block from CADANCE. The quantization level of the DAC are modeled by Equ. 13.

$$Ideal\,Quantization\,Level = \frac{2^{j-1}}{2^{nbit+1}} \tag{13}$$

$$j = 1 : nbit \tag{14}$$

Where nbit is the number of bit. j is an incremental number. j presents the number of thresholds. A mismatch in the capacitor or transistors could be introduced by Equ. 15,16.

$$Mismatch = Normalized\,Mismatch\,Percentage.Randn \tag{15}$$

$$Quantization\,Level - Mismatch = \frac{\left[2^{j-1} + (Mismatch.2^{j-1})\right]}{2^{nbit+1}} \tag{16}$$

Since the nature of mismatch is random, randn, a Matlab code, returning a pseudorandom, is introduced in Equ. 15. The SAR logic modeled by separate Matlab codes. Input value is compared with the reference value from the DAC. Linear and non linear offset could be introduced in the comparator. SQNR is calculated without windowing as mentioned in Appendix A.

The first testing is performed with ideal conditions. There is no mismatch in the DAC or offset in the comparator. In order to make sure that the MATLAB

model is functioning according to the theory, a DC signal of 0.7V with 8 bit resolution is tested as shown in Fig. 18. In theory, 0.7 V is compared with 0.5 V, the difference is greater than 0 , then 0.25 is added to 0.5 V, then the difference between 0.7 and 0.75(0.5+0.25) is less than 0, then 0.125 is subtracted from 0.75,then the difference between 0.7 and 0.625(0.75-0.125)is greater than 0. The same algorithm is performed through out the 8 cycles.

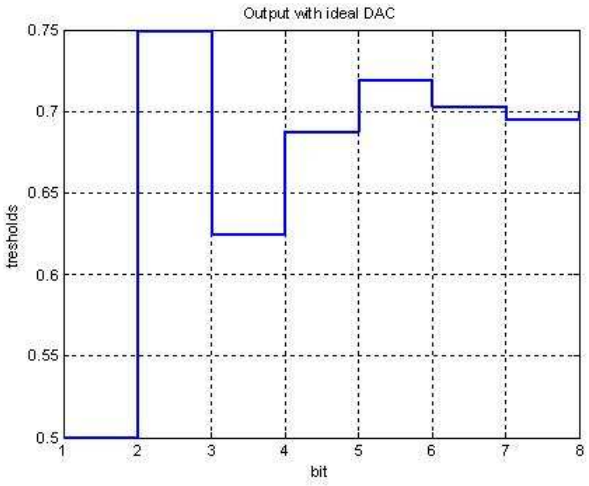

Figure 18: Output of SAR ADC with 0.7V DC input and 8 bit resolution

The output of the simulation agrees with the theory as mentioned. The final value is 0.69922 V which is very close to 0.7 V. To make sure that the system is working, different values of DC signal with different number of bit are applied to ADC as shown in Fig.19,20.

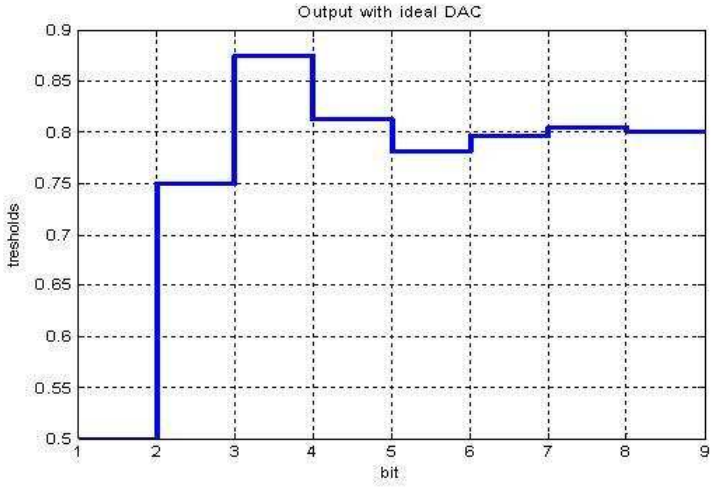

Figure 19: Output of SAR ADC with DC of 0.8 V and 9 bit resolution

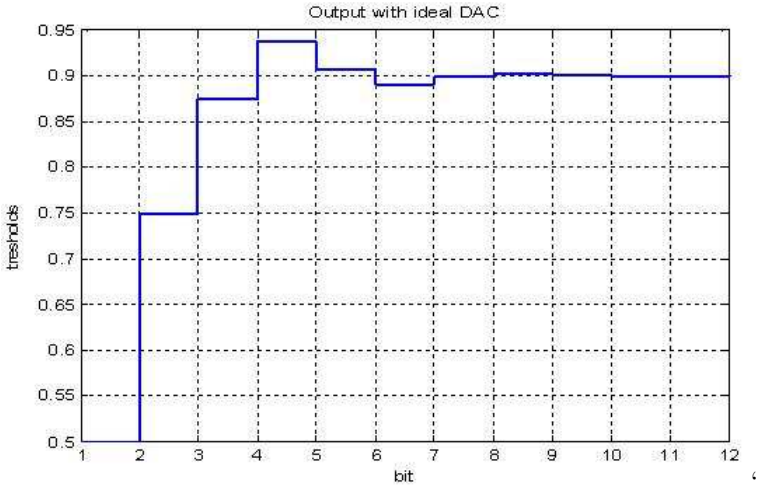

Figure 20: Output of SAR ADC with DC of 0.9 V and 12 bit resolution

The output of both simulations agrees with the theory. The same method of calculating of 0.7V 8 bit is applied to the plots above. Therefore, the MATLAB model is functioning correctly according to the theory.

2.3.1 Linear Current Steering DAC

linear and non linear DAC are tested with actual output of the gm-cell without any linearization techniques. The two system perform an 8 bits ADC without mismatch in the current sources. Then, the simultions are performed with mismatch. The quantization noise and SNR are calculated in all the different conditions. For 8 bit linear DAC the quantization levels is describes in Equ. 17:

$$X_Q = 2^{-n} n = 1..8 \tag{17}$$

Where n is the number of bit. The quantization levels in the current DAC are(1,2,4,8,16,32,64 and128). Ideally the maximum value of the quantization noise is calculated by Equ. 18:

$$\frac{1}{2} LSB = \frac{I_{Full\,Scale}/2^{N-1}}{2} \tag{18}$$

For 8 bit ADC, 0.5 LSB=0.003906. Also, The ideal SQNR is calculated by Equ. 19:

$$SQNR = [(N * 6.02) + 1.78]\, dB \tag{19}$$

For 8 bit ADC, The ideal SQNR=49.92dB.

The output of the linear DAC and the Quantization noise is shown in Fig. 21,23.

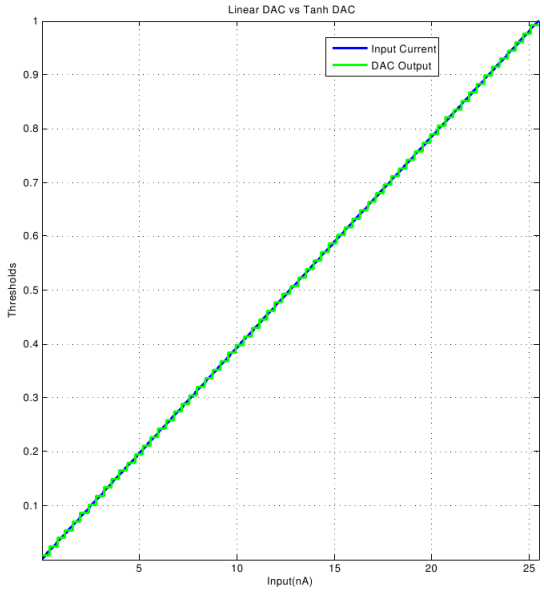

Figure 21: Input current vs Thresholds of Linear DAC

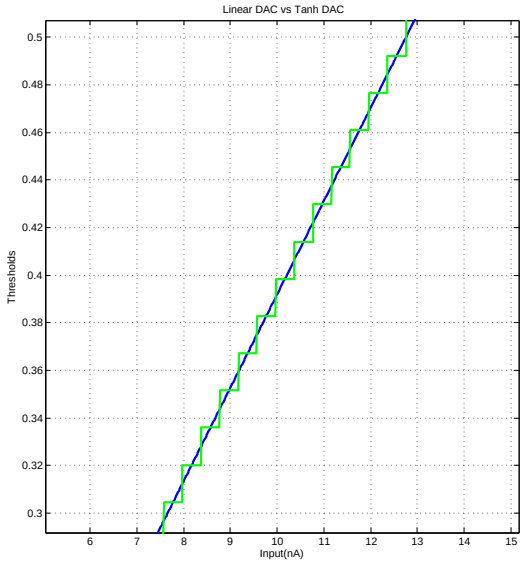

Figure 22: Input current vs Thresholds of Linear DAC_Zoom

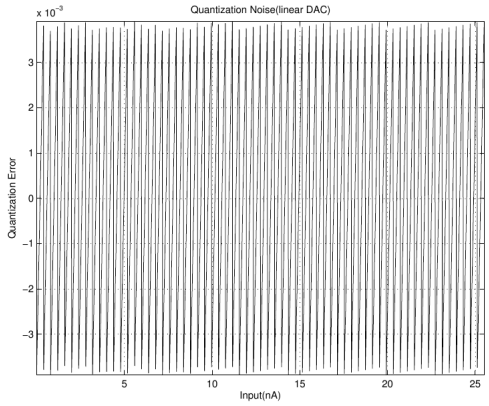

Figure 23: Input current vs Quantization error of Linear DAC

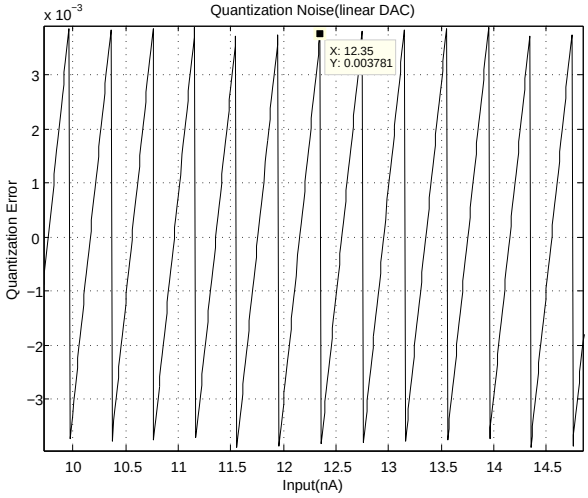

Figure 24: Input current vs Quantization error of Linear DAC_zoom

From Fig. 21, the output of the DAC is fallowing the input. The $\frac{1}{2}$ LSB 0.00385 which is very equal to theoretical 0.003906. The SQNR was measured with sine wave input to be 49.8dB which is very close to the theoretical, 49.92 dB.

2.3.2 Non linear Tangent Hyperbolic Current Steering DAC

The DAC implements Tangent Hyperbolic because the nature of the non linearity of the gm-cell is Tangent Hyperbolic. The quantization levels in the non-linearity current DAC are [1,2.26,4.1,7.95,16.211,31.8,63.8,127.9]. The output of the linear DAC and the Quantization noise are shown in Fig. 25,27. The non linearity could not be shown easily only if is compared with linear input with linear DAC.

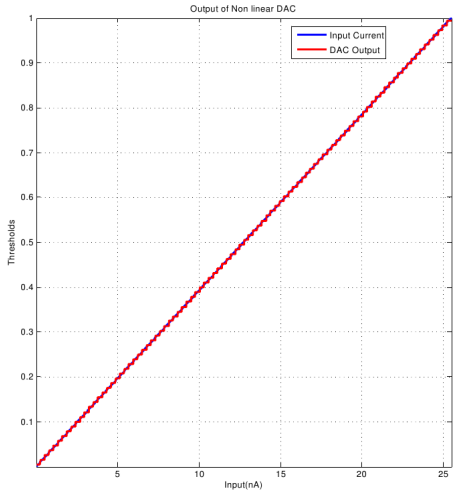

Figure 25: Input current vs Thresholds of Non Linear DAC

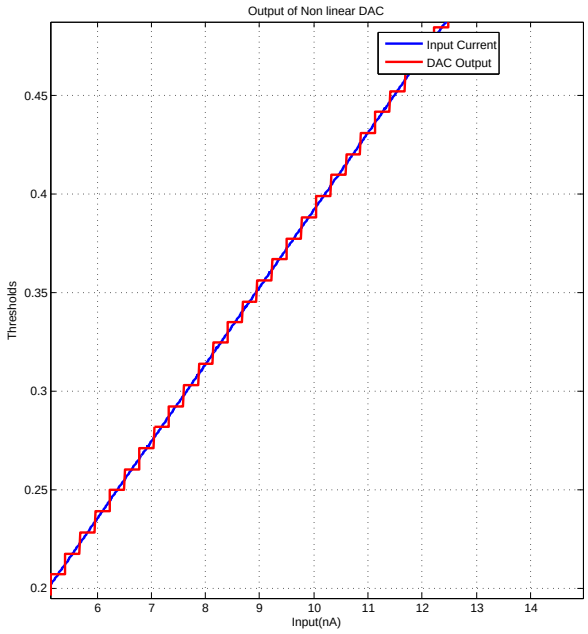

Figure 26: Input current vs Thresholds of Non Linear DAC_zoom

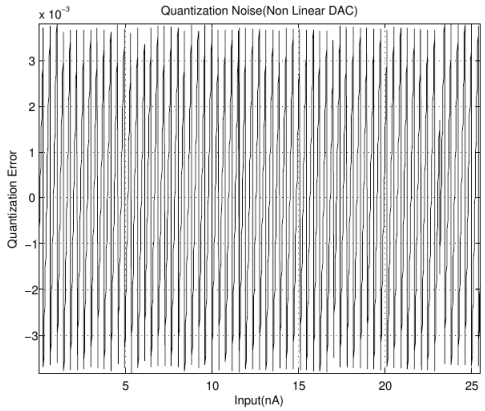

Figure 27: Input current vs Quantization error of Non Linear DAC

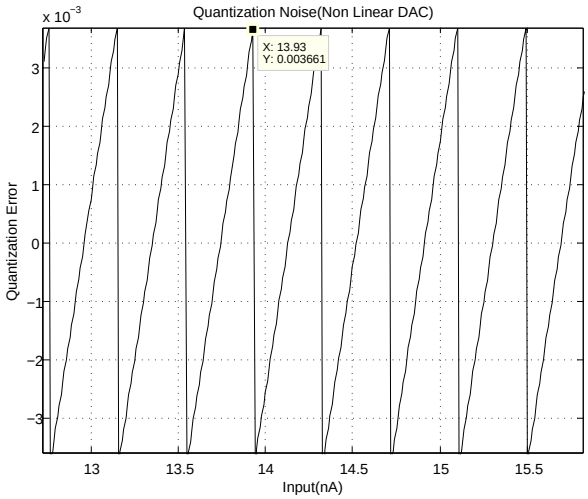

Figure 28: Input current vs Quantization error of Non Linear DAC_zoom

From Fig. 27, the output of the DAC is fallowing the input. The $\frac{1}{2}$ LSB 0.00375 which is less than the theoretical value. The SNR was measured with sine wave input to be 50.5 dB which is higher than the theoretical value. As a result, the non linear DAC has lower quantization noise and higher SQNR. The the non linear DAC fallows the sine wave more accurately than the linear DAC. To have a fair judgment, a triangular wave form is tested in both systems. The linear DAC has higher SQNR and lower quantization noise than the non linear DAC .The linear DAC fallows the triangle wave form form more accurately than non linear DAC.

2.3.3 Measuring SQNR with Mismatch

To have more insight about the performance of both systems, different mismatches are applied. The mismatch percentage are taken from the model of IBM 0.13μM. The mismatch is applied by Equ. 15. The mismatches, $\triangle W$, are 0.028 μM (all tolerance are $3\,\sigma$ value), 0.039μM (chip mean value) and 0.05μM (total tolerance). linear and non linear DAC are simulated simultaneously. His-

togram of the 100 runs is plotted to see how may of the runs falls into a certain value of SQNR as shown in Fig. 29,30,31.

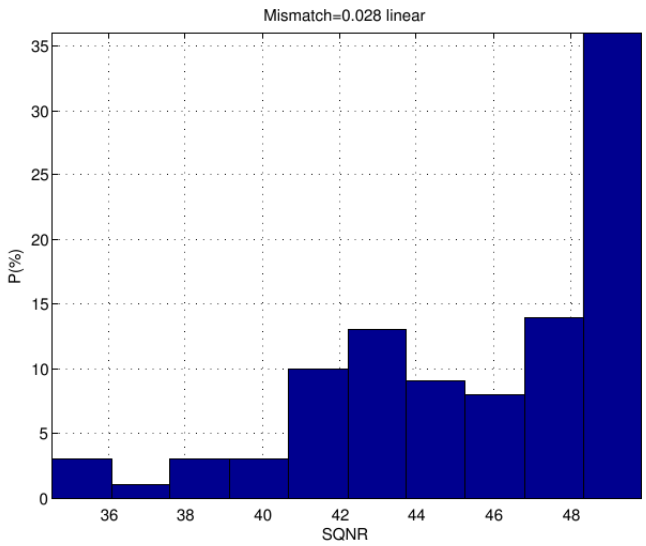

Figure 29: SQNR Histogram of SAR ADC for $0.028\mu M$ mismatch of the linear DAC

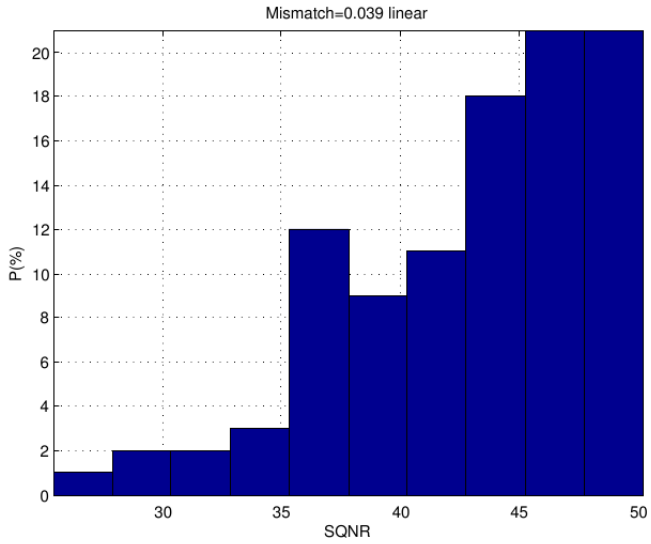

Figure 30: SQNR Histogram of SAR ADC for $0.039\mu M$ mismatch of the linear DAC

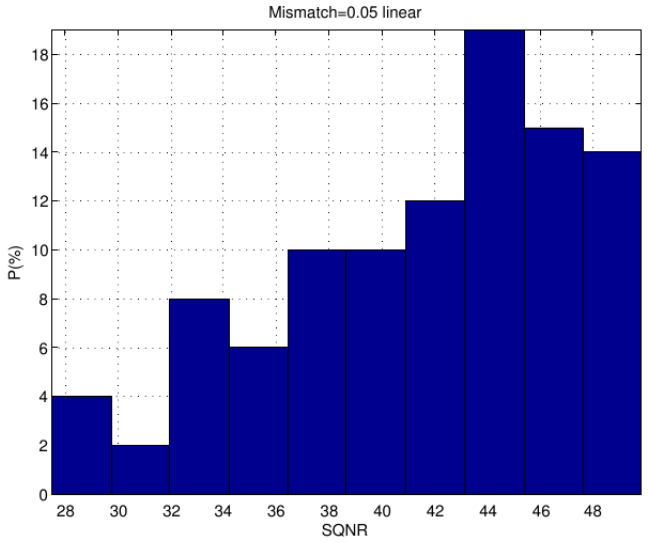

Figure 31: SQNR Histogram of SAR ADC for $0.05\mu M$ mismatch of the linear DAC

The mean values of the SQNR for linear DAC with the different mismatch is presented in Table. 1.

Mismatch(μM)	SQNR(dB)
0.028	45.5
0.039	43
0.05	41.5

Table 1: Compression between simulated SQNR of linear DAC with Mismatch

The value of SQNR is degrading at the mismatched increasing. For non linear DAC, the Histogram plots are show in Fig. 32,33,34.

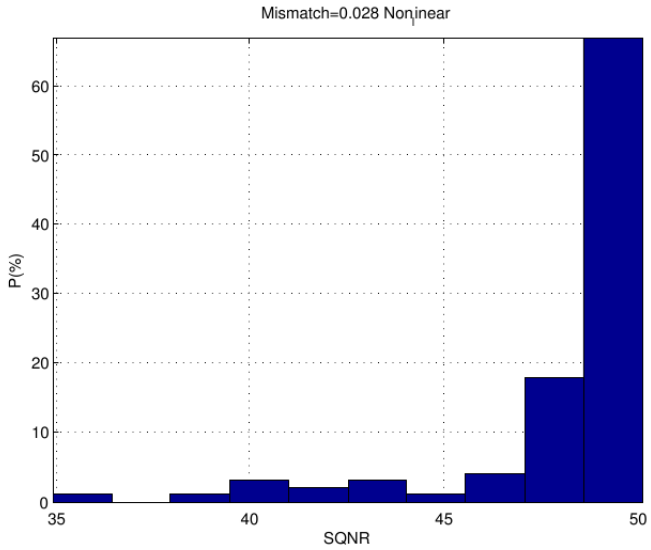

Figure 32: SQNR Histogram of SAR ADC for $0.028\mu M$ mismatch of the Non_linear DAC

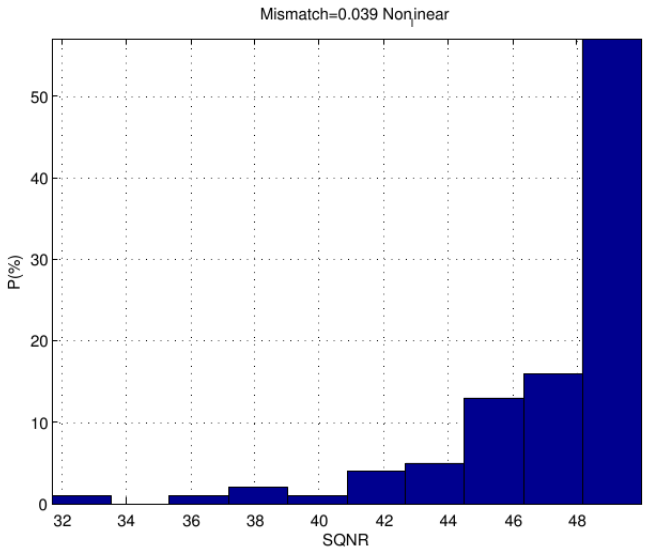

Figure 33: SQNR Histogram of SAR ADC for $0.039\mu M$ mismatch of the Non_non linear DAC

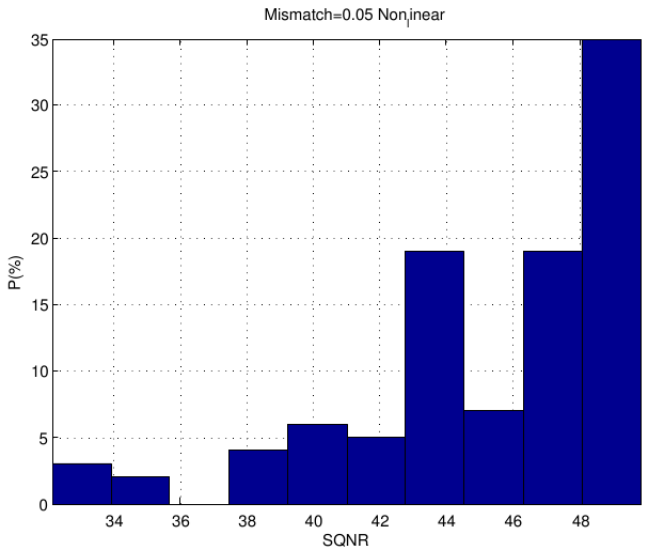

Figure 34: SQNR Histogram of SAR ADC for $0.05\mu M$ mismatch of the non_linear DAC

The mean values of the SQNR for linear DAC with the different mismatch is presented in Table. 2.

Mismatch(μM)	SQNR(dB)
0.028	48.14
0.039	47.26
0.05	45.33

Table 2: Compression between simulate SQNR of Non linear DAC with Mismatch

The value of SQNR is degrading as the mismatched increasing.However, the SQNR of the non linear DAC is higher than linear DAC for the same reasons mentioned in 2.3.2 as shown in Table. 3.

Mismatch(μM)	SQNR(dB)_Non linear	SQNR(dB)_Linear
0.028	48.14	45.5
0.039	47.26	43
0.05	45.33	41.5

Table 3: SQNR Compression between Linear and Non linear DAC

As a result, non linear DAC is implemented in this design because of its performance and ease of implementation of similar non linearity of Gm block.

2.4 Conclusion

The input signal of wearable or implanted biomedical devices should go through very low pass filter implemented by MOS-bipolar pseudo-resistor. The resistance could be controlled in different way as mention in sec. 2.2.1. In this work, the bandpass filter used a Pseudoresistor. The voltage output of the filter is converted to current by gm-cell. To have the lowest power possible, current SAR_ADC is proposed. More details about the linearity of the gm is Chapter 4.

3 Low Pass Filter Circuit Design (First Stage)

In this chapter, the characteristics of the very low frequency filter is explained with all the design challenges. The circuit design of the filter and the OTA are introduced with the necessary simulations using CADANCE. Noise and power analysis and optimization are discussed as well.

3.1 Very Low Frequency filter & Sub-threshold Two Stage Miller Op Amp

Different filter topology is discussed with different implementations. Comparison between the different implementation is explained in order to meet the requirements of the system. The OTA implementation and characteristics are explained to meet the requirements of the filter. Different challenges such as leakage and noise optimization are discussed. The load calculation is computed to minimize the power consumption.

3.1.1 Bandpass Filter Topology

As decided in Chapter 2, the filter should be implemented by Pseudoresistor as show in Fig. 35[14]. The OTA is a two stage Op Amp with miller capasitor as show in Fig. 40.

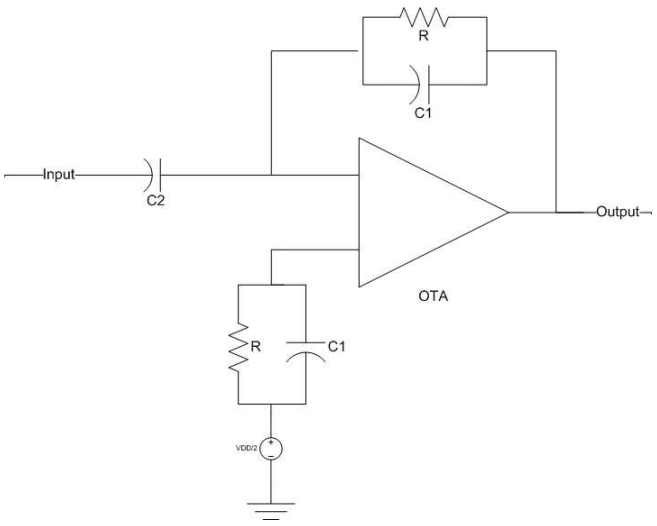

Figure 35: Bandpass Filter Topology

The low cutoff frequnecy of the filter is implemented by Pseudoresistor in parallel with capacitor (C1) in feedback. The same configuration of Pseudoresistor and capacitor is placed in positive input of the filter in order to allow the rejection of expected DC potential differences [23].

The frequency response of the proposed filter is show in Fig. 36.

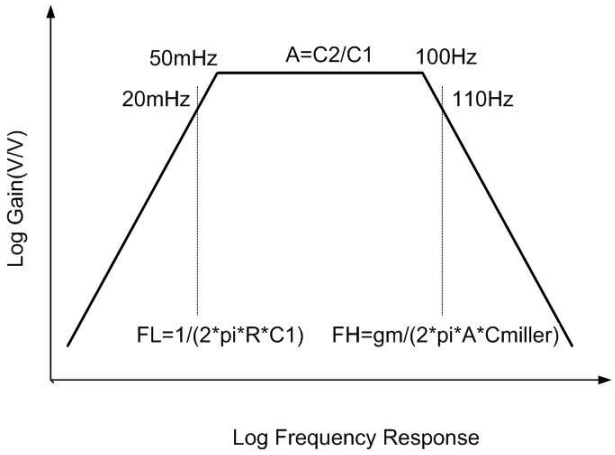

Figure 36: Gain vs Frequency for the Proposed Bandpass Filter

The gain is set to A=20dB. Therefore according to Equ. 20,
C2=30pF,C1=3pF.

$$A(gain) = \frac{C_2}{C_1} \tag{20}$$

A larger value could be choosing to reduce the resistance required from the Pseudoresistor.However, a larger metal-insulator-metal capacitor,mimCap, consumes very large chip area. The reason to choose mimCap is explained in sec. 3.1.3. Therefore, the required resistance of the Pseudoresistor with low frequency cutoff of 20mHz is equal to 2.65TΩ according to Equ. 21. The 20mHz is chosen to have safe margin and to compensate for any variations as stated in[27].

$$f_{low} = \frac{1}{2\pi CR - Pseudoresistor} \tag{21}$$

The high cutoff frequency set to be equal to 110Hz. The 110Hz is chosen to have safe margin and compensate for any variations as stated in[27]. The high cutoff frequency is calculated by Equ. 22

$$f_{high} = \frac{gm_1}{2\,\pi\,A\,C_{miller}} \tag{22}$$

High frequency cut off is function of the Miller Capacitor. In other design[14], $f_{high} = \frac{gm_1}{2\,\pi\,A\,C_{Load}}$ is function of Cload which is varying depending of the load.

3.1.2 MOS_Pseudoresistor Element

MOS_Pseudoresistor operate in deep triode region creating a small-signal resistance around 1TΩ . It does not only reduces the area comparing to an

actual R but also gives the chance for reconfigurable filter.

The MOS_Pseudoresistor is implemented by different methods[22, 38, 21, 25, 20, 23, 14, 33, 26]. As the input changes the resistance changes. In other words, the pole of the filter is changing with the input. The resistance of Pseudoresistor is not linear. However, choosing the gain to be 20dB relaxing the linearity of the resistance as shown in Fig. 37. The magnitude of the ECG input is 5mV with gain of 20dB, the output is 50mV. On the other hand, if the gain is 40dB like most of the designs, the resistance would inter the non linear region which require different effort to linearized the pseudoresistor.

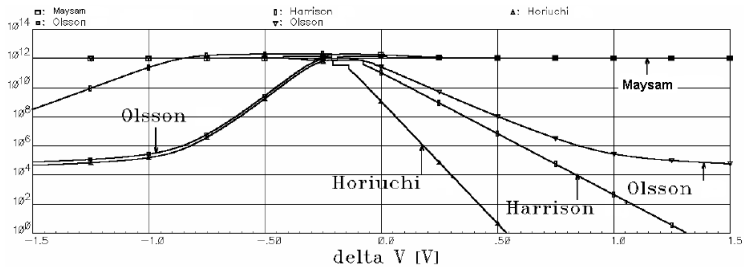

Figure 37: Comparison Between Simulated Resistances of Different MOS Pseudoresistor Designs

Controlling the Gate of the PMOS by voltages source gives the require resistance without any additional circuit technique. Resistance of the PMOS in weak inversion is calculated by [24].

$$rds \backsimeq \frac{L}{n\,C_{ox}\,W\,V_{th}}\,exp(-\frac{Vgs - V_T - n\,V_{th}}{n\,V_{th}}) \tag{23}$$

where n is the sub threshold slope factor,V_T is the transistor threshold voltage,V_{th} is the thermal voltage. To maintain a high input impedance with the same Vtune, PMOS is chosen since hole mobility is one-half to one-fourth

that of the electron[9]. Two PMOS's in series is chosen to reduce distortion for large output signals[14].

Equ. 23 is plotted to know the value the voltage needed to obtain the required resistance (1.32TΩ).

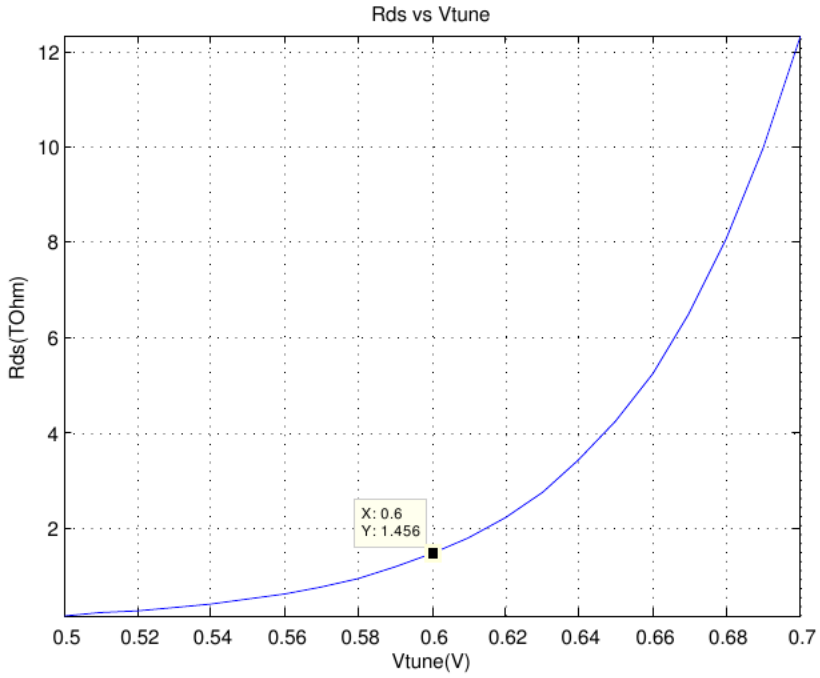

Figure 38: Rds vs Vtune for PMOS Pseudoresistor by Equ.23

As shown in Fig 38, Vtume=0.6V givies a resistance of $1.456T\Omega$ Rds (Pseudoresistor) is chosen to be little bit higher in order to accommodate for any variations. The PMOS Pseudoresistor is simulated to check if the calculated value from Equ. 23 match the value of simulation as show in Fig. 39.

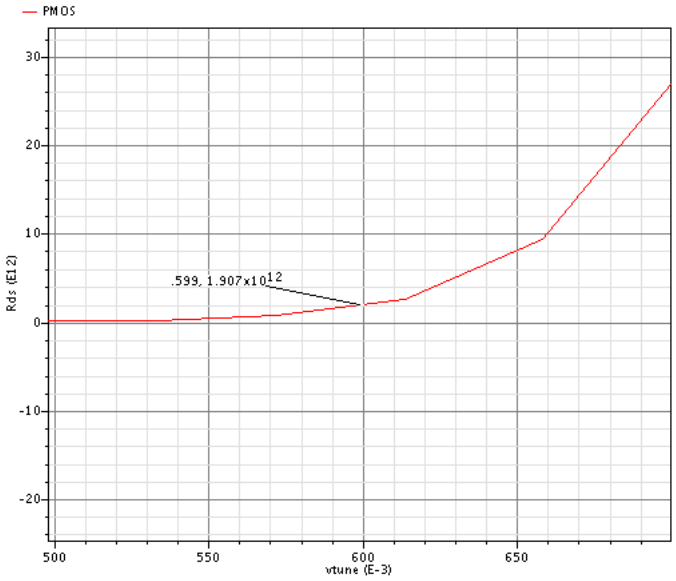

Figure 39: Rds vs Vtune for simulated PMOS Pseudoresistor

As shown in Fig. 39, as the voltage increased Rds increased which correspond to Equ. 23. The simulated value is 1.907TΩ which is relatively close the calculated value 1.456TΩ.

3.1.3 leakage Current(mimCap vs nCap & MOS_Pseudoresistor)

There are two main sources of leakage in the filter design. The gain is set by the ratio of C2/C1. Higher value of capacitor could be implemented by NMOS connected like capacitor, nCap. However, the nCap has high value of leakage current[39]. For C_2, the leakage goes directly into the input stage. For C_1, the leakage goes through feedback into the input stage. The same scenario applied to the capacitor connected to the positive terminal. These leakages change the biasing of some of the transistors and change the biasing voltage at the output. For this design mimCap is used.

Second source if leakage is the gate leakage form MOS_Pseudoresistor in order of 5fA. The leakage current goes through the feedback through the input because of the lower resistance. Then, the leakage current is amplified by second stage. Finally, the leakage comes to the output which will change the biasing voltage which change the frequency response of the filter. To solve this problem, a current buffer in inserted between the input stage and the current mirror to disassociate the voltage nodes. The functionality of the current buffer is explained in sec. 3.2. On the other hand, previous designs[20, 19, 26, 23, 14, 25, 24, 22, 21] have used large technology process which do not suffer from gate leakage.

3.2 OTA in Weak Inversion

In weak inversion saturation ID is independent from Vds and gm is function of ID as in Equ 24,25[10].

$$I_D = \frac{W}{L} I_{DO} \, exp(\frac{qVgs}{nKT}) \tag{24}$$

Where I_D is the drain current, W is width, L is length, I_{DO} is zero-bias current, V_T is thermal voltage, K is $1.38 \, . \, 10^{-23}$J/K (Boltzmann's constant), q is $1.60 \, . \, 10^{-19}$ C (elementary charge), T is temperature, n is sub-threshold slope.

$$gm = \frac{I_D}{nKT/q} \tag{25}$$

The circuit design of the OTA is show in Fig. 40. The OTA consists of two stages. The circuits operates in weak inversion with all the transistor in saturation(Vds>100mV).

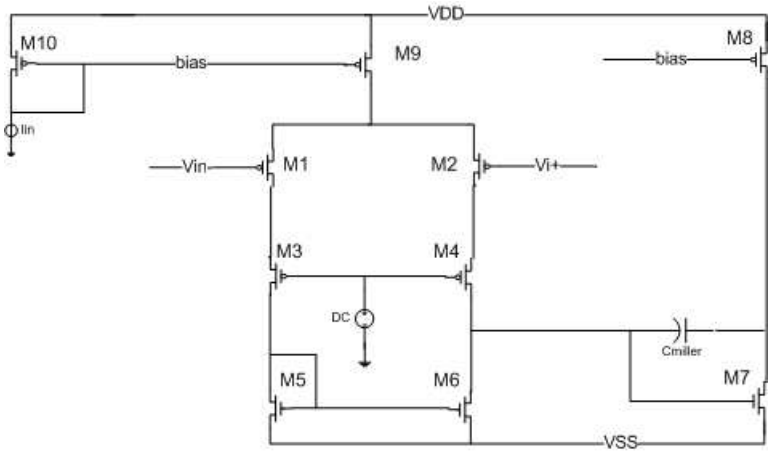

Figure 40: Two Stage Miller Op Amp

PMOS input is chosen because it has lower flicker noise[9, 8]. PMOS has lower flicker noise because the channel is further in distance from the interface which is less affected by interface trap. M3-M4 creates current buffer-cascode which reduce the offset due to leakage and 2nd harmonic distortion. The value of the DC voltage connected to M3 and M4 is 70mV. The miller capacitor,14pF, is used to have more control over the high frequency filter since the gain bandwidth is function of Cmiller according to Equ. 26[40].

$$GB = \frac{I_{D1}}{(nKT/q)C_{Miller}} \tag{26}$$

3.3 Noise Analysis & NEF.

The input referred noise of the whole system depends on the noise of the front-end amplifier. Therefor, analyzing and optimizing the noise of the filter is very essential to reduce the noise of the overall system. Generally, having

Av=10=20dB, input-reference noise of the whole system could be roughly estimated by Equ. 27.

$$\textbf{Input reference noise power} = \textbf{Power Noise}_{\textbf{Filter}} + \frac{\textbf{Power Noise}_{\textbf{gm}}}{\textbf{Av}^{\textbf{2}}} + \frac{\textbf{Power Noise}_{\textbf{ADC}}}{\textbf{gm}^{\textbf{2}}\,\textbf{Av}^{\textbf{2}}} \tag{27}$$

Where gm is the gm of the Gm block and Av is the gain. Setting Av(gain)=10, the second and third terms could be eliminated. Therefore, the input-reference noise is dominating by noise of the filter. The input referred thermal noise of the filter is given by Equ.28. The noise is simplified to be function of ID.

$$Vin = \sqrt{\frac{8K\,I_D\,(nKT/q)^2}{I_D^2}} \tag{28}$$

The current noise has to be taken into account as well. The higher the value of the input Capacitor(C2) the lower the current noise at the input. Equ. 28 is plotted to know the optimum point of current operation. As shown in Fig. 41, as the current increases, the noise decreases. However, the filter should be power limited. Choosing the power consumpation to be around 100nW and , gives a noise value around $5.854\mu V$.

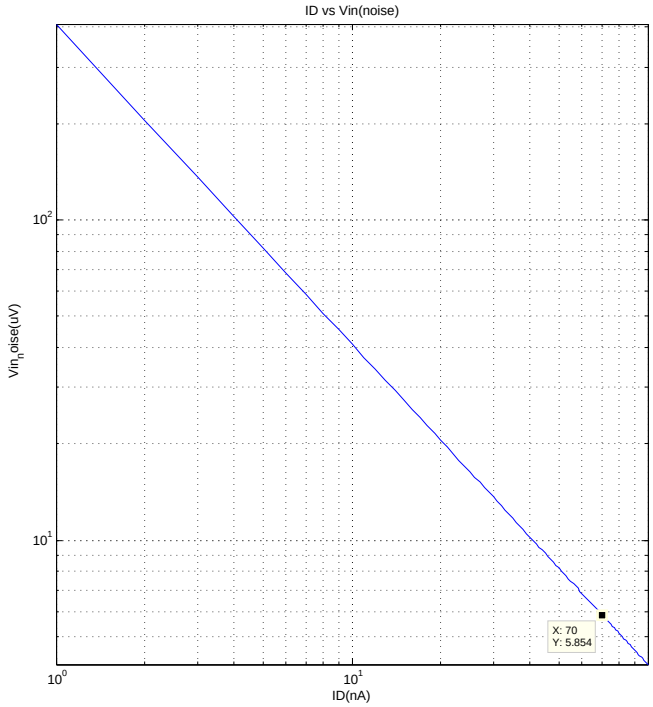

Figure 41: I_D vs Input Voltage Noise of the Bandpass Filter from Equ. 28

Since the flicker noise is the dominate source of noise, Noise Efficiency Factor (NEF) is needed. NEF takes into account diffrent factor like BW and total current. The noise efficiency factor (NEF) is first introduced in[41].

$$NEF = V_{ni,rms}\sqrt{\frac{2\,Itot}{\pi\,V_{th}\,4KT\,BW}} \tag{29}$$

where Vni,rms is the input-referred rms noise voltage, Itot is the total amplifier supply current, and BW is the amplifier bandwidth in hertz. Ideally, NEF is equal to 1. However, in weak inversion more accurate model for shot noise is taken into account. The NEF is calculated by Equ. 30 [8].

$$NEF = \sqrt{\frac{4}{k}} \backsimeq 2.9 \tag{30}$$

Where I total=2 ID, κ, gate coupling coefficient, is typically equal to 0.7 . NEF=2.9 is the theoretical NEF limit for an amplifier, assuming current

mirror ratios of unity. The noise bandwidth is very critical to determine the NEF. The input-reference noise could drastically decreases if the QRS bandwidth(50m~30Hz) is only filtered as in [19]. The input refer noise of this design is calculated differently than other designs. The output square noise voltage is divided by the square bandpass gain. Then, the result of division is integrated over bandwidth,50mHz~100Hz. The noise is calculated by Equ. 31.

$$Noise = \int (\frac{V_{Noise-Out}}{Av})^2 \tag{31}$$

Where Av is the Bandpass gain. Noise of this design is 5.4 μV and NEF=3.33 which is close to the theoretical limit 2.9.

3.4 Load Calculation

Calculating the require output current of the filter minimized the power consumption. Also, there should be enough current to drive the load (gm-Cell). In addition, having gm-cell after the amplifier would have lower Cload than ADC immediately after the filter. The filter characteristics is derived to calculate the require output current as in Equ. 32,33,34.

$$\frac{\text{Vo}}{\text{Vin}} = \frac{R\,\frac{1}{C_2 S}}{\frac{R+\frac{1}{C_2 S}}{\frac{1}{C_1 S}}} = -\frac{\frac{R}{1+SRC_2}}{\frac{1}{C_1 S}} \tag{32}$$

$$|A(j\omega)| = \frac{RC_1\omega}{\sqrt{1+\omega^2 R^2 C_2^2}} \tag{33}$$

$$\textbf{Iout} = \frac{\text{V}_{\text{biasing}}\,(1+\omega\,\text{R}\,\text{C}_2)}{R} \tag{34}$$

W=100Hz,R=2.65TΩ,C=3pF and Vbiasing=0.5V $\Longrightarrow$Iout=0.3nA. However, Iout is chosen to be little bit higher to make sure that the load would have

sufficient current. M5 and M6, in Fig, 40, is optimized to deliver the required Iout to reduce the power consumption.

3.5 Simulation Results

The sizing of the transistors is critical for achieving low noise,low power as mentioned before. The temperature is set to 37.0C, temperature of the human Body. The filter operates in weak inversion. The process technology used is $0.13\mu m$. The circuits is shown below in Fig. 42.

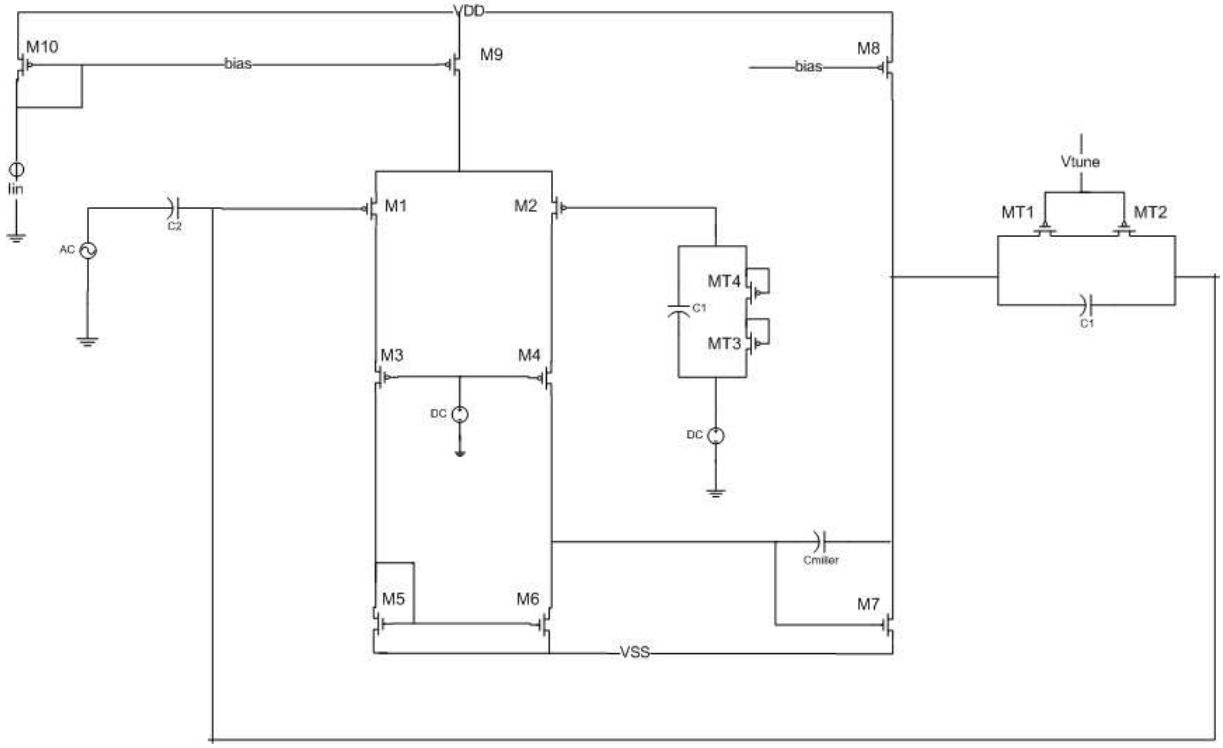

Figure 42: Bandpass Filter Circuit Design

The sizes of the transistors are giving below in Table. 7.

Devices	M_1,M_2, M_3, M_4	M_5,M_6	M_7	M_8	M_9,M_{10}	M_{11},M_{12}	M_{13}	M_{14}
W/L(μM)	25/20	20/20	1/10	3/10	0.31/20	100/0.12	13/3	6/3

Table 4: Devices Sizes

The frequency response, input referred thermal noise calculated by Equ. 31 and transient analysis at 2.5mV are simulated as shown in Fig. 43,44,45. From the simulations results, BW is 20m~111Hz and DC gain of 19.51dB. The noise which is simulated from 50mHz to 100Hz equals to $5.4\mu V$. The THD is 0.5%. The performance of the filter is in Table. 5. Also, a comparison between the different work is in Table. 12.

Parameter	Simulation
V_{DD}	1V
I_{Supply}	30n
Gain	19.51dB
BW	20m~111Hz
THD@ 2.5mV &2.23Hz*	-46.02dB (0.5%)
Input referred noise(50mH-100Hz)	$5.39\mu V$
NEF	3.3
Power Consumption	108nW

*Geometric mean of the BW.

Table 5: Simulated Performances of the Bandpass Filter

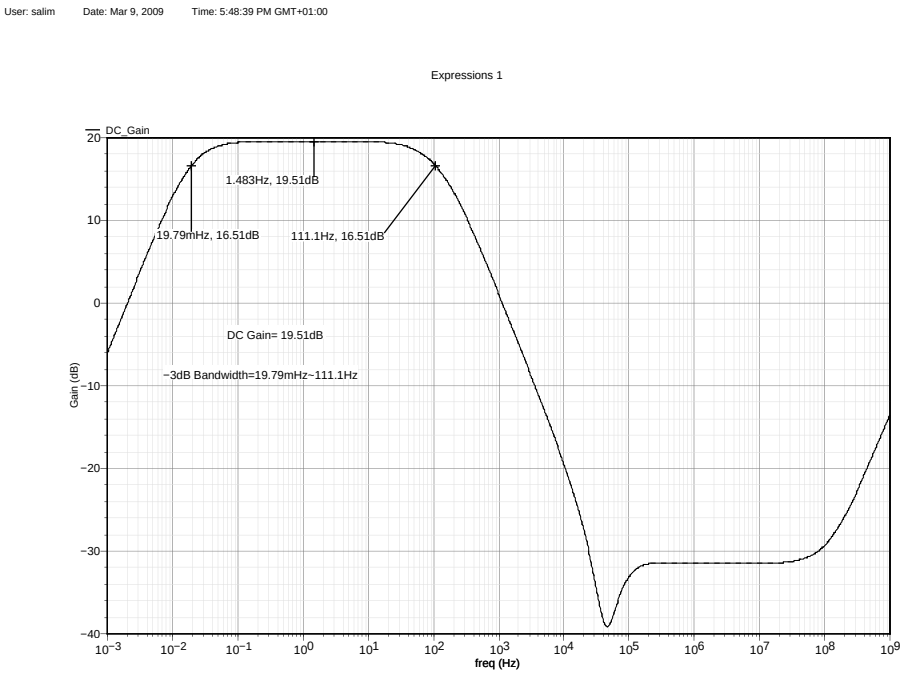

Figure 43: Frequency Response of Bandpass Filter

The noise in Fig. 44, is simulated from 50mH to 100Hz.

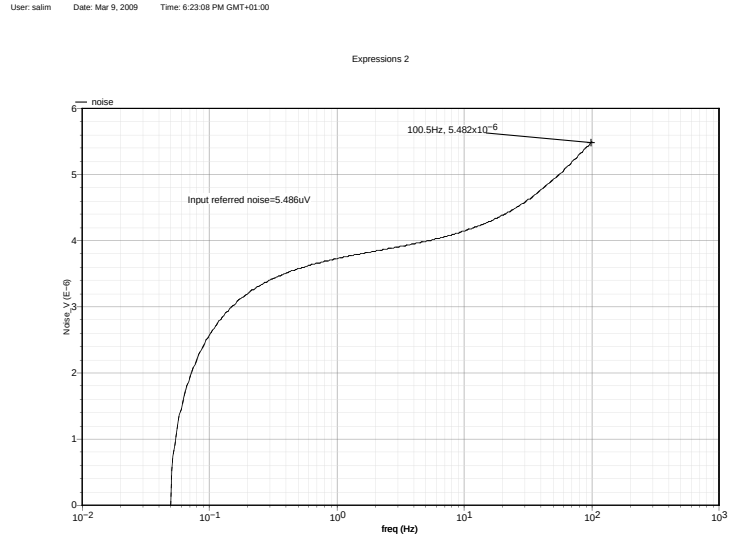

Figure 44: Input referred thermal noise of Bandpass Filter simulated from 50mHz to 100Hz and calculated by Equ. 31

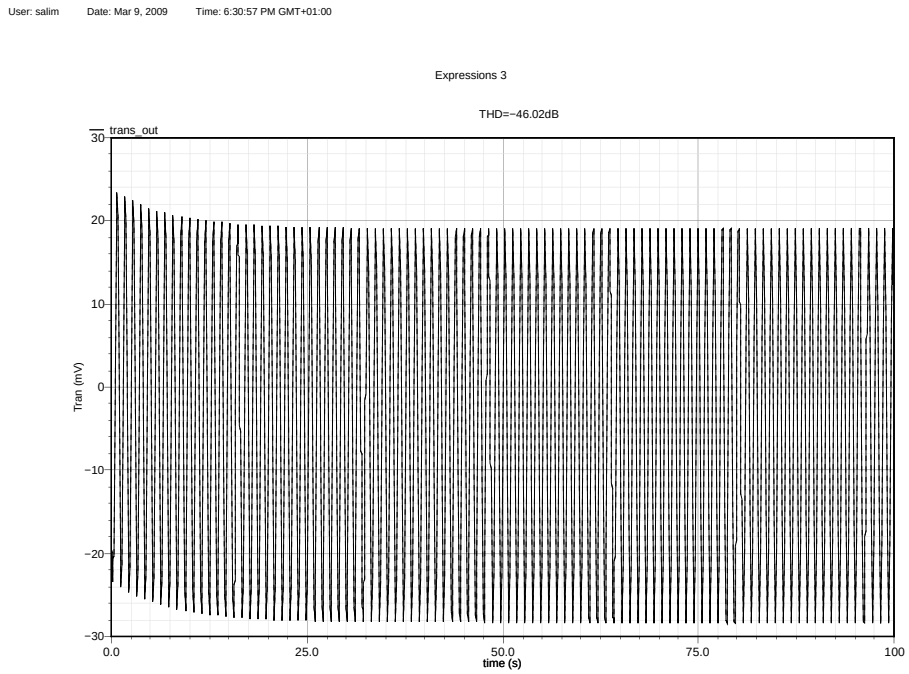

Figure 45: Transient analysis @2.5mV input and 2.23Hz Frequency input

The output signal starts to maintain constant value after 10 second. This behaviour caused by non zero derivative at the input step.

Parameter	Design in[14]	Design in[25]	Design in[33]	Design in[33]	This work
V_{DD}(v)	±2.5	±1.7	1	1	1
Process Technology(μm)	1.5	1.5	0.35	0.35	0.18
Mid-band Gain(dB)	39.5	39.3	40.2	45.6/49/53.5/60	19.51
BW(Hz)	0.025~7.2K	0.015~4K	0.003~245	0.05~262	20~111
Input referred noise(μV)	2.2 (0.5~50kH)	3.6 (20~10KHz)	2.7 (0.05~250kH)	2.5 (0.05~31Hz)	5.39(0.05m~100)
NEF	4	4.9	3.8	3.26	3.3
Power Consumption(W)	80μ	27.2μ	333n	104n	108n

Table 6: Performance Comparison between this work and recent works

From the Table. 12, this work has the smallest technology which means the highest gate leakage form the Pseudoresistor. However, it has similar noise to [19]. Although, the noise in [19] is 2.5μV which is lower than this design. However, the noise bandwidth of [19] is less by a factor of 1/3 than this work.

The reduced bandwidth in[19] reduced the noise. Moreover, NEF is almost the same which is more accurate measure of the noise.

Also, the THD is simulated at the coroners of the frequency response of the filter. At 2.5mV with frequency of 45mHz and 60Hz, the THD is 5.89% and 5.28% respectively. The main reason for the higher THD is the non linearity of the amplifier itself.

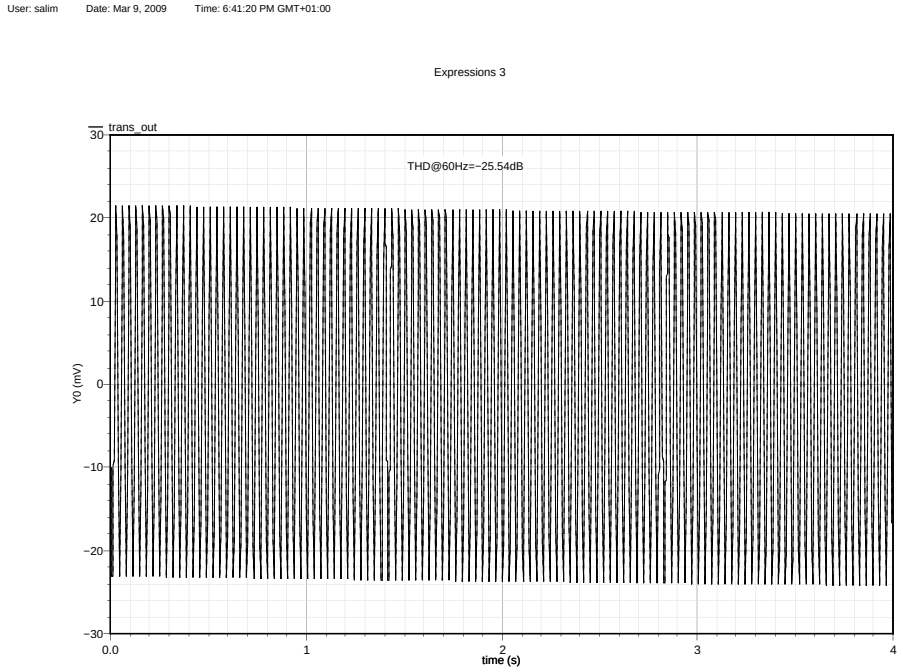

Figure 46: Transient analysis @2.5mV and 60Hz Frequency input

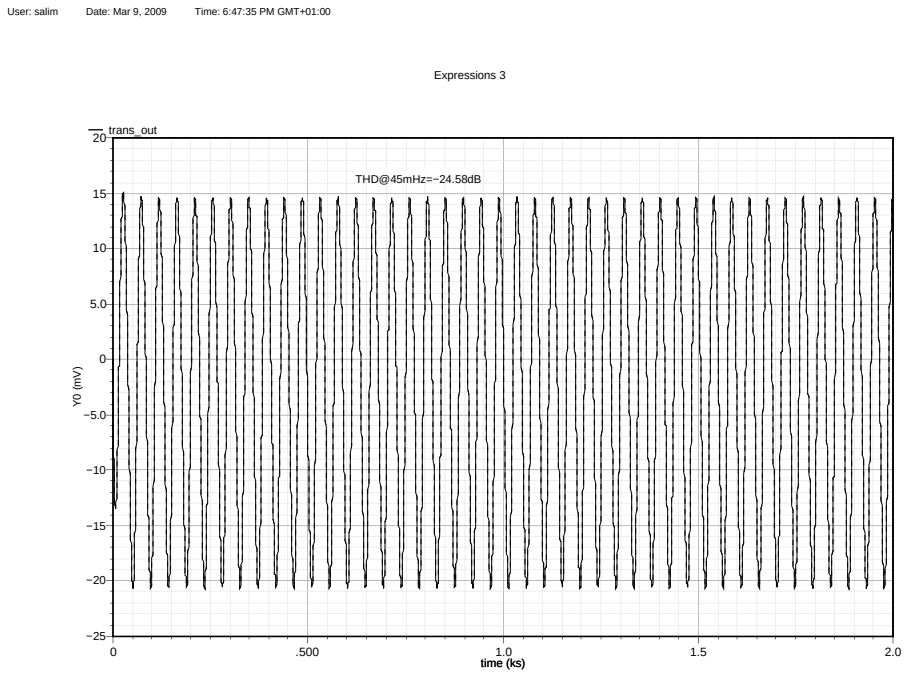

Figure 47: Transient analysis @2.5mV and 45mHz Frequency input

3.6 Conclusion

Bandpass filter is implemented using two Stage Miller Op Amp operating in weak inversion. The low cut-off frequency filter is implemented by pseudoresistor in parallel with capacitor. The high cut-off frequency is function of miller capacitor. The gain is set in way to relax the pseudoresistor and still maintain very low noise of the overall system. The gate leakage of the pseudoresistor is solved by current buffer. Metal-insulator-metal capacitor, mimCap, is chosen to set the gain and to eliminate the leakage and maintain a linear capacitance. The noise and power are optimized. The overall performance of the filter is very similar to the sate of the art design[19].

4 Gm-Current Cell (Second Stage)

In this chapter, the functionality of the Gm-cell is explained. The output current is calculated and simulated. Different linearization techniques are discussed to have general understanding of the trade-off.

4.1 Operational Transconductance Amplifier

The output of the bandpass filter needs to be converted to current since current SAR ADC is used. Gm-cell is implemented as shown in Fig. 48[42, 43].

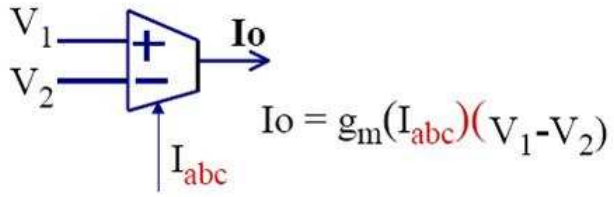

Figure 48: Gm_Cell

The output current which is the full scale current input to the ADC would decides the power consumption of the current ADC as discussed. The relationship between power and full scale input current will be explained in Chapter 5. The input voltages has DC value of around 500.4mV. The amplitude of the input signal to the filter is 5mV. Then, with gain=20dB, the output is 50mV. Iout set to be 25.5nA depending on the reference current (100pA) in the current ADC. The value of the gm is calculated by Equ. 35 [13].

$$Iout = gm(V_1 - V_2) \tag{35}$$

Where Iout=25.5nA,$V_1 = 550mV$,$V_2 = 500mV$, then gm=$0.51\mu A/V$.

The output of the filter is feed to the negative input of the gm and to the positive input through very low frequency filter as shown in Fig. 49. The low

frequency filter is very similar to the one in the bandpass filter. The value of the resistance is increased to make sure that the DC component, 500.4m, is passed only. A cascode current mirror is implemented for OTA to make sure that all the transistor are in saturation and the current is mirrored accurately. The characteristic of the non linearity of the gm is hyperbolic tangent. There are different linearization techniques as discuss in sec.4.2.

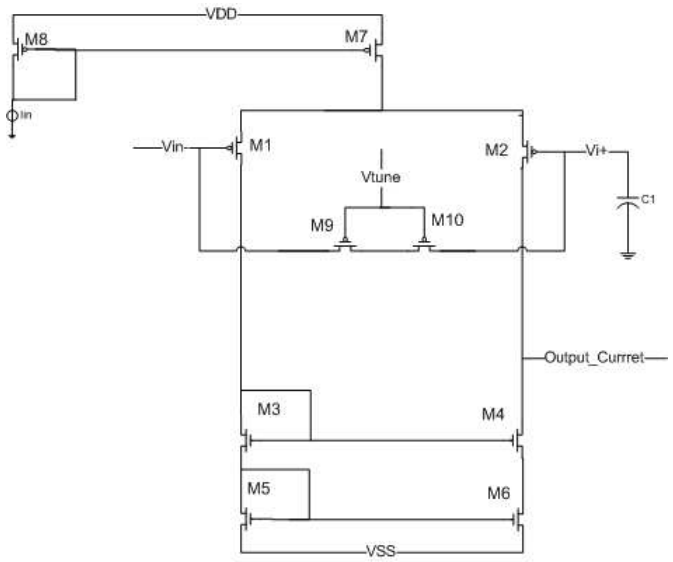

Figure 49: Operational Transconductance Amplifier

The low pass frequency filter is implemented by M9,M10 AND C1. M9 and M10 are sized in way to produce the required resistance.

4.2 Cell Choice (linearization)

Several method of linirization is explained in [13, 44, 43]. Edgar mentioned three way of linearization.(a) attenuation, (b) nonlinear terms cancellation, and (c) source degeneration. Source degeneration is explained briefly here. Source degeneration transconductors using resistor to increase linearity. The resistor

are placed in the differential bair as shown in Fig. 50.

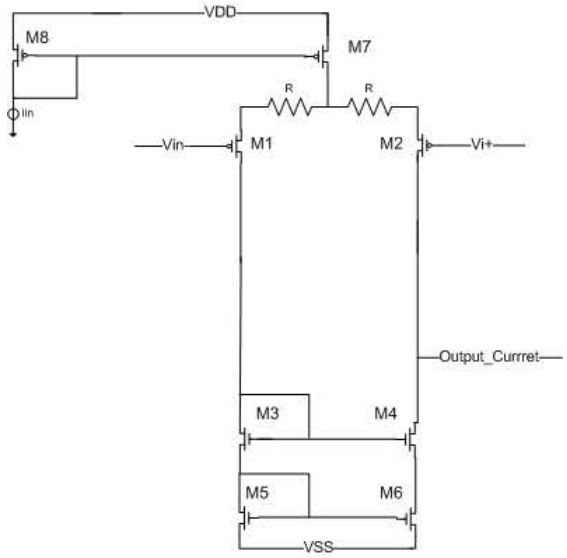

Figure 50: Fixed transconductor

According to Equ.37,36 to reduce the Gm, R has to be increased which leads current to increases to maintain higher loop gain and similar value of output current. The increase in current increases the power consumption[44]. However, to have ultra low power design, the gm should consume the lowest amount of power. In addition, even after adding the resistor, the gm would not be completely linear.

$$I = \frac{gm\,V}{1 + gm\,R} \tag{36}$$

$$Gm = \frac{gm}{1 + gm\,R} \tag{37}$$

For low noise design, the resistor would be implemented by CMOS connected diodes as shown in Fig. 51. The diodes would have voltage drop across them which reduces the linearity furthermore more.

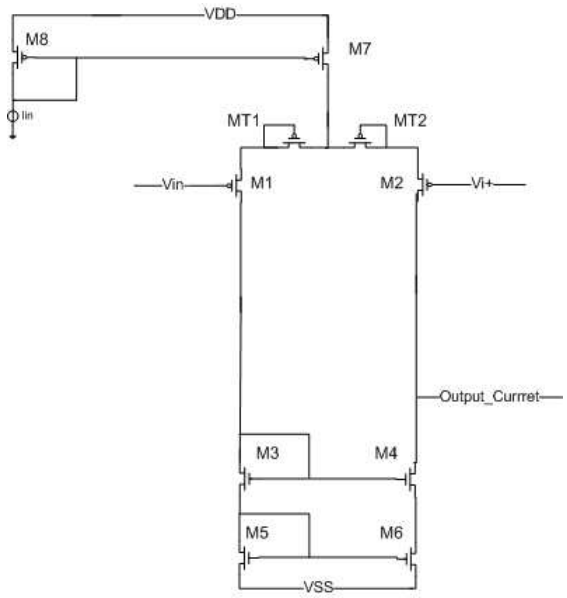

Figure 51: Fixed Transconductors using CMOS connected diodes

Many other designs could linearize the gm. However, most of these designs would consume more power and would not have completely linear [13, 44, 42]. Simulation results of the source degeneration is provided in sec.4.3.

In this design, a conventional operational transconductance amplifier is used without any linirization techniques in order to have the lowest power consumption of the gm-cell. The non linearity of the gm is compensated for by non linear current DAC.

4.3 Simulation Results

The temperature is set to 37.0C, temperature of the human Body. The gm-cell operates in weak inversion. The process technology used is $0.13\mu m$. For measurement purposes, a constant voltage is placed at the output to obtain the required current . The voltage scours has to keep equal voltage across the current mirror. Vconstant is calculated by Equ. 4.3.

$$V_{constant} = Vds_{3+}Vds_5 \tag{38}$$

The input voltage of the ADC is setting the output voltage of the Gm block. Input voltage of the ADC has to be supply the required voltage,Vconstan.

The sizes of the transistors are giving below in Table. 7. The sizes of the gm-cell is chosen to be close to the first stage of the OTA to minimize the noise. The total power consumption of the Gm-cell is 53.03nW.

Devices	M_1,M_2	$M_3, M_4 M_5$,M_6	M_7	M_8	C_3	R_{filter}
W/L(μM)	80/20	40/20	6/3	7.6/6	3.056pF	3TΩ

Table 7: Devices Sizes

The DC output current of the gm is plotted in Fig. 52. The value of the current is $\simeq$0~25.52nA as required. Since the sizes of the transistor is relatively big, the mismatch is minimized. As a result, the non linear current output maintain almost constant value with mismatched.

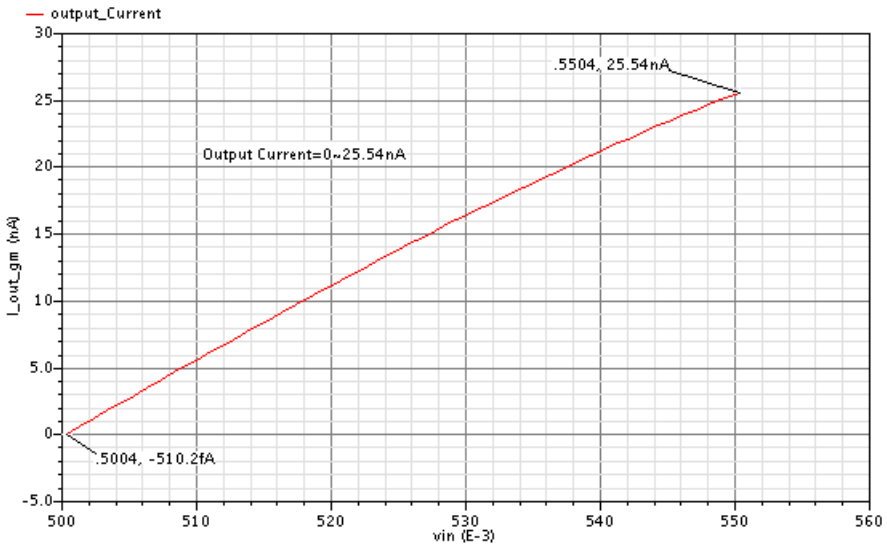

Figure 52: DC-Output Current

In Fig. 52, the LSB of the non linear output current is very close to linear current. The ideal output current is calculated by taking the derivative of the actual output current at biasing voltage of the filter. Then, the result of the derivative is multiplied by the full input voltage swing of the Gm block as in Equ. 39. Also, the difference between the actual output current and ideal current is calculated in Equ. 40.

$$Ideal\,Output\,Current = \left[\frac{dv}{dx}_{v=0.5}(Output\,Current) * Input\,Voltage\right] \quad (39)$$

$$Current\,Error = [Input\,Current - Ideal\,Output\,Current] \quad (40)$$

The ideal,actual and error current are plotted to understand the nature of the

error as show in Fig. 53. The error is around 15%.

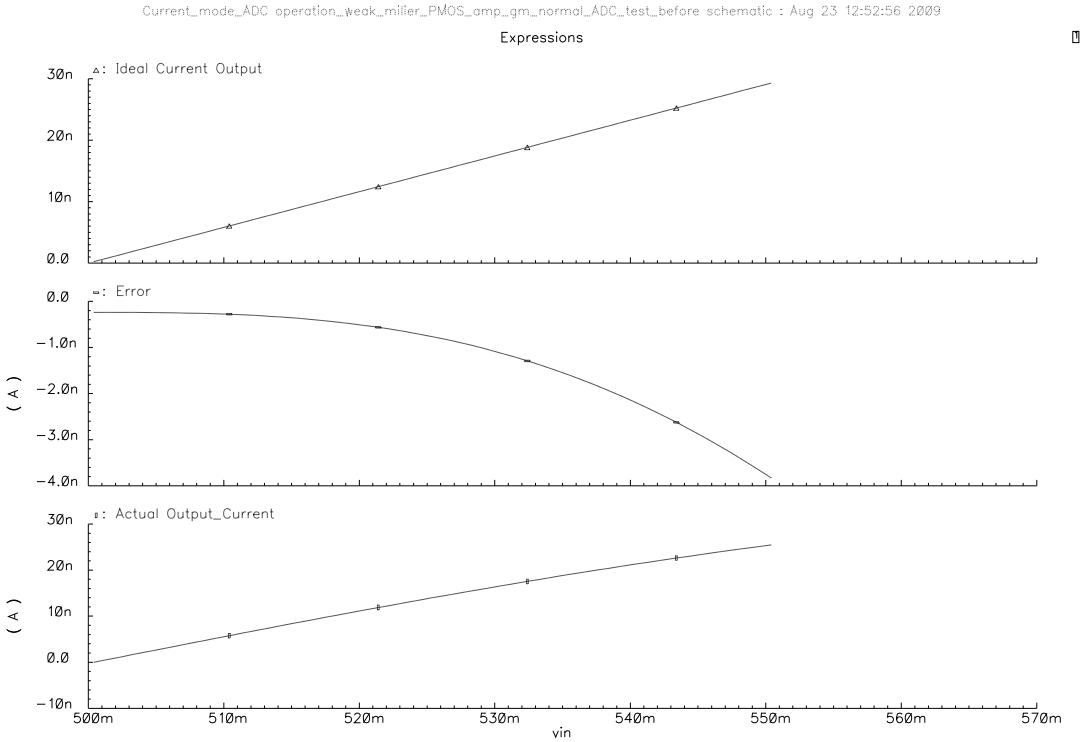

Figure 53: DC-Output Current with Error

The gm block is tested with sine wave to check if the output current match the DC-output current as shown in Fig. 54. The Full scale of the current is 25.55nA which is very close the the DC output current.

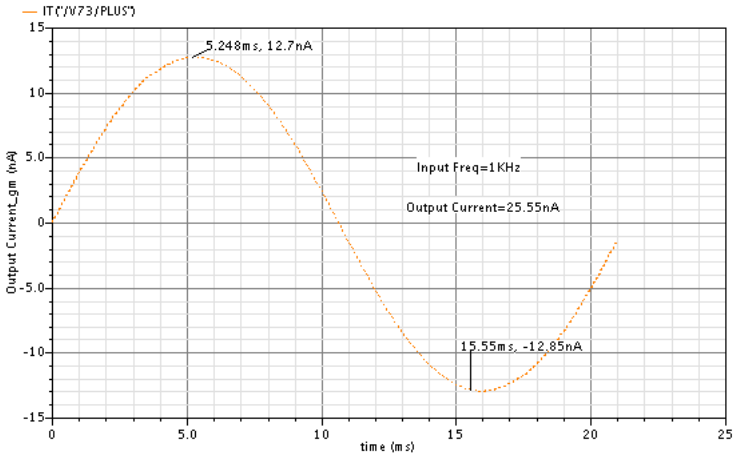

Figure 54: Sine wave_Output Current

From Fig. 55, it is noticeable that the gm is not completely linear in the range of interest(475~525mV).

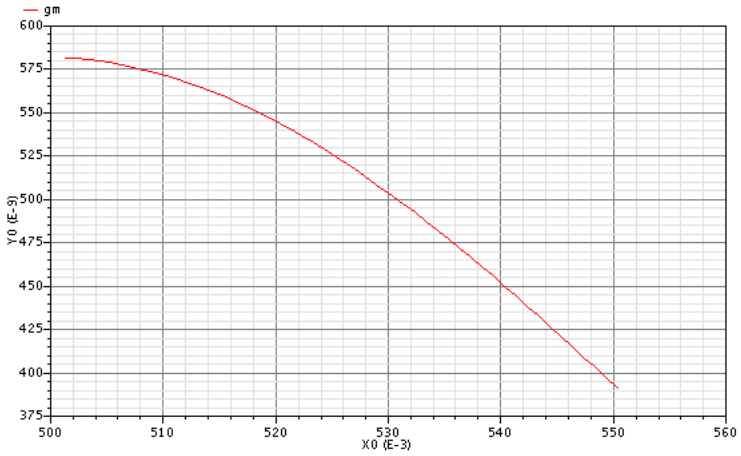

Figure 55: gm of Gm block

The frequency response of the filter in gm is plotted in Fig. 56. The 50mHz is

attenuated by 56.6dB in order to make sure that the DC component is passed only.

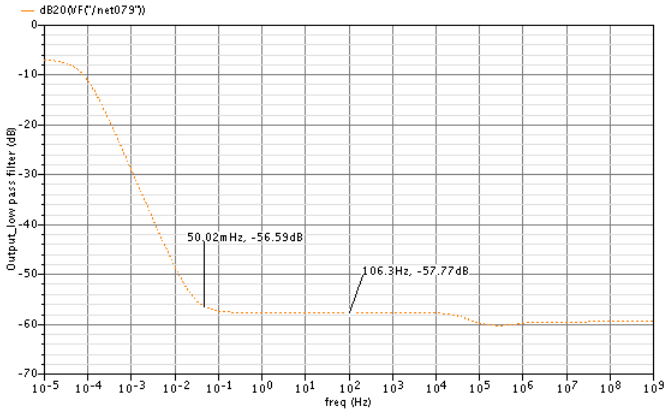

Figure 56: Frequency response of low frequnecy filter in gm Cell

The noise of the gm-cell is simulated and refer to the filter input by Equ. 31 as shown in Fig. 57. The noise is negligible 164.9fV.

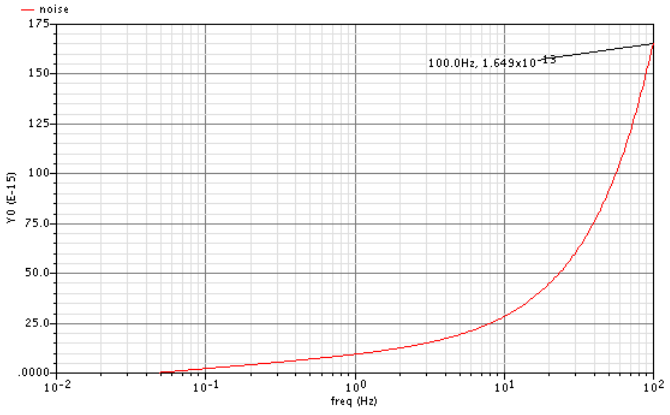

Figure 57: Noise of Gm from 50mHz to 100Hz calculated by Equ. 31

The performance of the non linear Gm block at Process Corner is listed in Table. 8.

Process Corner	Full Scale Output Current(A)
TT	25.54n~-510.4f
FF	25.15n~-219.6p
SS	25.37n~133.8p
FS	24.57n~-295.1p
SF	26.46n~79.3p

Table 8: Process Corner Simulations of Gm block

The full scale output current of FS and SF deviates the most form the full scale output current (25.54nA~-510.4fA) at typical corner. The performance could be enhance by optimizing the circuit at these corner.

The gm of the source degeneration transconductors is shown in Fig. 50. The gm is more linear than the conventional gm. The power consumption is 195nW which is almost four time higher than the conventional gm. The high power consumption match the theory in Equ. 36. In addition, as shown in Fig. 58, the gm is not completely linear.

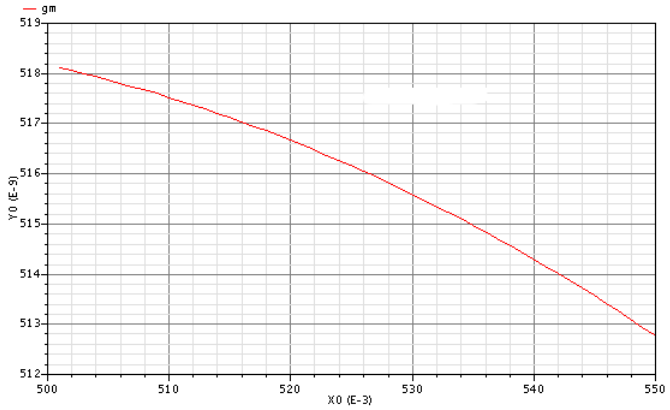

Figure 58: gm_source degeneration transconductors

4.4 Conclusion

Gm-cell is implemented to convert the voltage output of the filter to a current. The value of the current is decided by the full scale current of the ADC. The output of the filter feed to the positive and negative input of the gm. A very low frequency filter is implemented to pass the DC component. Since the gm of the Gm-cell is not linear, different liberalization techniques is introduced in the literature. Source degeneration is investigated. This design is implementing conventional OTA without linearization techniques to reduce the power. The linearity is solve by non linear current DAC in the ADC.

5 Current Successive Approximation ADC (Third Stage)

In this chapter, The architecture of the SAR ADC is presented with the different design aspects. Each block of the ADC (comparator,SAR register and DAC) are explained with simulations results. Statics and dynamics performance of the ADC are presented with Monte Carlo simulations.

5.1 8 bit SAR_ADC Architecture

As stated in Chapter 2, there are only two previous design of current SAR[37, 35]. In this design, a 8 bit with 1KS/s current SAR ADC consists of current sample and hold,current comparator,current DAC,register logic circuit and current mirrors. An system level design is shown below Fig. 59.

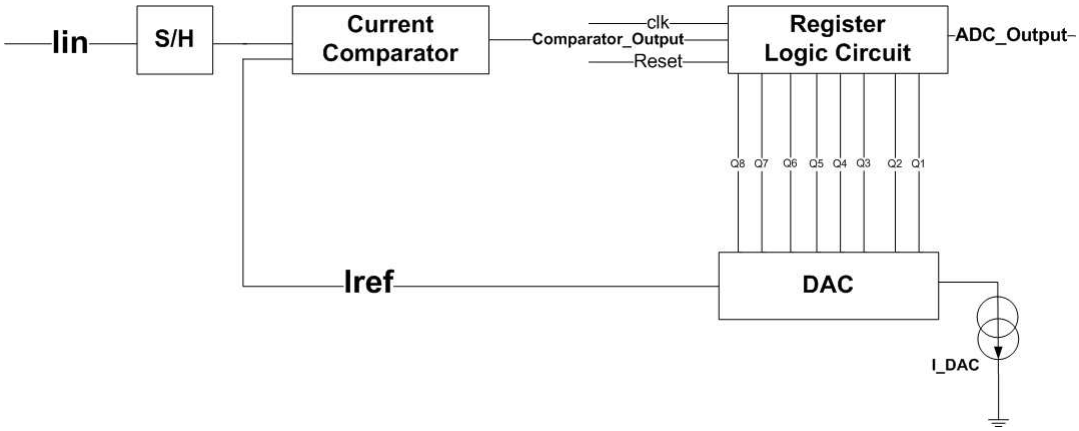

Figure 59: SAR_Architecture

An input current (Iin) is compared in each cycle with reference current using current comparator. Iin is obtained by using a current-mode sample and hold (S&H). Iref is obtained using the current DAC . The current DAC consist of current sources implemented by current mirror. The Iref is calculated by

Equ. 41

$$I_{ref} = (b_8.2^7 + b_7 2^6 + ... + b_2.2 + b_1).I_{DAC-constant} \tag{41}$$

where $I_{DAC-constant}$ is a constant current source to generate Iref. $I_{DAC-constant}$ is equal to 100pA as in [35]. Therefor, I_{ref} is equal to 25.5nA. The lower the constant current, the lower the power consumption as in sec. 5.5. However, a very low $I_{DAC-constant}$ would require very high accuracy current.

The current sources in the DAC are controlled by switches which are controlled by the output of the logic circuit(V_out). The logic circuit (Register) is implementing the successive approximation algorithm. The logic circuit is control by the clk and Reset signal. A full discussion about the logic circuit is in sec. 5.4.

5.2 Current Comparator

Different current comparator topologies are introduced. A simple comparison is explained. A conventional current comparator with minor changes are implemented to maintain the lowest power and high accuracy.

5.2.1 Comparator Topology

The first current topology is reported in [45]. It consists of two simple current mirror. One of the current mirror is connected to input current and the second one to the reference current. Then, the difference between input current and reference current is feed to two or three inverter for different purposes. In general, there are different current comparator topology for high speed application reported in the literature[46, 47, 48, 49, 50]. Most of these techniques are interested to have low input resistance to achieve high speed current comparator. For example, Traff et al. used positive voltage feedback from the CMOS inverter

to maintain a sufficient gain in order to amplify small signal variations as show in Fig. 60[51]. However, at the point where both of the transistor in the first inverts are off, the input resistance increases[46].

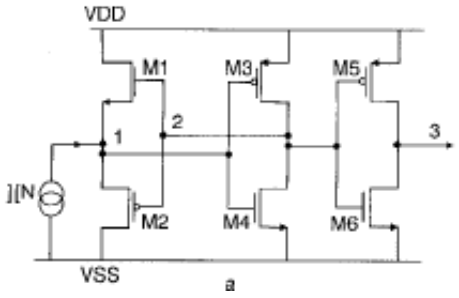

Figure 60: Current Comparator by Traff[51]

Tang et al. used additional circuitry which increases the power consumption[47][46]. In this design, low frequency application, conventional inverter is sufficient and consumes the lowest power. The input and reference current are added using current mirror. In this way, the power is minimized. The accuracy is discussed in sec. 5.2.2 and 5.2.3.

5.2.2 Circuit Implementation

The current difference between Iin and Iref results in $I_{diff} = (I_{in} - I_{ref})$. The, I_{diff} is inverted twice. In the first inverter, Idiff is integrated by the input gate-to-source capacitance. The second inverter changes the sing of the output of the first inverter as shown in Fig. 61[35].

The input current goes through are two cascode current mirror (PMOS and NMOS current mirrors). The two current mirror are used to cancel the Vt mismatch between the NMOS and POMS current mirror. The same structure is used for the reference current as show in Fig. 61.

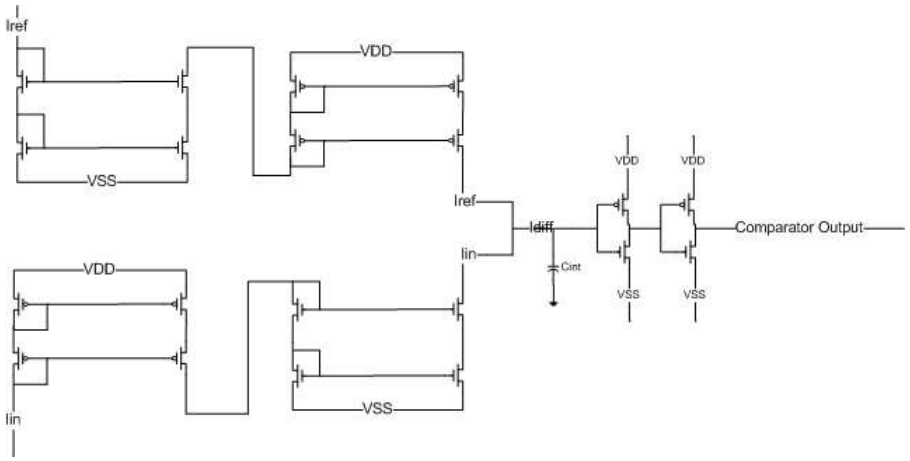

Figure 61: Current Comparator

5.2.3 Accuracy Test and Dynamic Performance

The temperature is set to 37.0C, temperature of the human Body. The current comparator operates in weak inversion. The process technology used is $0.13\mu m$. The sizes of all the transistors including the inverters are $(1\mu m/1\mu m)$ to minimized mismatch. To test the accuracy of the comparator, 1 LSB (100pA) and MSB are taken as an input current. For 100pA, the comparator starts to change at 110pA which is close to 1 LSB. The output is shown in Fig. 62.

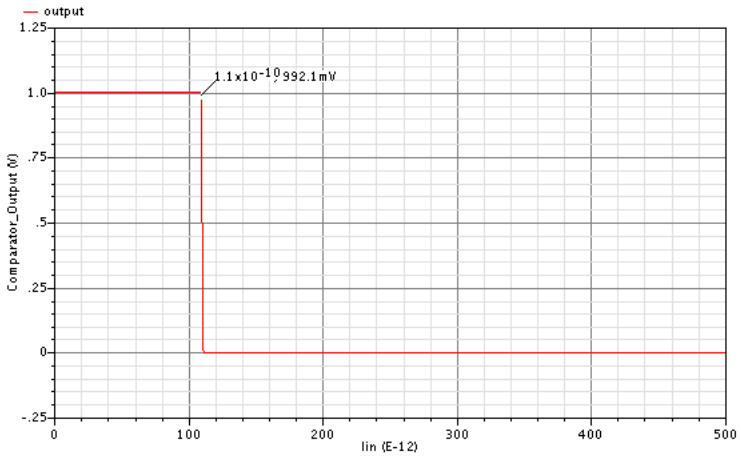

Figure 62: Iin vs Output Voltage of Comparator with Iin=100pA

For 25.5nA, the comparator goes to zero at 25.5nA. The output is shown in Fig. 63.

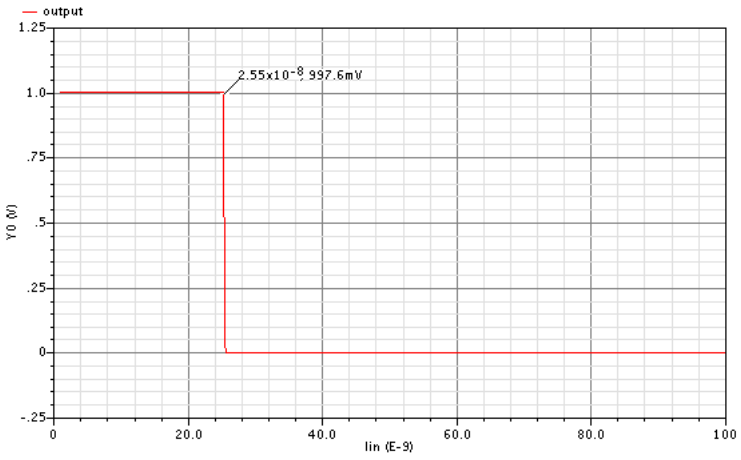

Figure 63: Output of Current Comparator with I=25.5nA

Furthermore, a input current sine wave with amplitude of 200p and reference current with 100p is tested to see if the output of the comparator would change at 100pA. As shown in Fig. 64, the output of the comparator changed at 108.6pA which is very close to 100pA.

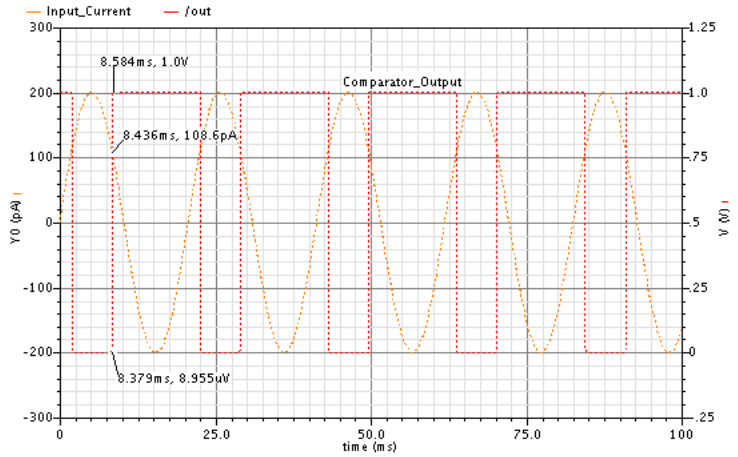

Figure 64: Iin vs Output Voltage of the Comparator with input current sine Wave(200pA)

Finally, the comparator consumes the lowest amount of power with high accuracy comparing with [46, 47, 48, 49, 50] for the intended application of this design. A details analysis of the power calculation and optimization are discussed in sec. 5.5.

5.3 Non Linear (Tanh) Current Steering DAC

In this design, a non linear DAC is implemented to compensate for the non linearity of the gm-cell. A special attention has been paid to the design of the current mirror to get the require performance.

5.3.1 Current Steering DAC Topology

$I_{DAC-constant}$ is mirrored through a current mirrors to generate the current sources of the DAC. The DAC is a unary wighted control. The current sources are scaled to produce the quantization levels. The linear quantization levels are 1, 2, 4, 8, 16, 32, 64 and 128 as shown in Fig. 65.

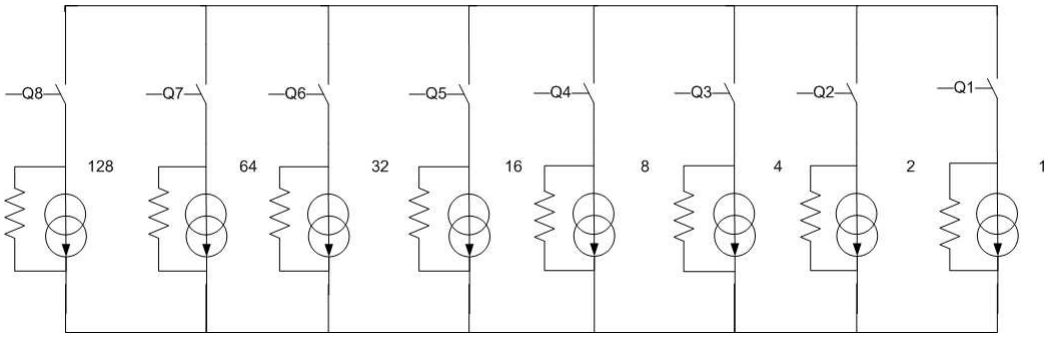

Figure 65: Linear Unary Wighted Control DAC

There are several papers implementing non linear current DAC[52, 53, 54, 55, 56]. All these designs implement a sine or cosine wave function. Edward at el.used row and column thermometer code recorder to control a current cell. The current cell consists of current steering pair (P and N) as show in Fig. 66[53]. The P and N current cell produces the positive and negative part of the sine wave.

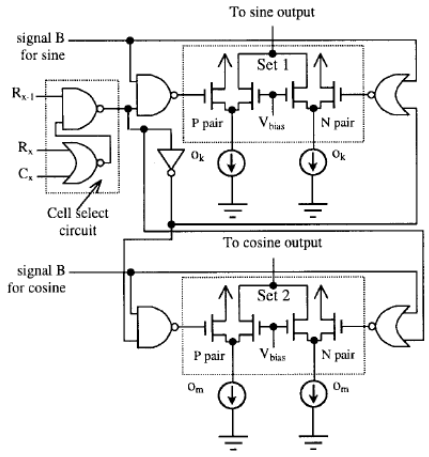

Figure 66: Edward's current cell[53]

For this design, there is no Tanh current DAC reported in the literature. For non Linear (Tanh) Current Steering DAC, the quantization levels obtained form Matlab are [1, 2.26, 4.1, 7.95, 16.211, 31.8, 63.8, and 127.9]. These quantization levels are implemented by changing the ratio of the current mirror of the DAC. The current output of the Unary DAC is mirrored again inside the current comparator as show in Fig. 67.

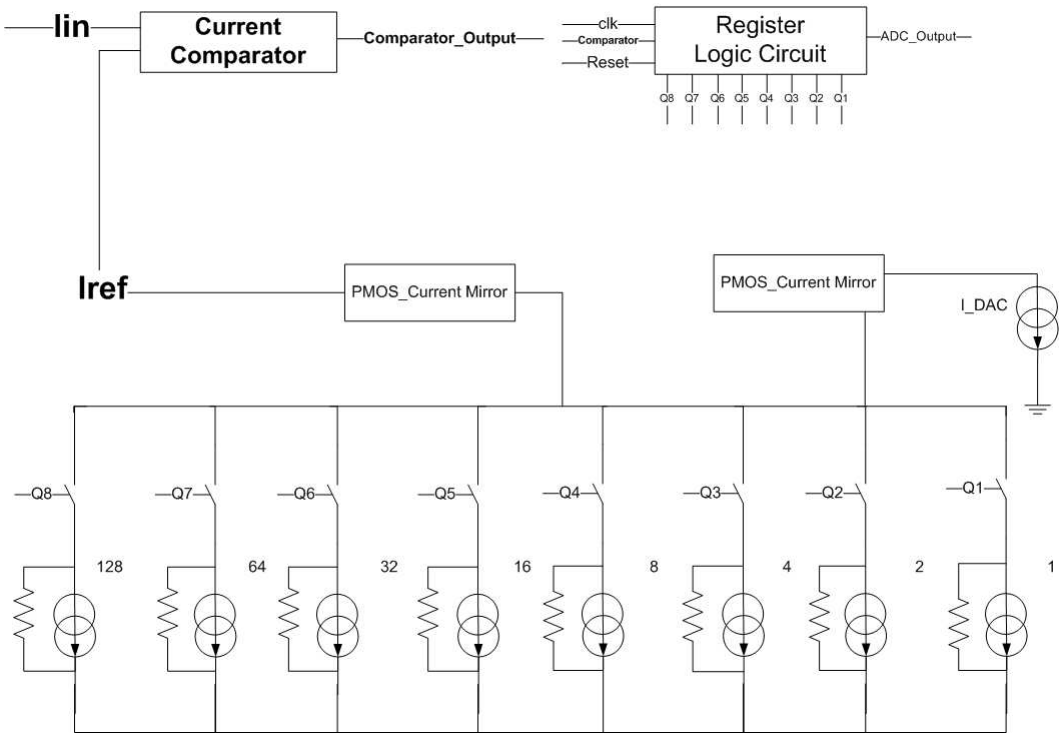

Figure 67: Unary Current DAC

Furthermore, from Fig. 67, the number of current mirror is reduced from 6 to 4 comparing to[35]. The reduction in number reduce the power consumption and the error introduced by each current mirror.

5.3.2 Weak Inversion low Voltage Current Mirror Topology

In current SAR ADC, current mirror is very essential element in the current SAR_ADC. There are two main requirements in the current mirror. First, the current has to be mirror with high accuracy since the 1 LSB is equal 100pA. A small error in certain current mirror could lead to a missing code at the output of the ADC. Second, all transistors implementing the current mirror in the DAC need to be in saturation(Vds>100mV) in order to provide high swing. High voltage swing is necessary for the current sources for two reasons. First,

the current sources should maintain constant value when other current sources are switched. Second, the transient time takes the current source to switch should be minimum. An accurate mirror current is needed. There are several low voltage current mirror in the literature[57, 58, 59, 60, 61]. Most of these designs consumes double of the power of conventional cascode current mirror. However,Bruun at el. used resistor implementing by two CMOS connected diode to bias the current mirror. The two transistor are sized in way to provide the right voltage bias as show in Fig. 68[59].

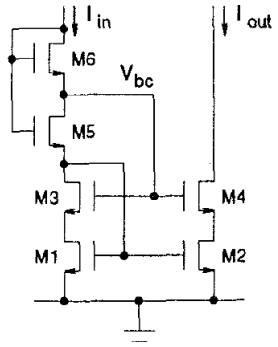

Figure 68: current_mirror by Bruun[59]

However, the technique provided above is not sufficient enough in weak inversion to make all the transistors in saturation. Another biasing scheme is need to make sure all the transistors are in saturation. Abo at el. provides a biasing scheme for the transistors to be in saturation as show in Fig. 69.

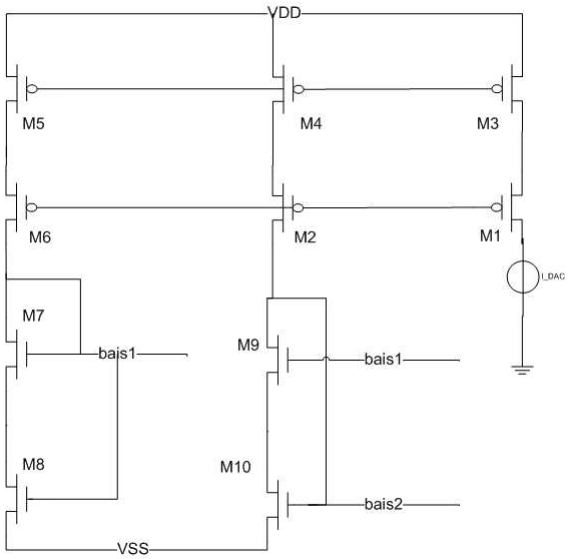

Figure 69: Current Mirror by Abo

M7 and M8 create a voltage source. By controlling the size of M8 which operate in triode region, the correct gate bias voltage is set. Full details about Abo's current mirror is explained in sec.5.3.3.

5.3.3 Circuit Implementation

The circuit implementing of the whole current SAR_ADC is shown in Fig. 70. The sizes of the transistors are provided in Table. 9.

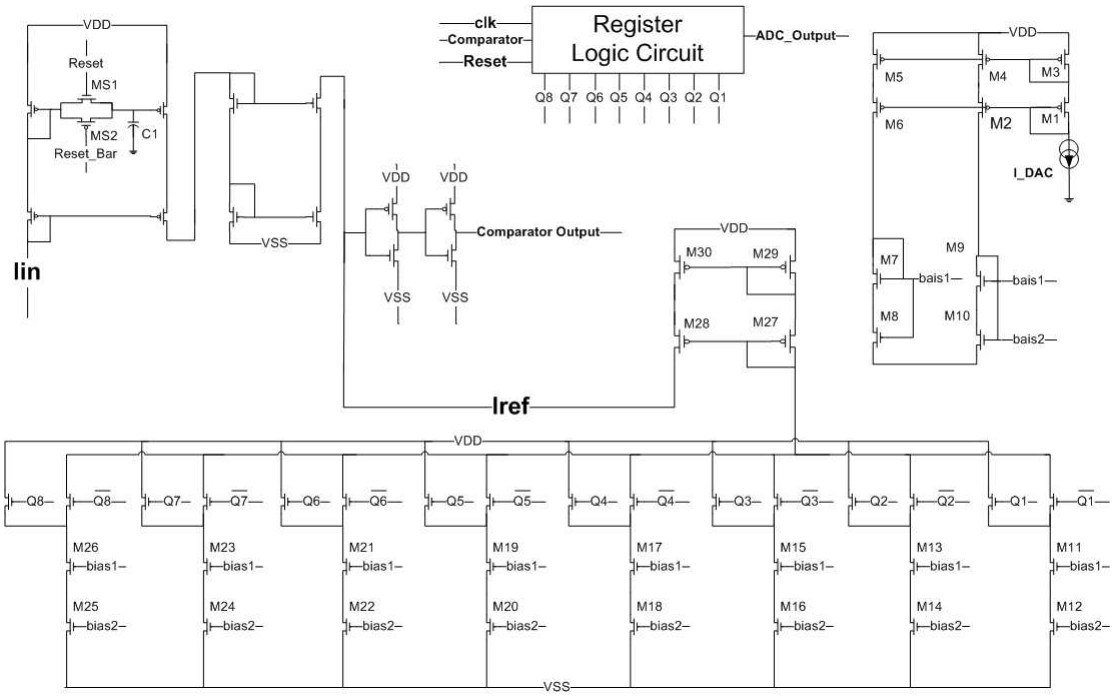

Figure 70: Current Successive Approximation ADC

Devices	M_1,M_2	M_3,M_4	M_5,M_6	M_7	M_8
W/L(μM)	1.76/1	1/1	3/1	1/1	1/15
Devices	M_9,$M_{10}M_{11}, M_{12}$	M_{13},M_{14}	M_{15},M_{16}	M_{17},M_{18}	M_{19},M_{20}
W/L(μM)	1.5/1.5	3.39/1.5	6.15/1.5	11.92/1.5	24.32/1.5
Devices	M_{21},M_{22}	M_{23},M_{24}	M_{25},M_{26}	M_{27},$M_{28}M_{29}, M_{30}$	M(comparator)
W/L(μM)	47.7/1.5	42.5/1.5	192/1.5	10/8	1/1

Table 9: Devices Sizes_ADC

a 1nA(I_DAC) current source is mirror using M1-M4. M7 and M8 is used to generate the gate bias voltage in order for the drain-to-source voltage of M9 and M10 to be equal. M5-M6 are sized to provide scaled version of the I_{DAC}. M7 is a diode-connected device operating in the saturation region. M8 is sized to create a Vds sufficient to keep M9 and M10 in the saturation region. Due to the finite output impedance, the mismatch in the current is eliminated in first order. The output of the DAC is mirror to the current comparator by

M27-M30. The transistors of M27-M30 are sized in way to give enough swing for DAC. M9-M26 are sized to give the thresholds of the non linear DAC. The current source are connected to complementary switche connected to supply voltage (V_{DD}) in order to reduce the leakage current when the switches are off[35]. The input current is sampled by current sample and hold (MS1,MS2 and C1). MS1 is connected to Reset signal and MS2 is connected to Reset signal inverted. CMOS switch is used since the input current is converted to voltage (Vgs) then converted back to current. The Vgs is not close to V_{DD} or Vss. Also, the CMOS switch would reduce clock feedthrough and charge injection.

Layout Considerations

The matching between transistors of this design is not critical because any mismatch can be easily compensated by adjusting I_DAC during device calibration. However, a careful matching between transistors M11- M26 is important because it can affect the accuracy of the ADC. The length of the transistors in M11-M27 is the same ($1.5\mu M$) and the width increases from LSB to MSB. Also, matching in the MSB's transistors is better as compared to the LSB's transistors. The LSBs of the tanh DAC is very smilier to linear DAC. In addition, as mentioned in Chapter 4, the error between the actual and ideal output current in minimum. Therefore, the matching is better and the non linear current output of the DAC maintain almost constant value with mismatched.

Output Impedance

Output impedance of the Unary DAC, R_{unary} ,is function the required INL. The INL of the DAC should be than than 1 LSB to insure minimum deviation

from the transfer function from the ideal interpolation line .The R_{unary} ,is calculated by Equ. 42[15].

$$Output\,Impedance\,of\,Unary\,DAC\,(R_{unary\,DAC}) > R_{load}.2^{2n-2} \tag{42}$$

Where n is the number of bit, Rload is the input impedance of the current mirror M27-M30. The Rload is calculted by Equ. 43.

$$R_{load} = \frac{2}{gm} \tag{43}$$

$$gm = \frac{I_D}{n\,KT/q} \tag{44}$$

Where $I_D$is rhe full scale input current. n,sub-threshold slope, equals to 1.61 according to Chapter 1. KT/q,V_T equals to 26m.

$Id = 25.5nA \Longrightarrow gm = 0.632uA/V \Longrightarrow R_{load} = 3.164M\Omega \Longrightarrow R_{unary\,DAC} >$ $51.77G\Omega$.

The output impedance of the single current source(R_{out}) in the DAC, as show in Fig. 71, is calculated by Equ. 45.

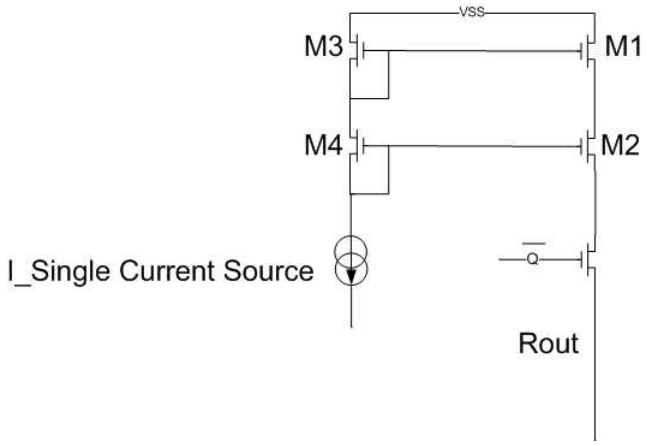

Figure 71: Single current source in Unary DAC

$$(R_{out}) = r_{ds\,switch.} r_{ds1} . gm_1 . r_{ds2} \tag{45}$$

NMOS current mirror is chosen for the DAC since it has smaller sub-threshold slope than the PMOS as mentioned in Chapter 1. Then, according to Equ. 45, gm_{27} is higher and R_{out} is larger. From simulation, Rout for MSB is calculated when the switch is on to be around $100G\Omega$. Rout for MSB by itself without the other current sources is larger than R_{unary} $51.77G\Omega$. As a result, the required output impedance, $51.77G\Omega$ of the DAC is achieved.

5.4 Logic Circuits

Brief details of the logic design is presented in this section. Also, simulation results are introduced to verify the functionality of the logic circuit.

5.4.1 Register Topology

The register topology implanted in this design is the same in [30]. The register consist of two shift registers to implement the successive approximation

algorithm as shown in Fig. 72. The two register are implemented by D-Flip Flop.

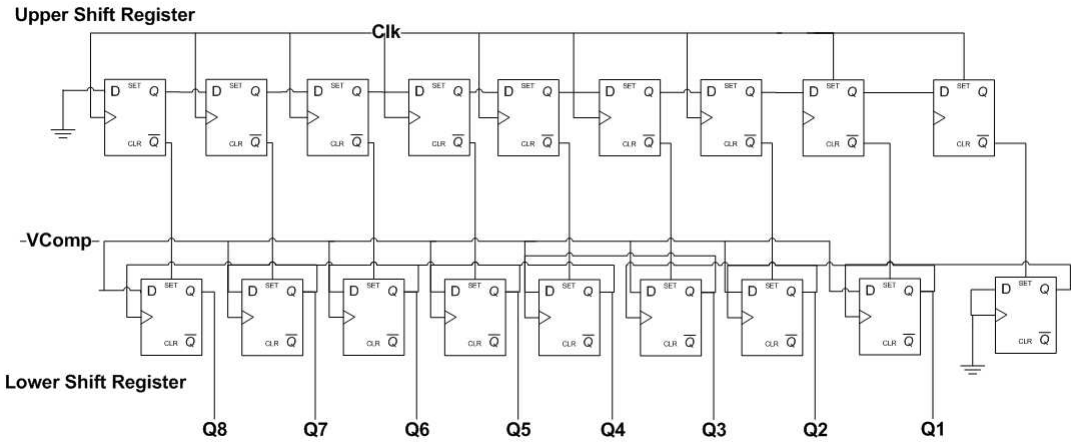

Figure 72: Register logic

The upper shift register is clocked synchronously. The lower register stores the conversion value. When the reset signal arrives, the upper shift register is reset in the 10000000 condition. When the rising edge arrives, the 1 at the first D-Flip Flop propagates along the upper shifter. The 1 value shifts from i-th position to the i+1-th. The inverted output of the upper shift is fed to the input of the lower conversion register. Finally, the output of the lower register is used as a clock the i-th flip flop in the conversion register. Due to the fact that the logic circuit operates at low voltage and low frequency, there are not enough effort in the literature to reduce the power. However, according to [62] which most of the SAR ADC design refer to it, states that because of the large number of registers caused an increases leakage current especially in weak inversion. Also, according to [62], the leakage current in the best case is half time higher than from the voltage comparator. For this design, the case is even more since current comparator which consumes very low power is used instead of voltages comparator. There are several way to reduce the leakage

power. First, number of register could be minimized. Second, using minimum sized logic gates could decrease switching power. Third, using high-threshold devices instead of standard-Vt ones could reduce standby power. In this design, a minimum logic gate was used to reduce the power.

5.4.2 D-Flip Flop

The design of the D-Flip Flop of this logic circuit is implemented in [40] as show in Fig. 73.Using Transmission gate reduce the load on the clock comparing to[40].

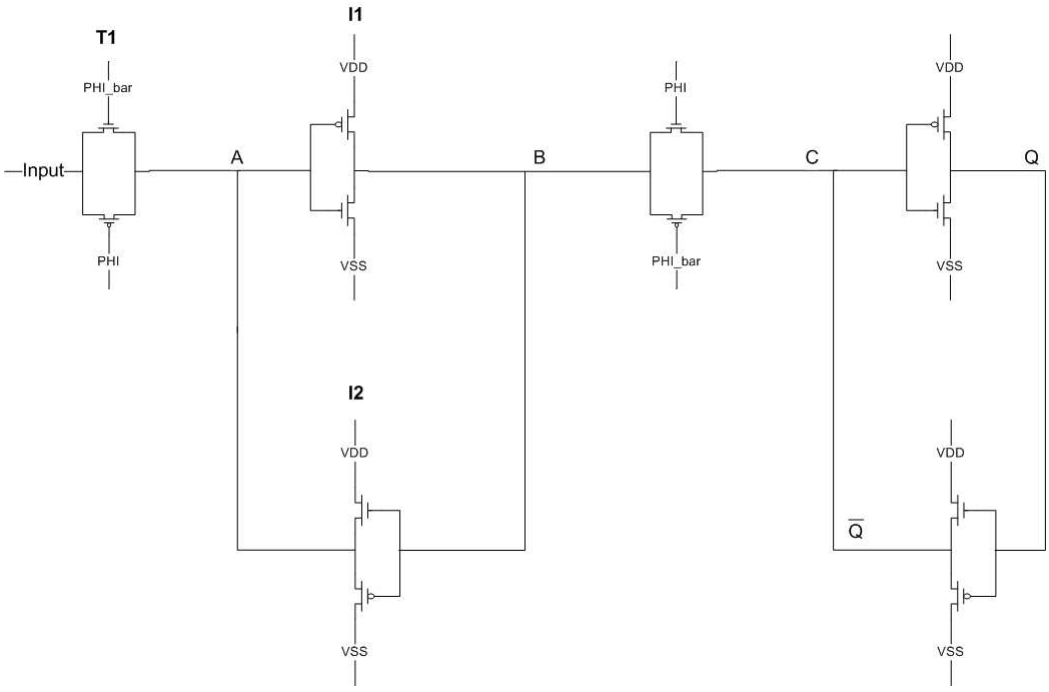

Figure 73: D-Flip Flop by Rabea

In Fig. 73,PHI is the clock frequency,9kHz. PHI_bar is the inverted clock.

However, the design in [40], would increase the design time in order for the T1 and I1 to overpower the feedback inverter I2. If the size of T1 is made to be minimum then I2 should be even smaller by using a larger length. In[63], the

design is modified to have less complex D-Flip Flop. The design of the flip flop is shown in Fig. 74. By using transmission gate at the feedback, it induces a delay in the feedback in order for I2 to store the value at node A without making the size of I2 smaller.

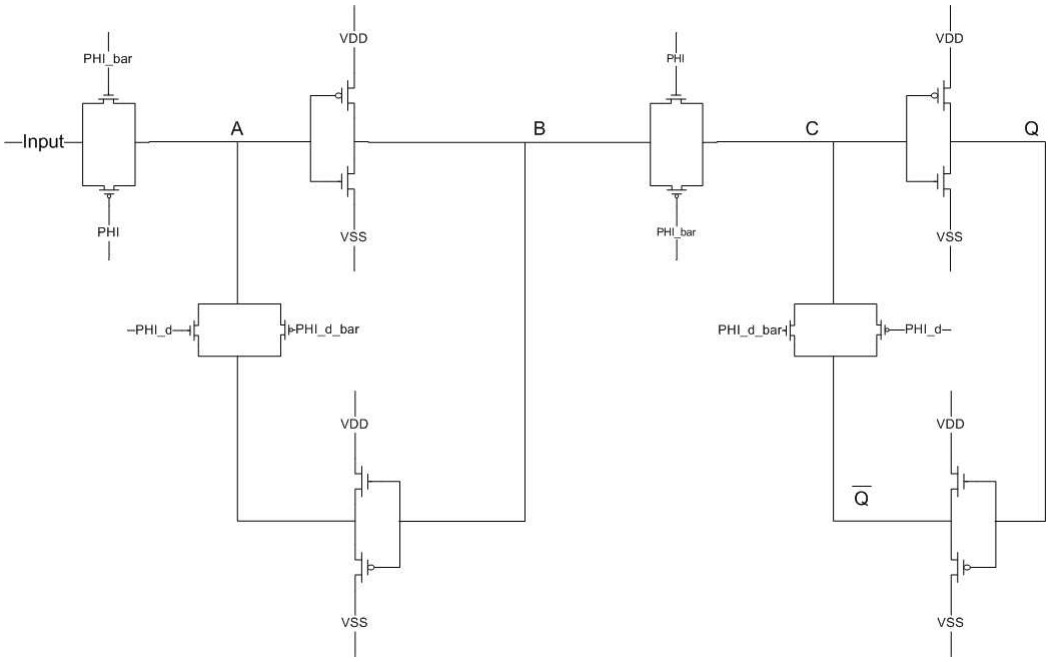

Figure 74: D-Flip Flop

In Fig. 74,PHI is the clock frequency,9kHz. PHI_bar is the inverted clock. PHI_d_bar is the inveted PHI_bar.

5.4.3 Simulation Results

The temperature is set to 37.0C, temperature of the human Body. The filter operates in weak inversion. The process technology used is $0.13\mu m$. All the sizes are set to minimum(160nM/120nM). The upper register act like shift register as show in Fig. 75.

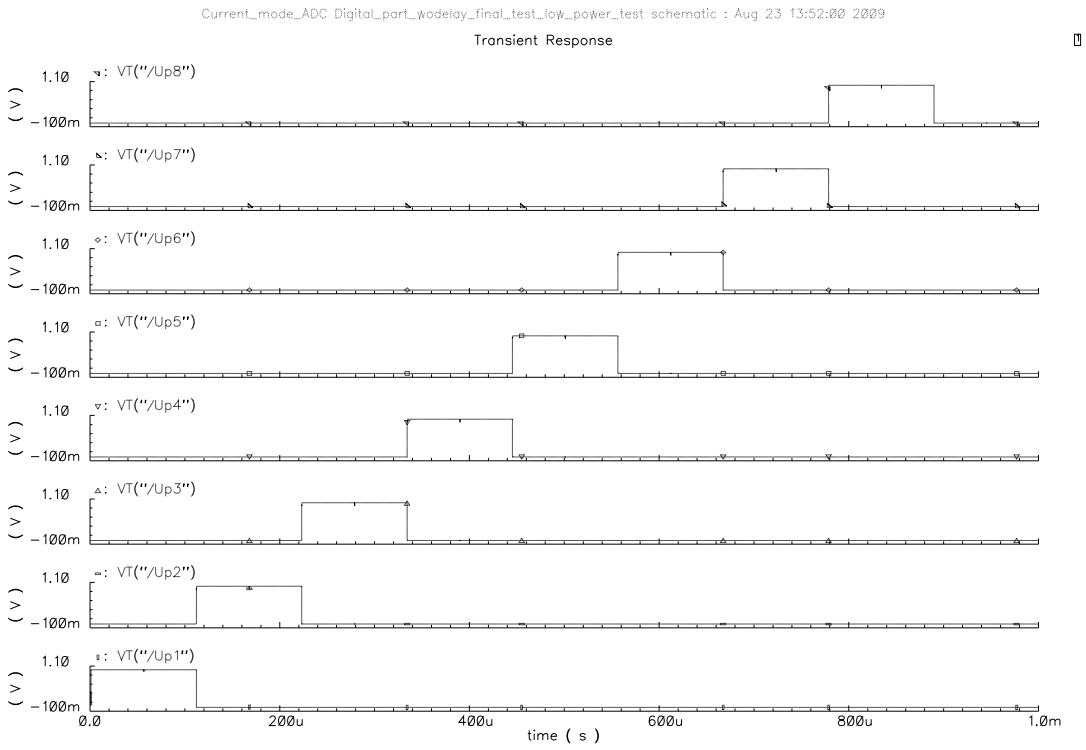

Figure 75: Transient output of Upper Shift register of SAR logic Circuit

The output of each D-flip flop is shifted at the rising of the RESET signal. To test the functionality of the logic circuit, a comparator with value of 0V is tested as shown in Fig. 76

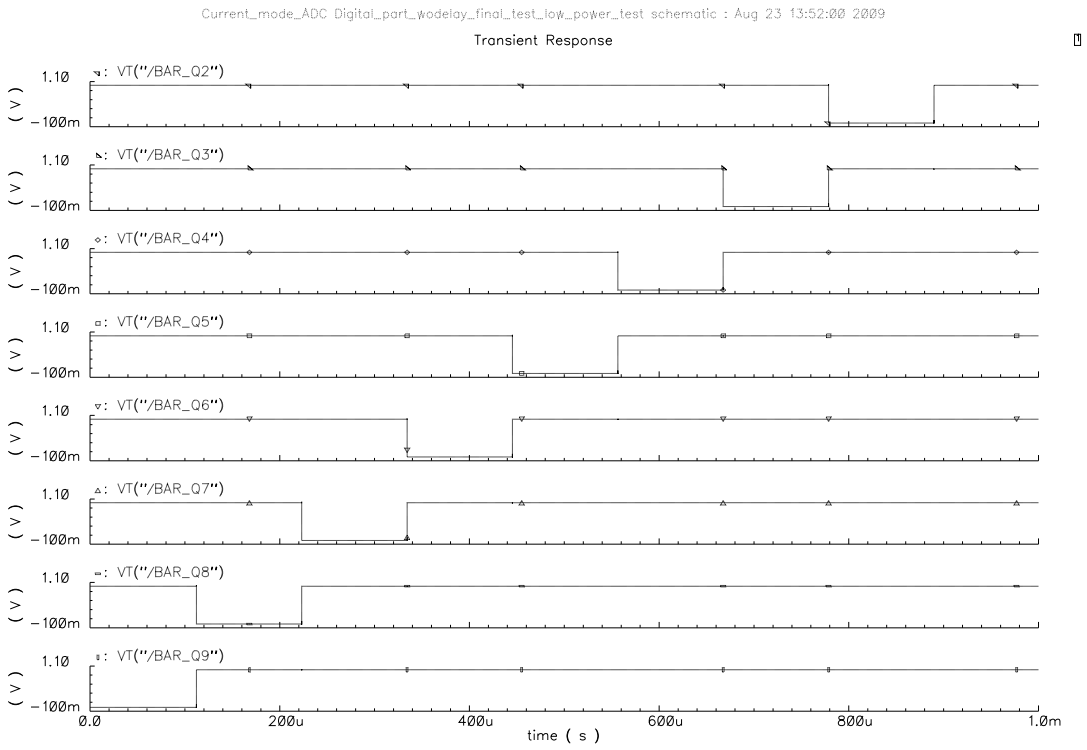

Figure 76: Transient output of the lower Shift register of SAR logic Circuit

The output of the logic circuit,lower Shift register, is shifted depending of the output of the Upper Shift register as show in Fig. 75.

5.5 Power Calculation and Optimization

The total power consumption of the ADC could be calculated depending on the full scale input current and the I_{DAC}. The lower the full scale input current the lower the power. However, the full scale input current can be only lower to a certain limit because the accuracy would start to decrease. The SAR logic consume the largest power consumption. If a 0.5V supply is used the power consumption can be reduced to one-fourth (50nW). More detailed studies is

needed to calculate the leakage current of the D-Flip Flop at such low frequency. In general the power consumption of this design could be calculated by Equ. 46:

$$Total\,Power = [(I_{full\,scale}.V_{supply})_{Comparator} \tag{46}$$

$$+ [(1\,LSB + m\,LSB).V_{supply}) + (I_{full\,scale}.V_{supply})]_{DAC} + Power_{logic}]$$

In the DAC 's term, m is the scaling factor in the current mirror. The total simulated power consumption of the ADC without optimizing the logic circuit is 255nW.

5.6 ADC Performance & Simulations

The ADC is tested with DC value and sine wave. Statics and Dynamic simulations are presented. Also, Monte Carlo and process corner simulations are performed to validate the robustness of the ADC.

5.6.1 Simulation results

The temperature is set to 37.0C-temperature of the human Body. The filter operates in weak inversion. The process technology used is $0.13\mu m$. The sampling frequency is 1KS/s and 8 bit resolution. First to test the ADC a DC value of 10.1nA is taken. The output of the ADC is shown in Fig. 77. The output of the DAC is 10.15nA wish is close the 10.1nA.

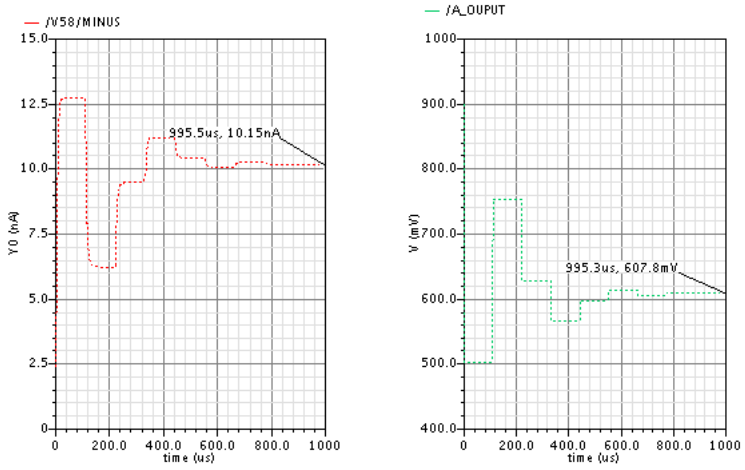

Figure 77: ADC Output with DC input

Then, a sine wave is taken as an input in order to check if the ADC is able to digitize all the different values. The output of the ADC with linear DAC is shown in Fig. 78. The output is obtained by ideal DAC at the output of the ADC. The wave forms is plotted to validate the shape. The output of the ADC is modulated depending on the input frequency bandwidth. To test the performances of the ADC, statics and dynamics performance of the ADC are discussed in sec. 5.6.2, 5.6.3.

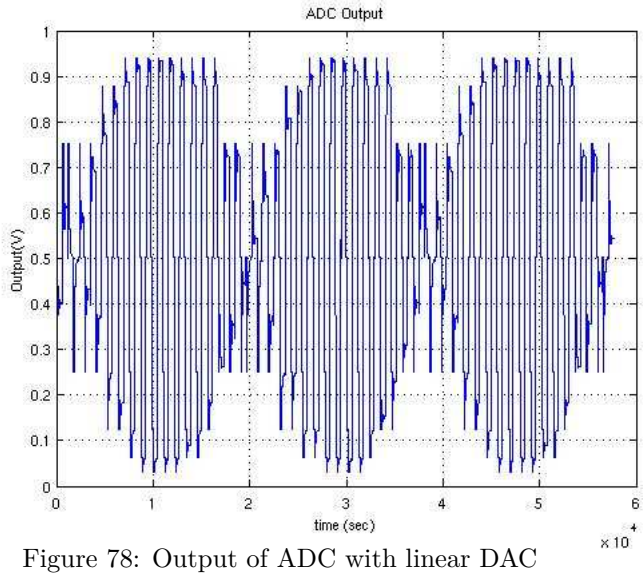

Figure 78: Output of ADC with linear DAC

The output of the ADC with non linear DAC is shown in Fig. 79.

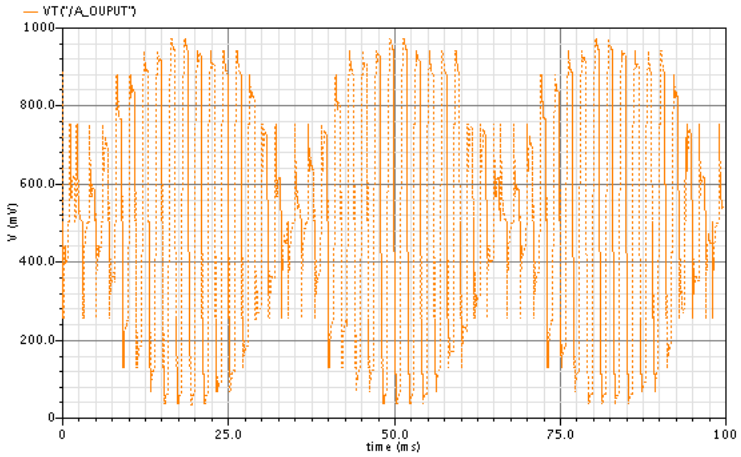

Figure 79: ADC_Non linear DAC

5.6.2 Static Performance(DNL,INL)

Typical ADCs are design to have DNL<0.5LSB. The DNL of this design is = +0.9039 / -0.7692 LSB which guaranteed no missing code. The INL is =+2.0382 / -1.129 LSB which insure minimum deviation from the transfer function from the ideal interpolation line. Usually, the INL>DNL as the case of this design. A current input ramp is tested to measure the DNL and INL. The length of the ramp is calculated by Equ. 47.

$$Length\,of\,Ramp = 2^{nbit}.nbit.\frac{1}{fs} \tag{47}$$

Where nbit is the number of bit and fs is the sampling frequency. For 8 bit and 1KS/s, the length of the ramp equals to 2.048 seconds. The DNL and INL is calculated by Murmann's code[64].

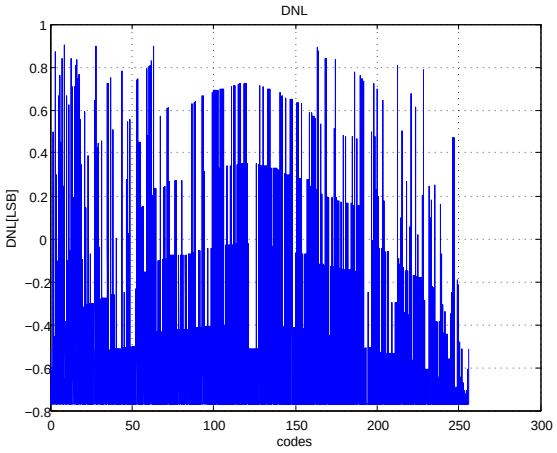

Figure 80: DNL of ADC with non linear DAC

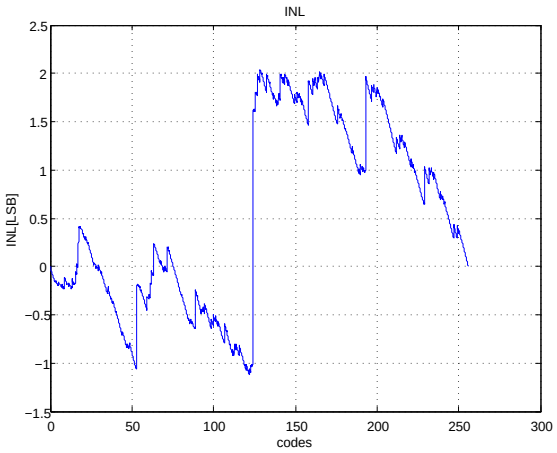

Figure 81: INL of ADC with non linear DAC

5.6.3 Dynamic Performance(THD,SNDR,ENOB,FOM)

The THD for ADC with linear DAC is 47.02dB. For ADC with non linear DAC, the THD is 47.51 dB which match the result of the simulation of matlab in Chapter 2. To calculate SNDR (Signal to Noise Distortion Ratio) , the noise has to be calculated. a 1 LSB=100p is refereed to the gm input and then to the filter input. Ideally, the noise should be less that 1 LSB The noise is equla to 32.59nV which is negligible. Also, according to Chapter 2, the noise of the ADC is negligible. In addition the noise of the current comparator is simulated by Equ. 31 as show in Fig. 82. The noise is equal to 15.19nV which is negligible.

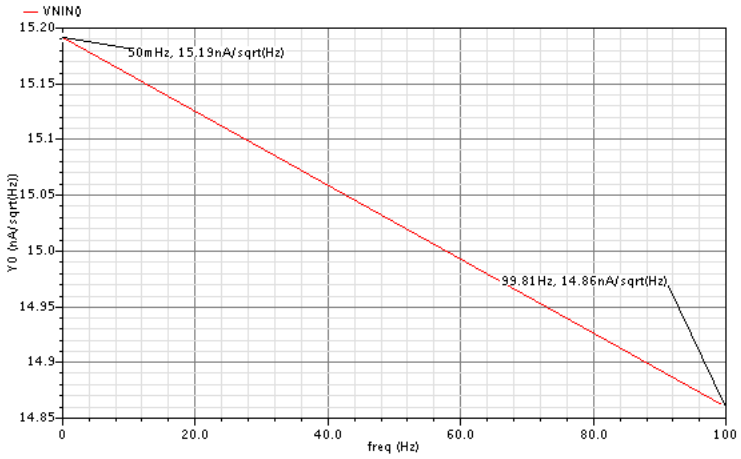

Figure 82: Noise of Current Comparator from 50mHz to 100Hz calculated by Equ. 31

As a result, the the SNDR could be equal to $|THD|$. To have more accurate measurements and comparison between this design and other related works the ENOB (Effective Number of Bit) and FOB(Figure of Merit) have to be calculated. The ENOB and FOB are calculated by Equ. 48,49 respectively[15].

$$ENOB = \frac{SINAD_{dB} - 1.76}{6.02} \tag{48}$$

$$FOM = \frac{Power_{total}}{2^{ENOB}.2.fs} \tag{49}$$

Where fs is the sampling frequency.

For this design, ENOB=7.598 bit and FOM= 0.6580pJ/conversion step. A comparison between the different work is in Table. 10.

parameters	Design in[33]	Design in[19]	This work
VDD(V)	1	1	1
Process Technology(μm)	0.35	0.35	0.13
Sampling Rate	1KS/s	1KS/s	1KS/s
Resolution(bit)	11	12	8
THD(dB)	-	-	-47.51
DNL(LSB)	+/-1.5	+/-0.8	+0.9039 / -0.7692
INL(LSB)	+/-2	+/-1.4	+2.0382 / -1.129
ENOB	-	10.2	7.595
FOM(J/Conv)	-	0.197p	0.6580p~0.284p*
Power Consumption(W)	1.97μ	465.4n	255n~110n*

* If the power consumption of the logic circuit is 50nW.

Table 10: Comparison between this design and recent works

If the LSB set to 50pA which is equal to I_DAC_Constant, then the total power consumption is equal to 55nW and FOM equals to 0.141 pJ/Conv. Such ultra low power could be achieved if the noise and accuracy requirements are satisfied.

The performance,THD, of the ADC with non linear DAC at Process Corner is listed in Table. 11.

Process Corner	THD(dB)
TT	-47.51
FF	-45.29
SS	-43.83
FS	-46.67
SF	42.12

Table 11: Process Corner Simulations of ADC with non linear DAC

The THD of FS and SS deviates the most form the THD,-47.51dB at typical corner. The performance at FS and SS corner could be enhance by optimizing the current mirror at the DAC.

- Monte Carlo Simulation

Montcarlo Simulation is done with 25 runs. Sampling frequency 1KS/s and 8 bit. THD and Total power is simulated as show in Fig. 83,84. For THD, the mean value is -44.5dB which is only 3 dB less than the simulated value. 4 runs are -47.5 dB.

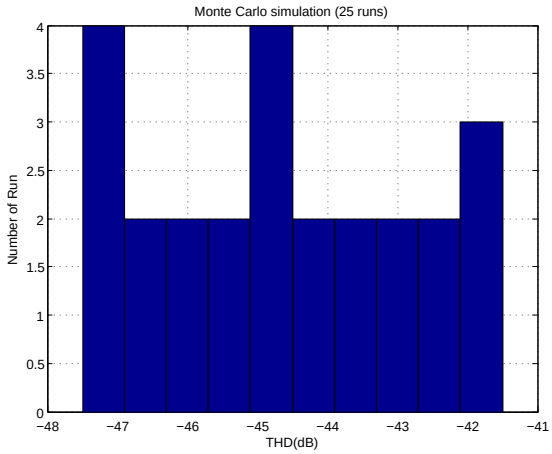

Figure 83: Montcarlo Simulation_THD

There are variations in the total power caused by the mismatch in the current source. As a result, the power of the logic circuit and comparator changed as well. The mean value is 190nW. 8 of the runs falls into 225nW.

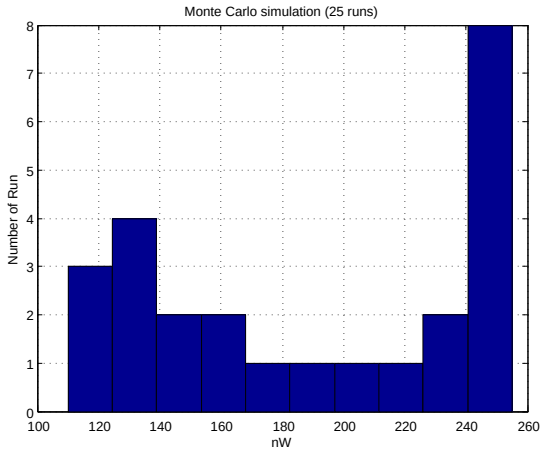

Figure 84: Montcarlo Simulation_Total Power

5.7 Conclusion

Current Successive approximation ADC has been designed and simulated. The first Non linear DAC implementing Tanh is designed in this work compared to the literature. The non linear DAC compensates the non linearity of the Gm Block. Current comparator is designed with low power consumption compared in the literature. A Low voltage high accuracy current mirror is designed to archive the required accuracy. The process corner and Monte Carlo Simulations are comparable with the simulations at typical corner without mismatch The simulated total power consumption of the current SAR ADC is the lowest reported in the literature with a comparable FOM,Figure of Merit.

6 System Simulations

Simulations of the overall system is performed. The output of each stage and block is tested. Different aspect of the whole system are discussed.

6.1 System Simulations in Cadance

The whole system consist of bandpass filter (50mHz~100Hz), Gm-cell and Current Successive Approximation ADC as shown in Fig. 85.

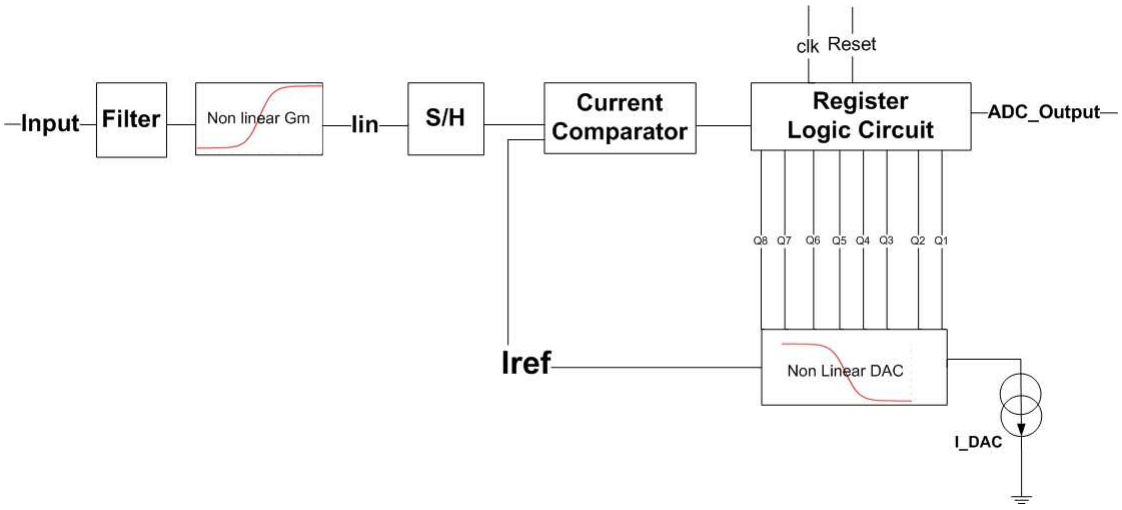

Figure 85: Overall System

Input voltage of the filter,output voltage of the filter, are presented in Fig. 86,88,91 respectively.

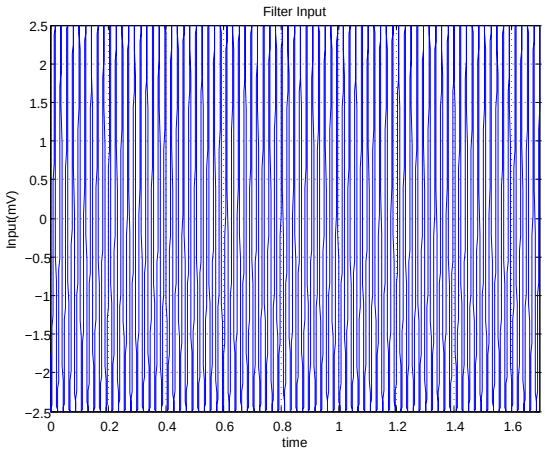

Figure 86: Input Voltage

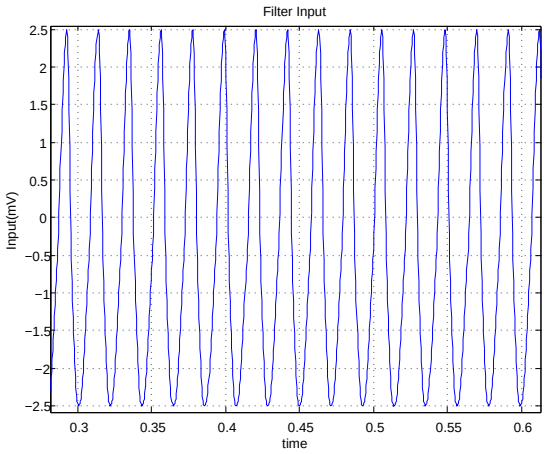

Figure 87: Input Voltage_zoom

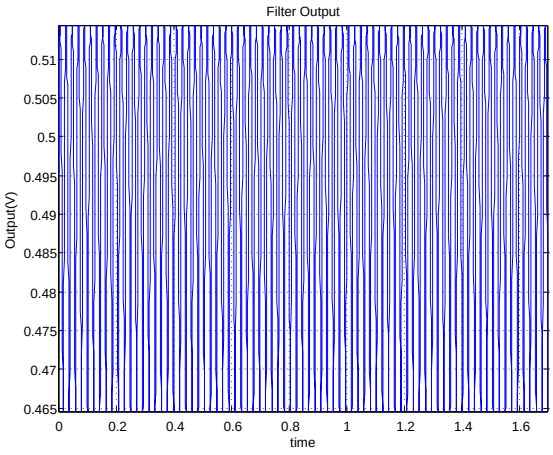

Figure 88: Output Voltage of the Bandpass Filter

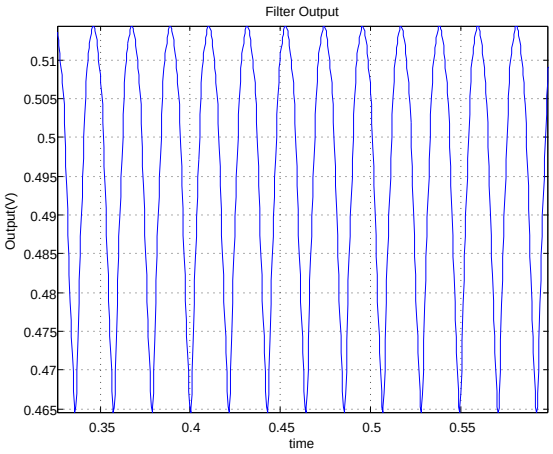

Figure 89: Output Voltage of the Bandpass Filter

As shown in Fig. 88, the input signal is amplified by 19.51 dB. The filter characteristics of the Bandpass filter is very close to the simulation results on Chapter. 3 as show shown in Fig. 90. The baising voltage is changed by small amount. The new baising voltage is 500.6mV. The valued is restored by increasing the output current by very small amount. The changed in baising

voltage caused by gm load.

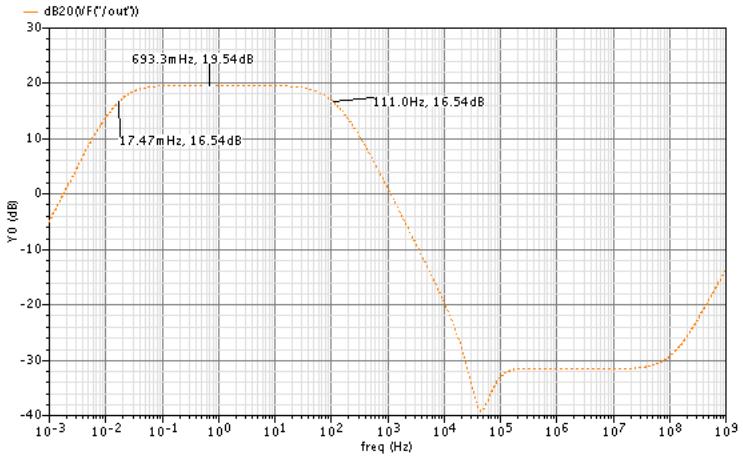

Figure 90: Frequency Response of the Filter

The DC gain equals to 19.54 dB. The BW of the Bandpass filter is 17.47mH to111Hz. Output current of the gm is presented in Fig. 91.

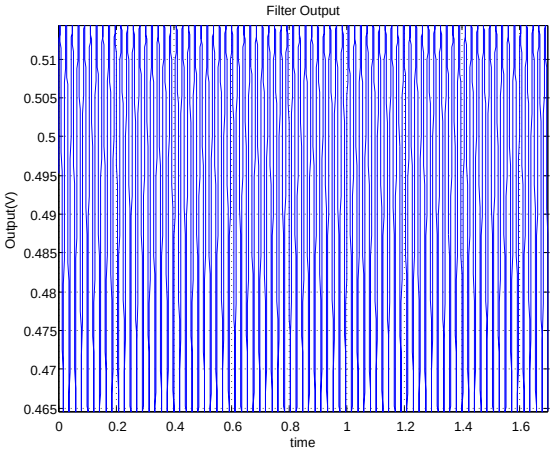

Figure 91: Output Current of Gm-Cell

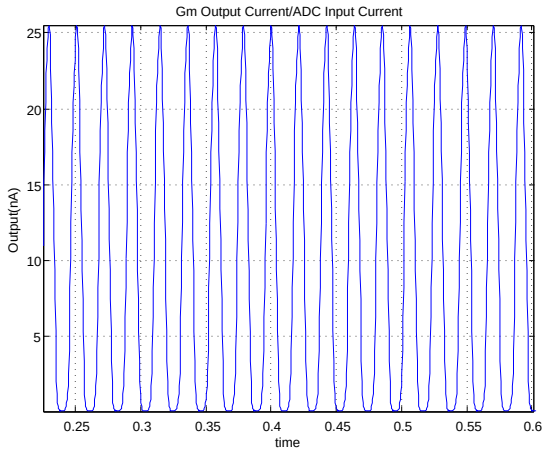

Figure 92: Output Current of Gm-Cell_zoom

The sized of the folded current mirror in the current comparator is increased to match the voltage node at the output of the gm and input of the ADC.

The THD is calculated to be -46.8 dB which is close the value reported in Chapter 5. However, when linear DAC is tested, the THD is -42.32 dB. As a result, the Non linear DAC has an improvement around 4.5 dB over the linear DAC. In other words, implementing a non linear DAC cancel the harmonies distortion caused by the non linearity. The performance of the design and the compression of the recent state of the art works are presented in Table. 12.

Parameter	Design in[14]	Design in[25]	Design in[33]	Design in[19]	This work
V_{DD}(v)	±2.5	±1.7	1	1	1
Process Technology(μm)	1.5	1.5	0.35	0.35	0.18
Mid-band Gain(dB)	39.5	39.3	40.2	45.6/49/53.5/60	19.51
BW(Hz)	0.025~7.2K	0.015~4K	0.003~245	0.05~292	20~111
Input referred noise(μV)	2.2 (0.5~50kH)	3.6 (20~10KHz)	2.7 (0.05~250Hz)	2.5 (0.05~30)	5.39(0.05m~100)
NEF	4	4.9	3.8	3.26	3.3
Sampling Rate	-	-	1KS/s	1KS/s	1KS/s
Resolution(bit)	-	-	11	12	8
THD(dB)	-	-	-	-	47.51
DNL(LSB)	-	-	+/-1.5	+/-0.8	+0.9039 / -0.7692
INL(LSB)	-	-	+/-2	+/-1.4	+2.0382 / -1.129
ENOF	-	-	-	10.2	7.595
FOM(J/Conv)	-	-	-	0.197p	0.6580p~0.284p*
Total Power Consumption(W)	80μ	27.2μ	2μ	895n	416n~276n*

Table 12: Comparison between this work and recent puplished works

If the LSB set to 50pA which is equal I_DAC_Constant, then the total power consumption of the overall system is equal to 216nW. The current mirror in the ADC should be more accurate.. Also, if the noise requirements is satisfied. If all the changes could be done, then the design would have an outstanding state of the art design in the literature. To have general understanding of the power consumption of the whole system, power distributions among functional blocks is shown in Fig. 93.

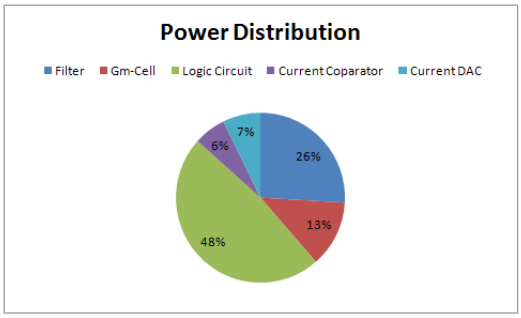

Figure 93: System power distributions

6.2 Monte Carlo and Process Corner Simulation of the Overall System

Since one of the new ideal of this design is to compensate the non linearity of the Gm and non linear DAC. The process corner simulation for THD of the Gm block and the ADC with non linear DAC is presented in Table. 13.

Process Corner	THD(dB)
TT	-46.81
FF	-44.83
SS	-42.32
FS	-45.76
SF	-41.75

Table 13: Process Corner of Gm connected to ADC with non linear DAC.

The THD of FS and SS deviates the most form the THD,-46.81dB at typical corner. The performance at FS and SS corner could be enhance by optimizing the current mirror at the DAC. The results in Table. 13 proves that the Non linear DAC compensate for the non linearity of the Gm block.

Monte Carlo Simulation is done with 5 runs for the overall system in Fig. 85. The number of runs could be increased but the simulation time is very large, in terms of days. These simulation is performed for several reasons. First, to insure that the non linear DAC compensates the non linearity of the Gm-Cell. Second, to insure that there is no or minimum non linearity introduced by the filter and the gm stages. If the THD of the over all system match the THD of the ADC, then the non linear DAC compensates for the non linearity of the gm. In Fig. 94, THD is calculated.

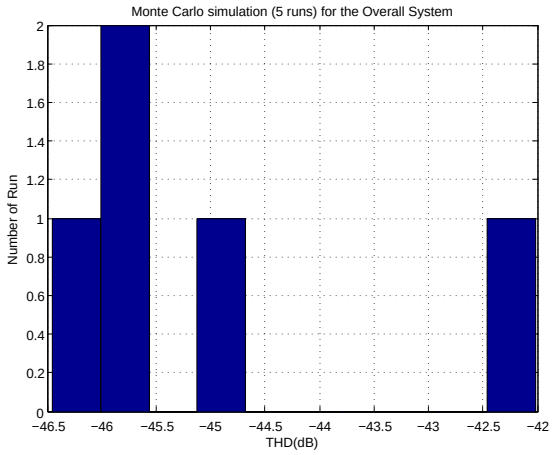

Figure 94: System Monte Carlo Simulation_THD

As show in Fig. 94, the mean value of the THD is -44.936 dB. The mean is only 1.864 dB less than the simulated value.

6.3 Conclusion

The simulations results of the overall system are presented. The performance of each block when they are connected is very close when they are separated. The performance of this designed with otter works is compared. Monte Carlo simulations of the overall system is introduces. Process corner of the Gm block connected with the ADC is presented.

7 Conclusion

A summery of the whole system is introduced. Future recommendations and design contributions is presented at the end.

7.1 Design Summery

The whole system operates in weak inversion. Different design challenges are explored and solved. The proposed design shows improvements in various aspects comparing to other recent works. It achieves the lowest power reported in the literature for ECG applications of 416nW for QRS complex and T wave.The band-pass filter achieves a NEF of 3.3 which very close the lowest reported in the literature 3.26. The THD of the filter is the lowest reported in the literature 0.5%. Choosing the gain to be 20 dB relax the MOS_Pseudoresistor design. To conserve power, a conventional Gm-Cell is designed to converter the voltage to current with lowest power consumption 53nW which is very close to ideal value 51nW. The noise of the gm is negligible. A current SAR ADC is designed to reduce the power consumption. Choosing the input full scale current and controlling the I_DAC controls the power consumptions. Using Current SAR ADC with very low I_DAC current would have the lowest power consumption in the literature. The total power consumption of the whole system is 416nW which is less by 46.5% than the lowest reported 895nW with a comparable FOM,Figure of Merit.

7.2 Future Recommendations & Suggestions

- Programmable Filter could be implemented for different bio-medical signal[33].
- Using the two current branches of the Gm block to have more symmetrical current output.

- Different SAR ADC could be used to increase the linearity.
- Binary weighted or Segmented DAC could be used for higher resolutions ADC. Using different selection strategies reduces the number of current sources which reduced the sources of mismatch and increase the linearity[15].
- Reducing I_DAC in the ADC reduces the power consumption. For example, if I_DAC is 50pA, the power consumption of the ADC would be round 55nW. However, very low voltage current mirror should be design carefully.
- Different SAR Algorithm could be implemented to reduce the number of cycles which reduces the power consumption [65].
- Mismatch in the gm block and DAC to be calibrated or measure through digital circuitry [56].
- Finally, to test the actual functionality of the design, the chip has to be layouted and fabricated to take the measurements.

7.3 Design Contributions

In general, this design explore the area of using current mode system for biomedical applications. The design contributions is listed as fallows:

- Choosing the different design system parameters to meet the requirements of Pacemaker
- Design methodology to choose the required filter types for different applications.
- Choosing filter gain to be 20dB which is different from the rest of the designs 40dB. The DC gain relaxes the MOS_Pseudoresistor design. As

a results, converting MOS connoted diode could be implanted with Vtune without complected design techniques.

- Designing band-pass filter with $0.13\mu M$ which has not been done before. The lowest and most recent is 0.35 μM. Therefore, the chip area is lower.
- Eliminating the gate leakage of the MOS_Pseudoresistor caused by smaller technology by adding current buffer in the OTA.
- Compensating the non linearity of the gm by Tanh current steering DAC which has not be implemented before. The compensation decreases the power consumption while maintaining the same accuracy.
- Design methodology for different types of Data Converters for different applications.
- Current Successive Approximation with ultra low power consumption.
- Power analysis and optimization of the overall system

8 Apppendix

8.1 Matab Code

DAC

```
function [ideal,non_ideal_tanh_mis,non_ideal_tanh]=DAC(nbit,Cu,kk);
% % function [vmis]=DAC(nbit);
mm=[1e-2 0.5e-2 0.1e-2 ] % mismatch persentage
ideal=[];
non_ideal_tanh_mis=[];
non_ideal_tanh=[];
for j=(1:nbit);
er=(mm*randn(1)); %mismatch
C_ideal(j) =((2^(j-1))/(2^(nbit)));
jj1=Cu*(1/2^j);
C_nonideal_tanh_mis(j)=tanh(jj1)+tanh(jj1*er); %Tanh mismatch
jj=Cu*(1/2^j);
C_nonideal_tanh(j)=tanh(jj); %Tanh without Mismatch
end
ideal=[ideal C_ideal]; ideal=ideal(nbit:-1:1);
non_ideal_tanh_mis=[non_ideal_tanh_mis C_nonideal_tanh_mis];
non_ideal_tanh=[non_ideal_tanh C_nonideal_tanh];
```

Comparator & Logic Circuit

```
function [counter,thresholds,bit]=Approx(input,nbit,f_s)
% input= input sample
% nbit= number of converter bits %
f_s= sampling frequency
```

```
%************************************************************
% global variables %
%************************************************************
threshold(1,nbit+1)=0; % threshold array
counter=0; % converter decimal output
Iref=0.5;
threshold(1)=Iref; % 0 threshold t
hreshold(2)=Iref; % first threshold
threshold_id=Iref; % next ideal threshold
in=input;
%************************************************************
for i=2:(nbit+1) % conversion cycle
% thresholds=[ ];
threshold(i) = threshold_id;
%************************************************************
% successive approximation conversion
%************************************************************
if (in-threshold(i)) > 0
threshold_id=(threshold_id)+(1/2^i);
bit=1;
else
threshold_id=(threshold_id)-(1/2^i); bit=0;
end
counter=(counter+bit*2^(nbit-i+1)); %storing
thresholds(i-1)=threshold(i); % storing the value of output
thresholds=[thresholds threshold];
end
```

Calculating SQNR

```
fb=10;
f_s=2*fb; % BW
nbit=8; %simulation trick,
f_in=10.003;
fres= 0.02; % define FFT resolution (kHz)
nr_periods = round(f_in/fres); % simulate a whole number of periods =>
input falls into an FFT bin
%************************************************************************
% Locaate the bins related to the main tone, as well as the inband bins
%************************************************************************
signal_bins=nr_periods ; % pointer to main tone
inband_bins = [1:fb/fres]; % pointer to
inband bins noise_bins = setdiff(inband_bins,signal_bins); % pointer to
noise bins
N =round(nr_periods*f_s/f_in);
fin=antismear(f_in,f_s,N);
in = 0.5+(0.5*sin(2*pi*fin*(1:N)/f_s)); % input signal
[ideal,non_ideal_tanh_mis,non_ideal_tanh]=DAC(nbit);
th_non_ideal_mis=[];
th_non_ideal=[];
th_ideal=[];
for i=1:N % cycle for collect ADC outputs
[counter,thersh]=Approx_DAC(in(i),nbit,f_s,non_ideal_tanh_mis);
[counter1,thersh1]=Approx_DAC(in(i),nbit,f_s,(non_ideal_tanh));
[counter2,thersh2]=Approx_DAC(in(i),nbit,f_s,(ideal));
th_non_ideal_mis= [th_non_ideal_mis thersh(nbit)];
```

```
th_non_ideal= [th_non_ideal thersh1(nbit)];
th_ideal = [th_ideal thersh2(nbit)];
end
y1=y-mean(y);
ffty = (fft(y1)); % compute FFT
inband_power = ffty(inband_bins).*conj(ffty(inband_bins)); %
signal_power = sum(inband_power(signal_bins)); % sum signal power
noise_power = sum(inband_power(noise_bins)); % sum noise power
SNR =10*log10(signal_power/noise_power) % calculate SNR in dB
```

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