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Detection of Series Arcs using Load Side Voltage Drop for Protection of Low Voltage DC Systems

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Abstract—Low voltage dc distribution grids face issues associated with arc faults, aggravated by the absence of current zero crossing. The focus of this work is to comprehensively develop a method of series arc fault detection at the load side power electronics, based on the electrode dependent initial voltage drop occurring at the arc initiation. The proposed arc detection algorithm is described along with the structure and time constants of the designed bandpass filter. The operational boundaries of the arc detection algorithm are defined for copper electrodes depending on the set threshold voltage and the system parameters, like grid inductance, resistance and the load capacitance. Further, the detection time and the zone of guaranteed positive detection are depicted. These are validated through test simulations on the state space model of the system. Finally, experimental validation of the proposed scheme is carried out, wherein, a series arc is generated in the dc circuit and the programmed micro-controller provides a real time signal upon detecting the arcing event. The results on variation in detection time with set threshold voltage is also presented experimentally.

Index Terms—arcs, boundaries, dc, detection, distribution grids, elimination, experimental, faults, low voltage, microgrids, operational, protection, safety, selectivity, series.

I. INTRODUCTION

Modern power utility grids are contemplating an operational shift towards adopting dc microgrids, in order to benefit from the seamless and efficient integration between sources (PV panels, fuel cells), storage (batteries, super-capacitors) and loads (datacentres, electric vehicles (EV), heat pumps) that are predominantly dc in nature or require a intermediate dc conversion stage (wind farms) [1], [2].

Apart from system level efficiency, dc microgrids are favourable because of the high controllability, flexibility and better availability due to easy interconnected meshing without synchronization requirements [1], [3]. However, protection of dc microgrids is less mature and demands greater research attention. Sensitive detection, differentiation and selective clearance of parallel and series dc arc faults is one of the important protection aspects. As compared to ac microgrids, dc distribution systems are more susceptible to sustained arcs due to the absence of current zero crossing [4], [5].

A. Arc Occurrence and Impact in dc Microgrids

Both series and parallel dc arc faults occur in microgrids due to cable wear and tear, short circuits, loose connectors as well

as unintentional unplugging of energized loads by the users. Series arc faults can be dangerous from perspective of failed or delayed tripping of circuit breakers in response to such low current faults [6], causing permanent equipment damage.

DC arc faults may sustain themselves and can be a cause of fire hazards, the probability of which increases as the lifetime of installed dc based systems such as photovoltaic (PV) panels increases [7]. Rapid anticipated evolution in the number of EVs and their synergistic integration with PVs [8] will fuel the rise of dc based nanogrid workplaces. As higher automotive dc network voltages are being preferred more and more, it is observed that the probability of the occurrence of arc faults will become significant [9]. Thereby, unintended unplugging of energized loads will bring the danger of sustained series arcs close to the residential end users.

Performance impact of arc faults at different dc microgrid locations and their implications on controller protection algorithms is explored in [10]. For example, for a constant power load, an input side series arc fault can actually increase the arc current in response to a drop in input voltage [4]. The problem with unintentional unplugging of home appliances in a residential dc distribution system is highlighted in [11].

B. Arc Behaviour, Mitigation Techniques & Their Limitations

Series arcs are created in a network when two electric contacts are pulled apart while conducting current [12]. The inductance in the circuit favours the continuation of current flow which vaporizes the metal at the microscopic contact points just before the electrodes completely separate, thereby creating high temperature, conductive path of metal fumes and electrons. Thus, being essentially a current phenomenon, electric arcs can be created at much lower system voltages as against high voltages required for arc ignition across currentless open contacts [13].

Sustained and stable arcs occur when the arc voltage is lower than the system voltage while enough to maintain a current of 0.5 A [5], [13]. The arc voltage has two components: a) The electrode dependent constant voltage drop of about 11-14 V and b) arc current and electrode gap length dependent channel voltage drop. However, being a stochastic process, high frequency variations in conductivity of arc plasma channel occurs resulting in the high frequency noise signature in the electrical characteristics of the arc [13]. Based on the electrical as well as physical properties, several mitigation techniques exist, that have their own advantages and limitations.

- Based on simple voltage and current measurements at two different locations in the network, a protection zone

is defined [9]. This detection technique can identify series arcing through voltage difference ΔV and parallel arcing with ΔI and is robust towards noise. However, communication requirement is expensive and unreliable.

- Arc faults in 42 V automotive dc networks are detected using current shunt that identifies the rate change of current as an arcing event beyond a set threshold [14]. Apart from being vulnerable to noise, this method is susceptible to system parameters and load current variations.
- Centralized AFCI devices, particularly in PV systems, associate the high frequency (1/f) pink noise signature [15] superimposed on the dc current with arcing. This method cannot provide selective localized action to isolate the fault. It is also vulnerable to other high frequency noise sources like antenna effects, crosstalk and switching noise. Further, series and parallel arcs cannot be differentiated as their noise signature is similar [16].
- Mechanical approaches towards arc mitigation involve specially designed switches that reduce the possibility of arc ignition and also shield the users from the active arc. This method is prone to wear and tear.
- Acoustic detection is proposed for large battery systems [17]. It is shown that there is no specific frequency signature, which extends from 20 to 200 kHz and is vulnerable to other audible noises in the environment. Therein, the time signature is used to identify arcing. However, the performance is sensor dependant. In localized areas such as switchboards where arcing is expected, acoustic methods maybe used [18].
- Optical detection of arc flashes is proposed as a rapid detection method [19]. It is highlighted that detection can be as fast as 1 ms and tripping can be within 2 ms if a dedicated solid state breaker is used. However, this scheme needed secondary information such as over-current in order to avoid spurious triggering from surrounding light. For series arcs, this is not possible because variation in current is minimal.

Discussing on available arc detection technologies, including optical, pressure, temperature and current based sensing [20], it is noted that no single scheme can address all safety concerns. This is particularly true for series arcing.

In a previous work, we proposed a novel series arc extinction scheme based on monitoring the load voltage for a sudden drop of a specific electrode dependent magnitude associated with a series arcing event [4]. A refined algorithm was further developed in [21]. Limitations of the scheme, particularly its dependence on system parameters, was highlighted in [22]. Authors had concluded that the boundary of positive detection, detection time and set points must be clearly defined in future work. Experimental validation of the developed concept by showing real time arc detection was recognized to be important.

C. Research focus and Contributions

The focus of this work is to develop a protection application in low voltage dc (LVdc) microgrids in order to mitigate the problems related to series arcing by performing load-side voltage drop detection using the power electronic device at the load-side. The proposed method is robust towards both low and high frequency noise and is able to provide a selective action. With proper coordination with central high frequency noise signature based AFCI devices, differentiation between series and parallel arcs can also be achieved.

The following research objectives are addressed in this publication:

- Determining the set-point for threshold detection voltage ensuring sensitivity while avoiding spurious triggering due to low frequency grid voltage fluctuations.
- Obtaining insight on the detection time and its variation with threshold voltage and circuit parameters.
- Defining the operational boundaries of the arc detection algorithm depending on the system parameters like grid inductance, resistance and the load capacitance.
- Validating that the algorithm successfully operates in practice by carrying out real time experimental detection of series arcs.

Section II gives a background of the designed algorithm proposed for detecting and extinguishing series arcs using load side power electronics.

In Section III, a detection map is developed by simulating the interplay of varying grid parameters and set threshold voltages. For obtaining conservative results, the input that is representative of worst case arc characteristics is chosen. Insight on detection time is offered and boundary of positive detection is defined. To gain trust on the obtained boundaries, test simulations and experimental detection results are offered for arcing constant power loads.

Section IV validates the developed scheme through real time series arc detection on the designed experimental set up. Insight into sensitivity with threshold detection voltages as well as speed of detection is offered through measurements.

Finally, the key contributions of the paper are summarized in Section V and the main quantified findings are reiterated.

II. BACKGROUND ON THE DESIGNED DETECTION SCHEME

The proposed series arc detection algorithm monitors the load voltage V_{load} depicted in the equivalent circuit in Fig. 1 (a). When an arc is initiated, a voltage drop occurs at the load side as shown in Fig. 1 (b). This is a response corresponding to the initial arc voltage injected in the circuit as a step input. The stochastic initial arc voltage is dependent on the electrode material. For copper electrodes, the mean value is empirically determined to be about 13.3 V [23], [24].

The delayed build up, oscillatory behaviour and overshoot in the load voltage observed in Fig. 1 (b) is due to the presence of inductance and capacitance in the circuit. In fact the magnitude of circuit parameters can strongly influence the response of load voltage to the arc voltage step drop, thereby affecting the performance of the designed detection algorithm, which is discussed in Section III.

The flow diagram depicting the proposed series arc detection algorithm is shown in Fig. 1 (c). The bandpass filter is designed with time constants such that spurious triggering corresponding to the variations in load voltage is avoided. These variations can be associated with:

(a)

(b)

$\tau_s = 1\ ms$
$\tau_f = 0.1\ ms$ } 150-1.5 kHz

(c)
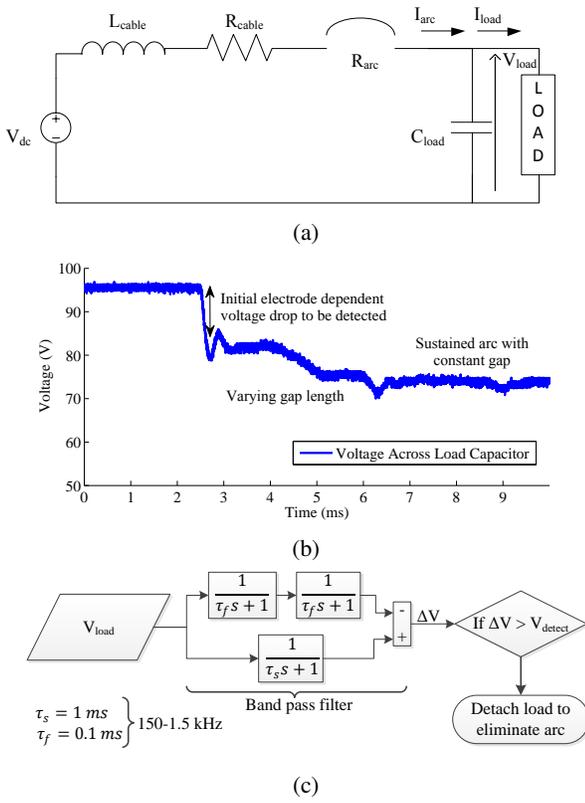
Fig. 1: Series arc detection scheme explained with a) Equivalent circuit with single constant resistance load b) Load voltage measurement during arcing event c) Flow diagram for proposed algorithm.

1) Low frequency grid voltage fluctuations due to load variations.
2) High frequency switching noise.

A complete experimental design of the bandpass filter, choice of time constants (150 Hz-1.5 kHz) & its cascaded structure to maximize the signal to noise ratio while attenuating the undesired frequency components is developed in [21].

The step change corresponding to the sudden electrode dependent series arc voltage is reflected in the load voltage based on the R-L-C circuit parameters. The frequency components of this step input, residing within the sensitive spectrum of the bandpass filter is detected and compared with the set threshold voltage to identify the arcing event. The threshold value determines the speed of detection (higher the threshold, greater the detection time) and also on whether the series arc can positively be detected successfully for the corresponding circuit parameters.

III. OPERATIONAL BOUNDARIES FOR CIRCUIT CONFIGURATIONS AND SET PARAMETERS

This section develops the frequency domain sensitivity analysis to determine the response of the designed algorithm under varying grid conditions. Further, the zone of positive detection is defined while obtaining adequate insensitivity to low frequency grid voltage fluctuations and high frequency switching noise.

A. Dependence on Arc Characteristics

The response of the algorithm is highly dependant on the arc characteristics. Apart from being stochastic, the electrical characteristics of the arc are dependent on electrode material, separation speed, current and gap length as shown in Fig. 2. Interpolation is used between empirically determined arc voltage points from arc current and gap length defined in [24].
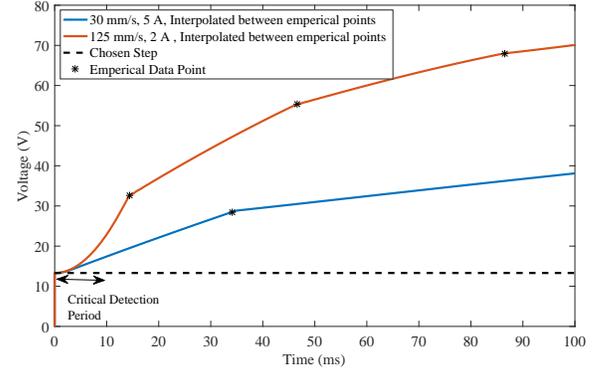
Fig. 2: Choice of arc response for defining detection boundaries.

A lower arc current and a faster electrode separation would ensure greater injected arc voltage and thereby result in a higher load voltage drop. The "critical detection time" is defined as the time range in which the detection algorithm is expected to operate (less than 10 ms). We chose a step of 13.3 V to define the operational boundaries, which reflects the worse case scenario. This is because the arc voltage is a summation of this initial electrode dependent voltage and the voltage component due to arc channel resistance, which is dependent on gap length and circuit current. If the designed algorithm is able to detect this step, it will be able to provide positive detection for any current and gap speed magnitude, thereby ensuring that the defined boundaries are as conservative as possible.
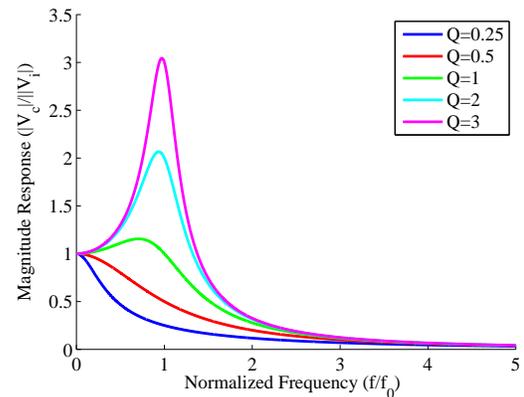
Fig. 3: Magnitude response of load side voltage for different grid inductance and input capacitance values.
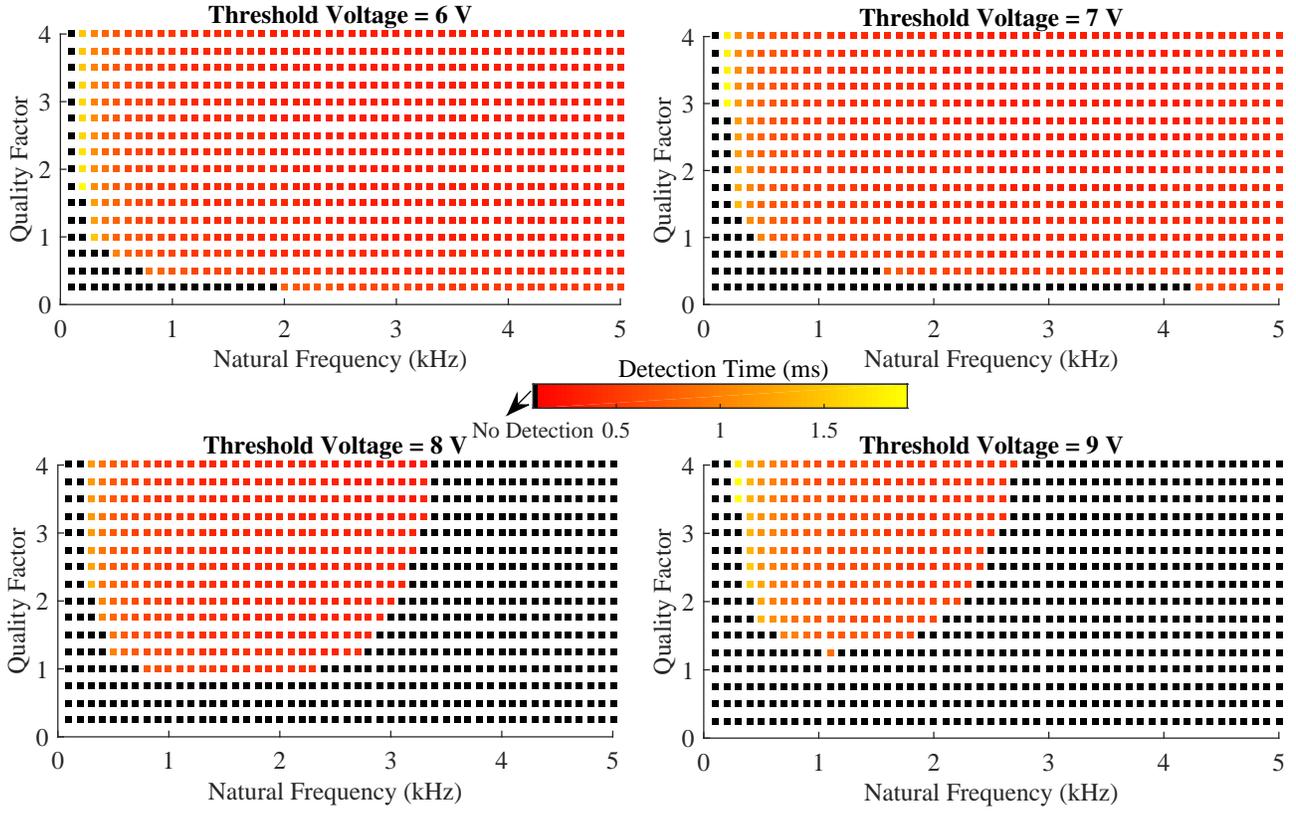
Fig. 4: Detection time for minus 13.3 V step in input with varying circuit quality factor and natural frequency.

B. Dependence on Grid Parameters

The magnitude response of the load side voltage (V_{load}) for the equivalent circuit of Fig. 1(a) with varying inductance and capacitance is depicted in Fig. 3.

The cut-off voltage and magnitude response depend on the natural frequency ($f_0 = \frac{1}{2\pi\sqrt{LC}}$) and the damping factor ($\alpha = \frac{R}{2L}$). The magnitude response of the load side voltage (V_{load}) to input voltage (V_{dc}) corresponding to Fig. 1 (a) is given by (1). Herein, the frequency of input is $\omega = 2\pi f$, natural frequency is $\omega_0 = 2\pi f_0$ and the quality factor Q is given by $\frac{\omega_0}{2\alpha}$.

$$\frac{|V_{\text{load}}|}{|V_{\text{dc}}|} = \frac{1}{\sqrt{\left(1 - \left(\frac{\omega}{\omega_0}\right)^2\right)^2 + \left(\frac{\omega}{Q\omega_0}\right)^2}} \tag{1}$$

It can be observed that above the natural frequency, the magnitude gets attenuated and the step response to an event such as arcing will contain the frequency spectrum which is below this value. It is also worth noting that with lower Q factor corresponding to higher damping resistance, attenuation is also observed for frequencies below the cut off point.

With increase in quality factor $\left(Q = \frac{1}{R}\sqrt{\frac{L}{C}}\right)$, the maximum voltage computed at the output of discrete bandpass filter increases when the natural frequency is close to the frequency bandwidth of the filter [22].

In the subsequent subsection, the impact of the attenuation of chosen step on the designed algorithm output is simulated to develop a map depicting the detection speed and reliability for different threshold set-points for varying circuit parameters. This map will be used to define the operating boundaries of the detection scheme.

C. Detection Map for Varying Configurations

Fig. 4 shows the detection time for minus 13.3 V step in input for different threshold voltages with filter bandwidth of 150 Hz-1.5 kHz. The black regions show the simulation points where no arc can be detected for the corresponding set threshold value. Herein, the quality factor was varied from 0.25 to 10 in steps of 0.25 and frequency was varied from 100 Hz to 10 kHz in steps of 100 Hz. Following can be observed:

- The detection time decreases with increasing natural frequency until it saturates to a low value towards the outer limit of the filter band.
- At very low natural frequency, there is no detection for any quality factor or set threshold voltage because the circuit attenuates the higher frequencies where the filter is sensitive. Further, the bandpass filter itself is designed to attenuate below 150 Hz.
- For very low quality factor (much less than 1), there is no detection when the natural frequency is within the range of filter bandwidth due to the high damping effect depicted in Fig. 3. For very high frequencies, this damping effect is pushed outside the frequency spectrum to which the bandpass filter is sensitive, while the step signal components in the frequency spectrum for detection is not affected.

- With higher set detection threshold voltage, the detection boundary confines around the natural frequencies corresponding to the filter bandpass. Threshold voltages of 8 V and 9 V are detected in this region due to the amplifying effect of a quality factor greater than unity. In other words, the boundaries for these thresholds are a result of interaction of filter attenuation and the amplification/damping of the specific frequency components of the step input about the natural frequency based on the quality factor.
- Threshold voltage of 6 V and 7 V is detectable for a wide range of frequency spectrum and quality factors. This is because the signal components of 13.3 V step within the frequency spectrum of the bandpass filter add up to a value greater than 7 V. In other words, amplifying effect of quality factor greater than unity is not needed to reach the threshold and also there is some margin to accommodate damping when the quality factor is below unity.

Hence, threshold voltage of 6 V is the most favourable to ensure arc detection for varied grid inductances and load side capacitances. Making the detection sensitive when the natural frequency is below 150 Hz is not possible, because we want to avoid spurious triggering due to grid side voltage fluctuations at this frequency and the bandpass filter is designed to cater to this need.

Insensitivity to arc detection when quality factor is very low and the natural frequency lies with the frequency spectrum of filter can be avoided by setting the threshold voltage lower than 6 V. However, this decision must be taken after careful consideration to avoid spurious triggering due to noise in the system. In the subsequent section, the boundaries of guaranteed positive detection are defined for a set threshold of 6 V so as to ensure that the magnitude of critical quality factor and natural frequency is not violated.

D. Boundary for Maximum Load Capacitance

Fig. 5 shows the stringent boundary of operation for a set threshold of 6 V, depicting the zone of guaranteed positive detection (green) for the maximum load capacitance value corresponding to the grid inductance independent of the resistance magnitude.

In other words, if the capacitance in the load side power electronics is lower than the depicted maximum, then the designed algorithm will always detect the arc for the corresponding grid inductance irrespective of the circuit quality factor.

As the quality factor of the R-L-C circuit increases, the zone of positive detection increases, as depicted in Fig. 6. This is due to the fact that the load voltage is less attenuated by the R-L-C circuit in the sensitive frequency spectrum.

E. Testing the Validity of Defined Boundaries

Different dc arc models are discussed in [24]–[27]. The complete state space model developed in [4], [22] along with the designed algorithm [21] was simulated to test the
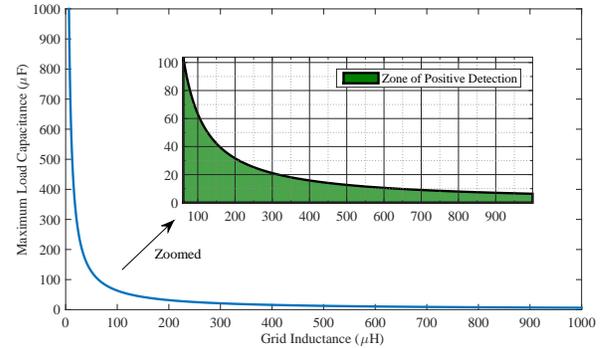
Fig. 5: Resistance independent positive detection boundary for maximum input load capacitance with varying grid inductance for a set threshold of 6 V.
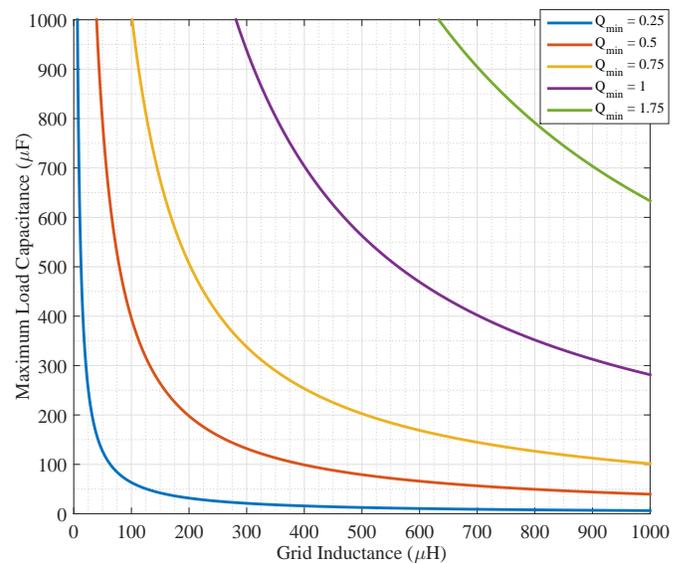
Fig. 6: Boundary for maximum load capacitance with varying grid inductance and quality factor for a threshold of 6 V.

theoretical validity of the defined boundaries as shown in Fig. 7.

Comparing Fig. 6 and Fig. 7, it can be observed that for $200 \, \mu H$ grid inductance and 0.5 quality factor, the former conservatively predicts the load capacitance detection boundary at $200 \, \mu F$ for a 6 V threshold. The actual simulations in the latter figure show that positive detection is achieved until $300 \, \mu F$, above which the detection fails. This proves that the defined boundaries are conservative estimates as expected while choosing the step input that would make dependence on arc current and electrode gap length irrelevant.

Along with the mathematical exercise of defining conservative boundaries, it is important to gain insight on the physics in order to understand what to expect when the detection fails.

- The theory predicts that with higher load capacitance, there is a greater chance of failed detection. However, higher load capacitance also decreases the chance of sustained series arcs. While this can be an added benefit, apart from good inertia and stability in the dc microgrid,
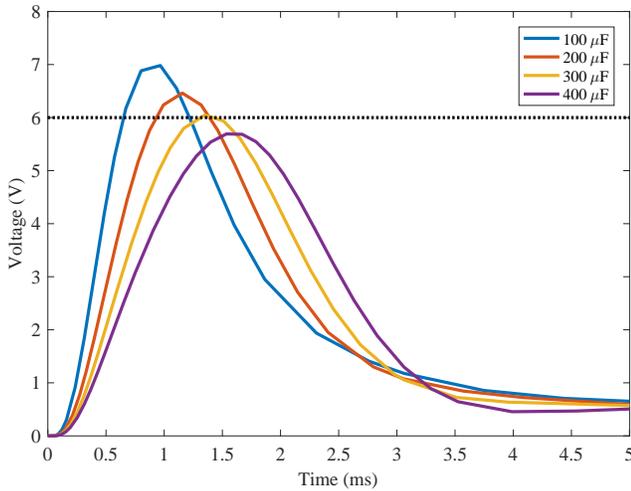
Fig. 7: Simulation results of algorithm output for series arcing in R-L-C circuit with quality factor of 2 and inductance of $200\,\mu$H with increasing load capacitance.

Fig. 8: Detection algorithm offline output to a measured series arcing event in a constant power dc lamp.

high capacitance has protection issues, particularly during short circuit faults.

- Higher grid inductance is generally accompanied by increase in resistance that inevitably leads to a lower quality factor. This not only leads to failed detection, but also, sustained arcs are much more probable due to greater inductance. Therefore, long link lengths or extremely high supply converter output inductance should be avoided.

Response of the designed algorithm to measured load voltage data is also important. A series arcing instance measured for a 700 V, 1 kW constant power dc lamp supplied through a noisy supply and an inductance of $100\,\mu$H is shown in Fig. 8.

A typical 300 Hz noise signature corresponding to a 6 pulse rectifier is observed, which is removed using an additional notch filter designed in [21]. The offline algorithm response to the load voltage data is depicted and indicates that a set threshold of 6 V would provide a positive detection, while a value above 8 V would fail to trigger, as predicted.

The constant power dc lamp was a hardware blackbox which offered no flexibility in choosing the load capacitance, voltage and current. The subsequent section aims at further exploring the robustness and speed of the designed algorithm in a controlled lab setup by obtaining real time detection signals to series arcs created in circuits with known operating parameters.

IV. REAL TIME SERIES ARC DETECTION EXPERIMENTS

In order to validate the proposed detection scheme, experiments were conducted by introducing series arcs in dc circuits with different supply voltages. The designed algorithm was programmed into the micro-controller and the set threshold detection voltage magnitude was varied. Upon series arc introduction, real time detection signal obtained from the controller was analyzed under different scenarios.
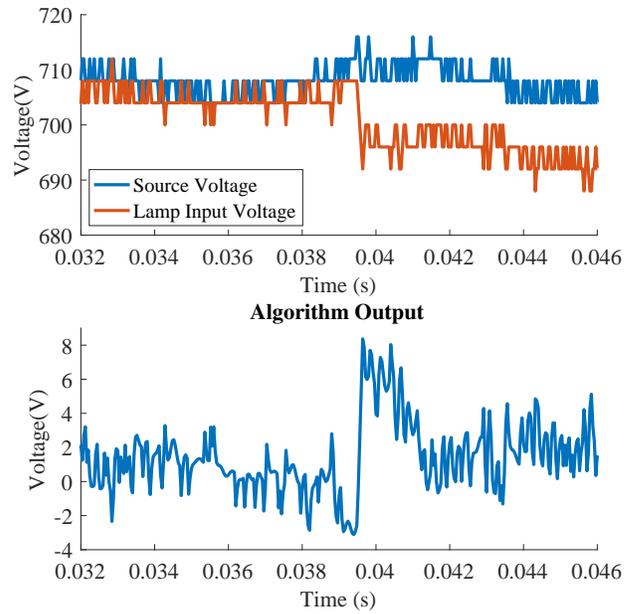
A. Experimental Setup

The equivalent circuit corresponding to the setup is shown in Fig. 1 (a). Fig. 9 depicts the experimental setup developed to validate the proposed series arc detection scheme in real time.
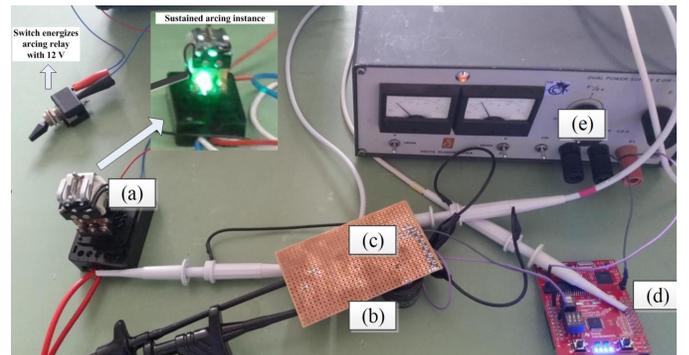
Fig. 9: Experimental setup for real time arc detection.

(a) A D-series 12 V Smitt relay is energized with a manually operated switch to create a series arc in the circuit. A sustained arcing instant is illustrated in Fig. 9. Designed maximum gap length is 0.7 mm for gold plated electrodes with calculated contact separation speed of 125 mm/s [4]. Detailed information on the relay can be found in relevant datasheet. Considering that gold plate has a higher voltage drop than copper, the electrodes were coated with tin that has an initial arc voltage lower than copper, with new maximum gap length of about 0.5 mm. It is more difficult to obtain positive detection with this lower initial tin electrode dependent arc voltage. Therefore, it can be

inferred that if detection is obtained for tin coating, a faster detection can be obtained for copper electrodes with all other conditions kept the same. A sample measurement describing the electrical characteristics of the generated arc is shown in Fig 10.
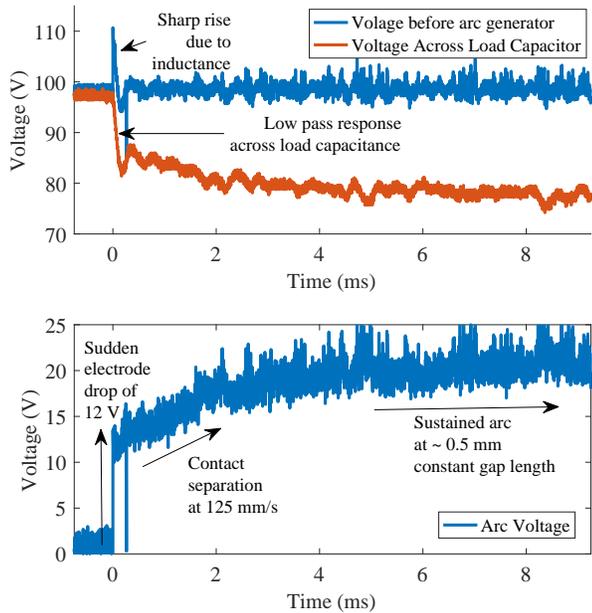
Fig. 10: Measured arc characteristics for source inductance of $100\,\mu$H and load capacitance of $30\,\mu$F.

Observe that the applied tin coating has a electrode dependent initial voltage drop of 12 V, which is lower than 13.3 V for that of copper electrodes considered in the theoretical section of this paper.

(b) Two different types of dc sources are used in series with a $100\,\mu$H output inductance. One is a 50 V 0-10 A constant voltage dc supply used to create 48 V, 8 A for experiments for constant power loads. For experiments with 100 V, 5 A, two of these are connected in series. Voltage across this source is observed to be highly stable. Second is a 600 V, 2.7 A dc supply with ability to operate in constant voltage or constant current mode. We operate it as 400 V, 2.5 A constant voltage mode supply to the constant resistance load. The supply voltage is observed to fluctuate with load changes.

(c) During series arc experiments with constant power dc load, an electronic load of 400 W, 400 V, 25 A rating is used. For constant resistance operation, load resistance connected in parallel with a $30\,\mu$F capacitor is used with a rating of 5.4 A.

(d) The voltage divider of 1000/3.3 V is used for sensing the load voltage across the capacitor.

(e) Measured input is provided to the Pin 'ADCINA0' of the analog to digital converter of the micro-controller LAUNCHXL-F28027 C2000 Piccolo LaunchPad Experimenter Kit

The detection algorithm depicted in Fig. 1 (c) is burnt into the controller. When the output of the programmed series arc detection algorithm is greater than the set threshold magnitude, a trigger signal is provided to the output pin 'GPIO3' which triggers the oscilloscope.

B. Experimental Results for Constant Power Load

In order to create conditions conducive for obtaining series arcs, high current and voltage is needed, which is constraint by the 400 W dissipation capacity of the load. We empirically observed that possibility of arcing was a stronger function of current and chose 48 V and 8 A steady state operation for our measurements. Fig. 11 shows that the designed algorithm positively detects the series arcing event in real time.
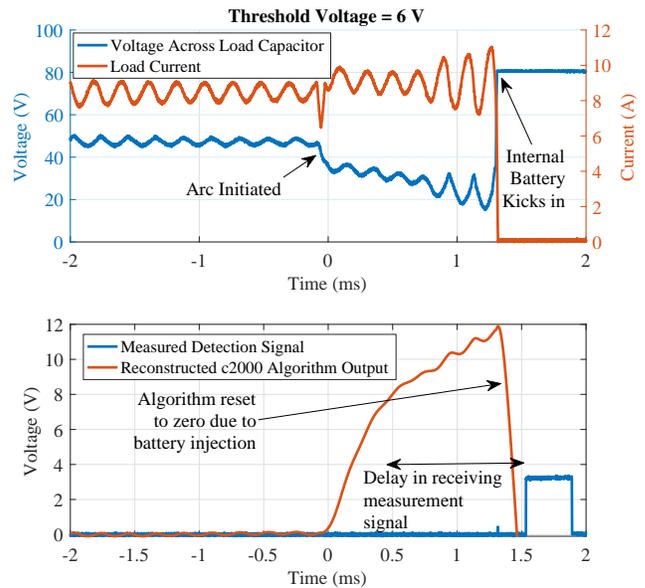
Fig. 11: Real time arc detection for series arcing with constant power load for a 6 V threshold voltage.

It can be observed that the trigger from micro-controller was obtained in about 1.5 ms of arc initiation for a set threshold voltage of 6 V. Generating sustained arcs was difficult due to 400 W rating constraint of the available electronic load, which limited our supply voltage to 48 V. While trying to increase the source inductance beyond $100\,\mu$H to aid arcing, the load operation became noisy. The option of lowering the load capacitance in order to obtain sustained arcs was not available. Therefore, while the proof of concept is experimentally depicted, sensitivity analysis cannot be carried out with this load.

When the internal battery kicks in, the load capacitor voltage increases and no longer reflects the drop corresponding to the series arc. Since our algorithm is sensitive to a drop in voltage, the increase in monitored voltage will mean that its harder for it to trigger. In other words, if we obtain a positive detection signal in spite of the internal battery, it can be concluded that we would get an equivalent or faster detection had the battery not kicked in. The reconstructed internal working of the algorithm depicts this in Fig. 11.
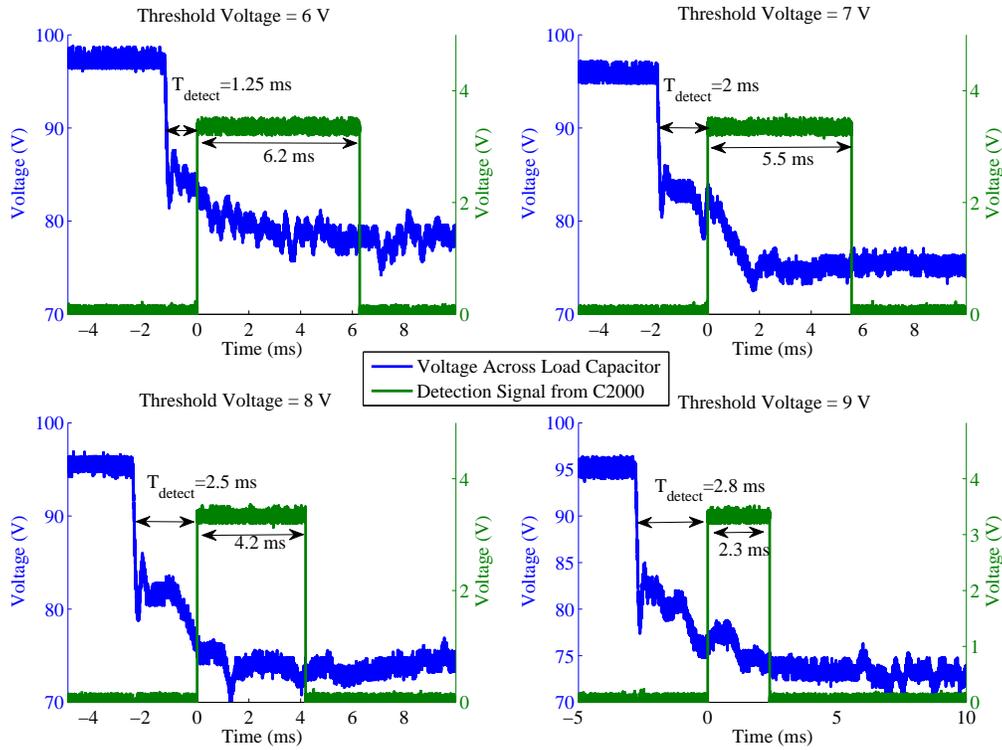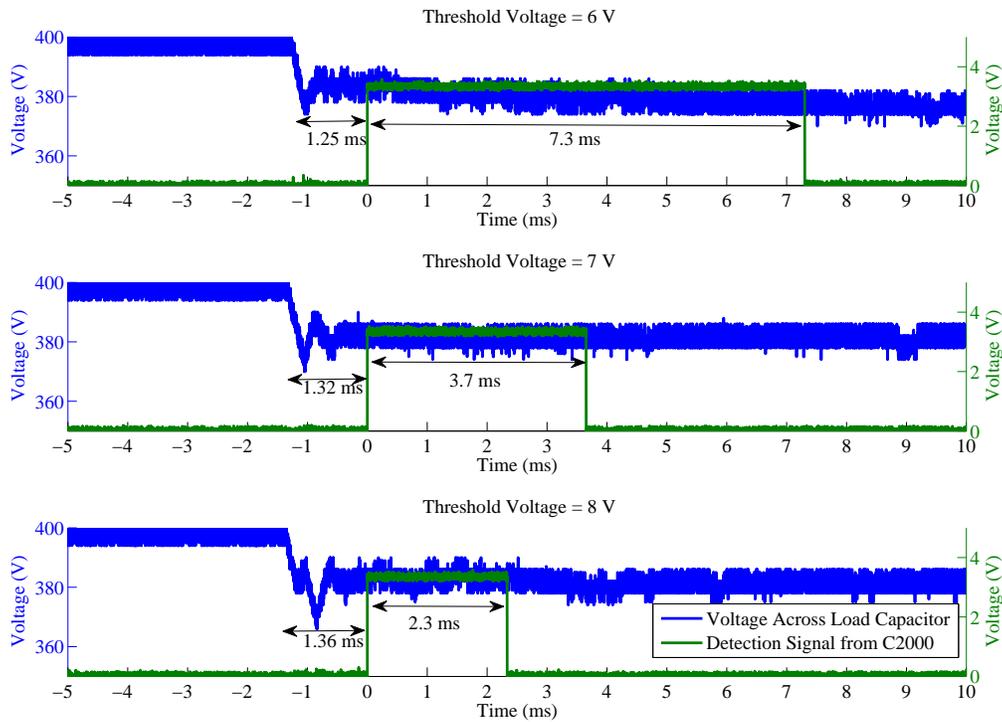
Fig. 12: Real time arc detection for a; a) 100 V supply with 5 A load current b) 400 V supply with 2.5 A load current.

It can be seen that the internal battery of the load kicks in when current goes too low and extinguishes the arc. Due to this reason, obtaining a slower detection by choosing a higher threshold voltage was rendered impossible. Therefore, in order to obtain greater flexibility in controlling the experimental set-up, constant resistance load was chosen for the sensitivity analysis.

From simulations in [4], it can be seen that the dynamics of load voltage in response to a series arcing event is similar for both constant power and constant resistance load, particularly in the first few ms. Physically, it can be derived that voltage drop will be greater for constant power loads considering that they attempt to deliver the same power, while the power output drops with load voltage in case of constant resistance loads, thereby discharging the capacitor less. This translates to the inference that under similar conditions, if series arcs are detectable for constant resistance loads, they can be detected with constant power loads as well.

C. Experimental Results for Constant Resistance Load.

A series of experiments with real time arc detection with varying threshold detection voltages were performed on 100 V and 400 V supplies; results are plotted in Fig. 12 (a) and Fig. 12 (b) respectively.

The following is observed for each set of experiments:

- The detection time is within few milliseconds, and increases with increasing set threshold detection voltage. For a 6 V set threshold, the detection is rapid, at about 1 ms.
- The pitch of the signal, which is the duration when the controller output pin is high at '1', indicates the sensitivity of the algorithm. Decreasing pitch as the set threshold voltage increases indicates a decreasing sensitivity.
- Detection time does not correlate for different supply voltages because different supply systems were used in each case. The 100 V supply did not fluctuate much and was more stable than the 400 V supply. It can be observed that the variation profile of load voltage in response to series arc is different in these two situations, thereby resulting in different detection time.

V. CONCLUSION

It is proved that the set threshold voltages of 6 V and 7 V are sensitive in detecting series arcing for a wide range of natural frequencies and quality factors of the system configuration. Set thresholds of 8 V or more are sensitive only due to the amplifying effect of the circuit within the frequency spectrum of the designed bandpass filter of the detection algorithm. It is highlighted that 6 V is the best choice because it is more sensitive in the regions of interest, while being insensitive to low frequency grid voltage fluctuations associated with load changes at 100 Hz.

The detection time decreases with increasing natural frequency of the circuit until it saturates to a low value towards the outer limit of the filter band. The detection time dt of the algorithm varies between $0 < dt \leq 3$ ms depending on the circuit parameters like grid inductance, resistance and load

capacitance mapped in the natural frequency in the range of 100 Hz -5 kHz and quality factors in the range of 0.25-4.

The zone of positive detection of series arcs by the algorithm is defined comprehensively for all load capacitance and grid inductance. For example, for a 100 μH inductance, the load capacitance should be lower than 60 μF to ensure positive detection if we do not take resistance into account. This limitation is improved to 400 μF with a higher quality factor of 0.5 and >1000 μF for quality factor of 1. Therefore, it is concluded that the zone of positive detection increases with quality factor for the same grid inductance due to its amplifying and attenuating effect on the arc detection signal. The boundaries are defined for copper electrodes and will theoretically hold for any electrode material that has an initial arc voltage drop greater than 13.3 V.

The detection scheme works in real time for both constant power and constant resistant loads for different supply voltage and load currents. Experimental results show that series arcs can be detected in about 1 ms after initiation for a set threshold of 6 V. The detection time increases with increasing set threshold voltage, while the sensitivity decreases. It is also observed that the detection time and sensitivity of the scheme was slightly different for different supply devices used because of their own source dynamics to the arcing event. It seems reasonable to conclude that 1-3 ms is the empirical detection time range and 6 V is a good set point for positive arc detection both theoretically and practically.

REFERENCES

[1] H. Kakigano, Y. Miura, and T. Ise, "Low-voltage bipolar-type dc microgrid for super high quality distribution," *IEEE Transactions on Power Electronics*, vol. 25, no. 12, pp. 3066–3075, Dec 2010.

[2] K. Strunz, E. Abbasi, and D. N. Huu, "Dc microgrid for wind and solar power integration," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 1, pp. 115–126, March 2014.

[3] A. Kwasinski, "Quantitative evaluation of dc microgrids availability: Effects of system architecture and converter topology design choices," *IEEE Transactions on Power Electronics*, vol. 26, no. 3, pp. 835–851, March 2011.

[4] L. Mackay, A. Shekhar, B. Roodenburg, L. Ramrez-Elizondo, and P. Bauer, "Series arc extinction in dc microgrids using load side voltage drop detection," in *2015 IEEE First International Conference on DC Microgrids (ICDCM)*, June 2015, pp. 239–244.

[5] A. Shekhar, "Detection, characterization and extinction of electric arcs in dc systems," *TU Delft, Delft University of Technology*, 2015.

[6] X. Yao, L. Herrera, S. Ji, K. Zou, and J. Wang, "Characteristic study and time-domain discrete- wavelet-transform based hybrid detection of series dc arc faults," *IEEE Transactions on Power Electronics*, vol. 29, no. 6, pp. 3103–3115, June 2014.

[7] T. Zgonena, L. Ji, and D. Dini, "Photovoltaic dc arc-fault circuit protection and ul subject 1699b," *Photovoltaic Module Reliability Workshop*, 2011.

[8] G. C. Mouli, P. Bauer, and M. Zeman, "System design for a solar powered electric vehicle charging station for workplaces," *Applied Energy*, vol. 168, pp. 434 – 443, 2016.

[9] T. J. Schoepf, M. Naidu, and S. Gopalakrishnan, "Mitigation and analysis of arc faults in automotive dc networks," *IEEE Transactions on Components and Packaging Technologies*, vol. 28, no. 2, pp. 319–326, June 2005.

[10] X. Yao, L. Herrera, and J. Wang, "Impact evaluation of series dc arc faults in dc microgrids," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2015, pp. 2953–2958.

[11] J.-Y. Jeon, J.-S. Kim, G.-Y. Choe, B.-K. Lee, J. Hur, and H.-C. Jin, "Design guideline of dc distribution systems for home appliances: Issues and solution," in *2011 IEEE International Electric Machines Drives Conference (IEMDC)*, May 2011, pp. 657–662.

[12] P. Slade, *Electrical Contacts - Principles and Applications.* Marcel Dekker, Inc., 1999.

[13] C. Strobl, "Arc fault detection in dc microgrids," in *2015 IEEE First International Conference on DC Microgrids (ICDCM)*, June 2015, pp. 181–186.

[14] M. Naidu, T. J. Schoepf, and S. Gopalakrishnan, "Arc fault detection scheme for 42-v automotive dc networks using current shunt," *IEEE Transactions on Power Electronics*, vol. 21, no. 3, pp. 633–639, May 2006.

[15] J. Johnson, B. Pahl, C. Luebke, T. Pier, T. Miller, J. Strauch, S. Kuszmaul, and W. Bower, "Photovoltaic dc arc fault detector testing at sandia national laboratories," in *2011 37th IEEE Photovoltaic Specialists Conference*, June 2011, pp. 003 614–003 619.

[16] J. Johnson, M. Montoya, S. McCalmont, G. Katzir, F. Fuks, J. Earle, A. Fresquez, S. Gonzalez, and J. Granata, "Differentiating series and parallel photovoltaic arc-faults," in *2012 38th IEEE Photovoltaic Specialists Conference*, June 2012, pp. 000 720–000 726.

[17] V. Cattin, P. Perichon, J. Dahmani, B. Schwartzmann, and V. Heiries, "Detection of electric arcs in large batteries," in *2013 World Electric Vehicle Symposium and Exhibition (EVS27)*, Nov 2013, pp. 1–9.

[18] C. S. Maroni, R. Cittadini, Y. Cadoux, and M. Serpinet, "Series arc detection in low voltage distribution switchboard using spectral analysis," in *Proceedings of the Sixth International Symposium on Signal Processing and its Applications (Cat.No.01EX467)*, vol. 2, 2001, pp. 473–476 vol.2.

[19] J. A. Kay and L. Kumpulainen, "Maximizing protection by minimizing arcing times in medium-voltage systems," *IEEE Transactions on Industry Applications*, vol. 49, no. 4, pp. 1920–1927, July 2013.

[20] D. C. Mohla, T. Driscoll, P. S. Hamer, and S. A. R. Panetta, "Mitigating electric shock and arc-flash energy: A total system approach for personnel and equipment protection," *IEEE Industry Applications Magazine*, vol. 18, no. 3, pp. 48–56, May 2012.

[21] A. Shekhar, L. Mackay, L. Ramírez-Elizondo, and P. Bauer, "Experimental design of a series arc load side detection algorithm for dc microgrid protection," in *2016 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM)*, June 2016, pp. 343–347.

[22] A. Shekhar, L. Mackay, L. Ramirez-Elizondo, and P. Bauer, "Dc microgrid protection by selective detection of series arcing using load side power electronic devices," in *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, Sept 2016, pp. 1–9.

[23] J. Li, D. W. P. Thomas, M. Sumner, E. Christopher, and Y. Cao, "Series arc fault studies and modeling for a dc distribution system," in *2013 IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC)*, Dec 2013, pp. 1–6.

[24] R. F. Ammerman, T. Gammon, P. K. Sen, and J. P. Nelson, "Dc-arc models and incident-energy calculations," *IEEE Transactions on Industry Applications*, vol. 46, no. 5, pp. 1810–1819, Sept 2010.

[25] J. Paukert, "The arc voltage and arc resistance of lv fault arcs," *Proc. 7th Int. Symp. Switching Arc Phenom.*, p. 4951, 1993.

[26] K. Sawa, M. Tsuruoka, and S. Yamashita, "Fundamental arc characteristics at dc current interruption of low voltage(<500 v)," in *ICEC 2014; The 27th International Conference on Electrical Contacts*, June 2014, pp. 1–6.

[27] F. M. Uriarte, A. L. Gattozzi, J. D. Herbst, H. B. Estes, T. J. Hotz, A. Kwasinski, and R. E. Hebner, "A dc arc model for series faults in low voltage microgrids," *IEEE Transactions on Smart Grid*, vol. 3, no. 4, pp. 2063–2070, Dec 2012.

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