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Comparison of Pulse Current Capability of Different Switches for Modular Multilevel Converter-based Arbitrary Wave shape Generator used for Dielectric Testing of High Voltage Grid Assets

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Keywords

≪Pulse Current Capability≫, ≪Si and SiC Device Technologies≫, ≪Modular Multilevel Converter≫, ≪Dielectric Testing of Grid Assets≫

Abstract

This article compares the pulse current capability of various Semiconductor (SM) device technologies for Modular Multilevel Converter (MMC)-based High Voltage (HV) Arbitrary Waveform Generator (AWG) for dielectric testing of grid assets to find the most suitable SM device technology which can perform well in generating lightning impulse that demands a high peak current for a relatively short time. For the typical HV loads of the AWG, Lightning Impulse (LI) test may require a pulse current to rise to 1.7 kA in 0.2 µs. It is essential to highlight that most other dielectric tests performed with an HV AWG demand a relatively low current such as less than 10 A. Therefore, TO-packaged semiconductors would be well-suited for a large number of tests other than short impulses. To optimize the size and cost of the HV AWG, this paper evaluates the pulse current capabilities of TO-packaged semiconductors for the above-mentioned current requirement to generate LI waveform. The first comparison is made among Non-Punch Through (NPT) Si IGBT, Field Stop (FS) Si IGBT, Si MOSFET, and SiC MOSFETs with roughly the same current rating of 40 A. It is found that the Si MOSFET gives the fastest rise time of 0.42 µs and the NPT IGBT gives the highest current amplification factor of almost 12 times greater than its own rated current. However, 3rd Generation SiC MOSFET combines Si MOSFET and NPT IGBT capabilities to generate a fast rise time and high peak pulse current. Additionally, the FS IGBT is compared with the SiC MOSFET. The SiC MOSFET performs better in peak current capability and the obtained rise time. All in all, the research results and the stringent HV AWG requirements for LI show that the application requires a relatively complex switch implementation with far superior current capability than in normal operation. Therefore, a parallel connection of several TO-packaged devices is necessary to generate LI from MMC-based HV AWG.

Introduction

Medium Voltage (MV) and High Voltage (HV) equipment such as transformers, switchgear, and cables in the electrical power system are experiencing new and more severe electrical stresses due to the rise of Distribution Generation (DG) systems and large-scale renewable energy integration by power electronic

converters [1][2][3]. For the reliable operation of the current and future electrical power system, MV and HV equipment need to be tested with electric stresses with complex wave shape such as the superposition of impulse waveforms with AC and DC, as shown in Fig. 1. Currently, these waveforms are generated using a superimposed circuit as shown in Fig. 2 [3]. On right side of the figure, the impulse generator or Marx generator is shown which can generate impulse waveforms with varied rise time ranging from 1 µs to 250 µs and tail time ranging from 50 µs to 2500 µs. The left side of the Fig. 2 can be either the transformer or rectifier circuit to generate the AC or DC part from the voltage waveforms as shown in Fig. 1(a) and (b) [2][3]. This arrangement needs to be customized and tuned for one particular test. Hence, generating such complex waveforms is a time-consuming process. Additionally, the third waveform depicted in Fig. 1(c) consists of AC, DC, and impulse [1][4], requiring three different test sources to generate the desired waveform, increasing the complexity even further. Therefore, a Modular Multilevel Converter (MMC)-based Arbitrary Wave shape Generator (AWG) is proposed in [4] which can generate all exemplary testing waveforms by itself and its schematic is shown in Fig. 3(a). It has been found that the programmability required to generate waveforms mentioned above is present in MMC-based AWG. However, the challenge lies in generating short impulses such as Lightning Impulse (LI) present in the waveforms from Fig. 1 as compared with the low frequency part from these waveforms. The LI waveform, as shown in Fig. 3, has a rise time of 1.2 µs and tail time of 50 µs [5] and the same waveform is studied in detail to understand the challenges to generate the LI waveform and other complex waveforms from MMC-based AWG.

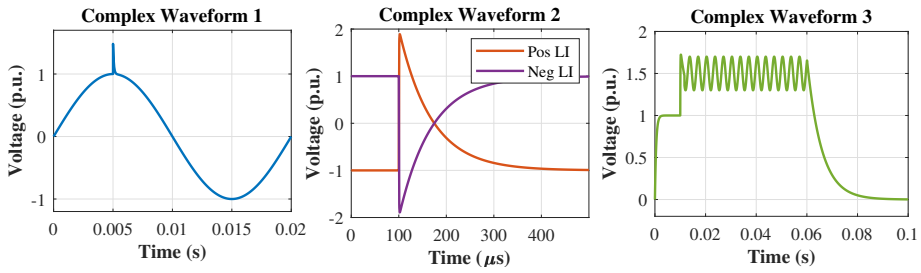

Fig. 1: Typical complex voltage waveforms required for the dielectric tests of grid assets [2][3][4]

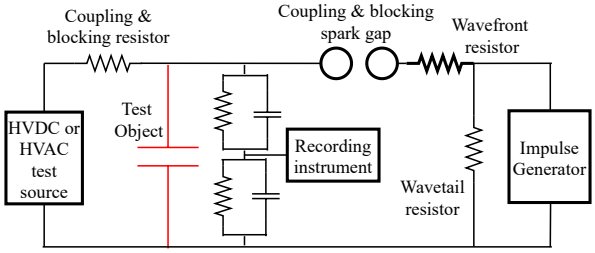

Fig. 2: Test Circuit for Generating Superimposed Waveforms shown in Fig. 1 [3]

There are several challenges for generating LI from an MMC, and they can be summarized as large bandwidth requirement, compensation of the jitter in several series-connected switches, and above all, the switches need to withstand a pulse current with high amplitude. The latter occurs because of the stringent requirement of applying steep dv/dt electric stress across the dielectric insulation of the grid assets that can be modelled as an electric capacitance [6]. The typical value of dielectric capacitance found in MV and HV grid equipment ranges from 100 pF to 10 nF [7]. Fig. 3(b) shows the equivalent circuit of a MMC-based AWG to calculate the exact current required to generate LI. Based on this equivalent circuit, the submodule current required to generate LI waveform across a MV distribution transformer of 36 kV rating which has a 10 nF equivalent dielectric capacitance [7] is calculated to be 1.7 kA in 0.2 µs, as shown in Fig. 3(c). The rise of 0.2 µs is calculated as the difference of time instants when the current magnitude is 10 % and 90 % of the peak current. Note that although the equipment is rated for 36 kV, it is tested at a much higher voltage amplitude such as 250 kV during a LI test [5]. Table I summarizes the pulse current required for generating LI across the MV distribution transformer.

Table I: Application requirement on pulse current

Pulse Current (A)	Rise time (µs)	Slew rate (A/µs)
1685	0.2	8425

Table II: IEC Standards for Performing Dielectric Tests on Most Common HV Grid Assets

Instrument	General Dielectric Standard	Switchgear	Distribution Transformer	AC Cable	Instrument Transformer
IEC Standard used	IEC 60060-1 IEC 60060-2	IEC 62271-1	IEC 60076-1 IEC 60073-3	IEC 60502	IEC 61869-1

If the high current rated IGBT modules are chosen to be incorporated into the MMC considering the generation of short impulses, the MMC-based HV test source will be bulky and costly. Moreover, other low-frequency waveform tests do not need a high current. Therefore, this paper aims to verify the pulse current capability of commercially available TO-packaged discrete SM devices instead of SM modules, which could be suited for the LI tests of grid assets.

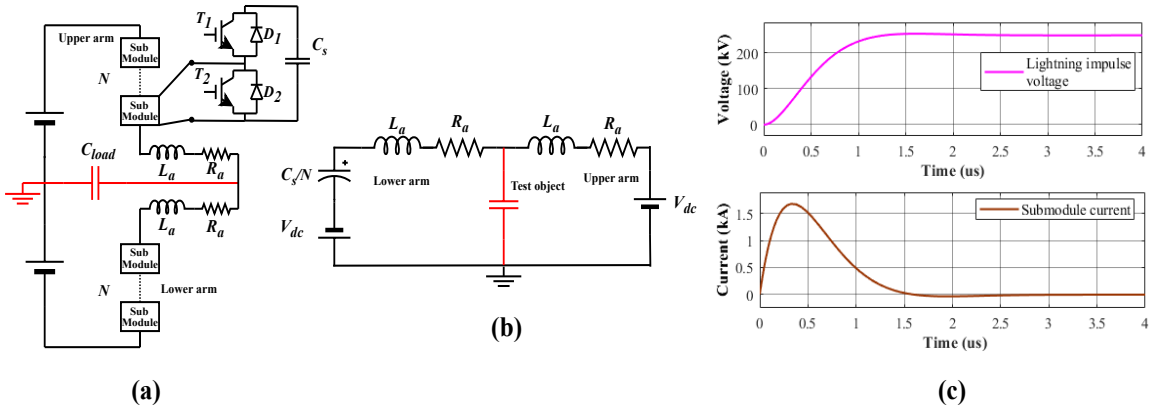

Fig. 3: (a) Schematic of the MMC-based HV AWG (b) Equivalent circuit of MMC for LI operation (c) Response of the MMC when the LI is generated

Please note that the MMC-based HV AWG does not generate continuous short impulses with a fast repetition rate. HV test sources are generally not used continuously like the HVDC converters [4]. They are used in shifts with definite off-time between two impulses and as per the testing requirement at the testing facility. Furthermore, the requirement of generating short impulses such as LI is different for different HV equipment. The testing requirements for each HV equipment are defined in their respective IEC standard, as shown in Table II. For example, LI is only applied seven times for MV transformers [8]. Additionally, it is possible to allow sufficient time between two impulses to prevent cumulative stress for the switches. In power electronic converters, SM devices are required to sustain the higher current for a short time due to various switching instants in the grid [9]. The switching instances in the grid are lower in the number compared to the impulse waveform generation from HV AWG. Hence, after studying the pulse current capability of switches, it is essential to test the short circuit reliability of SM devices to know how many pulses a device can withstand without undergoing severe degradation and how much off-time is necessary between two pulses to ensure the switches are not cumulatively overloaded.

Apart from the HV dielectric testing application, such a pulsed power operation of SM devices is extensively used in plasma applications [10]. Mostly, these plasma applications have a resistive load at a much lower voltage level. Even when it is capacitive load, the capacitance is in the range of 150 pF to 600 pF [11]. Additionally, the MMC-based AWG is a multi-purpose HV test source where the bandwidth of the desired waveform can vary from a very low value (such as DC) to a very large value (short impulses such as LI). This poses a unique requirement for the SM devices, where most tests need small

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current magnitudes, and only LI and other impulse tests require pulse currents with a high amplitude. All manufacturers of SM devices mention pulse current capability with other electrical properties in their datasheets. However, the single pulse current amplitude mentioned in these data sheets is rather limited to 2 to 3 times the rated continuous current at 25 °C junction temperature. Additionally, the short circuit test results on different semiconductor devices indicate that these devices can withstand much higher pulse current for short duration [9] [12] [13] [14]. However, these studies have analysed only the pulse current capability of a single switch technology, and benchmarking among other technologies is missing. In [14], pulse current capability of Silicon Carbide (SiC) MOSFET is compared with Field Stop (FS) IGBT.

This paper presents a comparison of 8 switches with different switch technologies and manufacturers to obtain the highest peak current with a fast rise time. The scientific contribution of this paper in relation to the pulse current capability of an MMC submodule implemented with several discrete SM technologies is summarized as follows:

- Comparison among Non-Punch Through (NPT) IGBT technology, Si Cool MOSFET technology, and SiC MOSFET technology
- Comparison between 2nd and 3rd generation SiC MOSFET technology
- Comparison between FS IGBT technology and 3rd SiC MOSFET technology
- Investigation of the NPT IGBTs with a different blocking voltage rating

Theoretical Background and Adopted Methodology

The current capability of a particular SM device is limited by various factors such as its on-state resistance, thermal stability limit, and package limit [15]. Fig. 4(b) shows these factors for a CREE-Wolfspeed device named C2M0160120D. Fig. 4(a) s hows the thermal impedance of the same switch for a single pulse with variable duty (0.01 to 0.5). As it is visible, the thermal impedance drops significantly as the pulse length is shortened, and thus this property enables the switch to safely conduct pulse currents of magnitudes much greater than its own rated current. As highlighted in Fig. 4(b), this article aims to find a safe operating point outside the typical SOA given in the SM datasheets for a single pulse application without damaging the device. The idea is to perform the pulse current tests in an MMC submodule prototype especially designed for the AWG application where TO-packaged SM devices can be implemented. Therein, various switch technologies are tested, and later their performances are benchmarked to find the most suitable SM technologies for the MMC-based HV AWG.

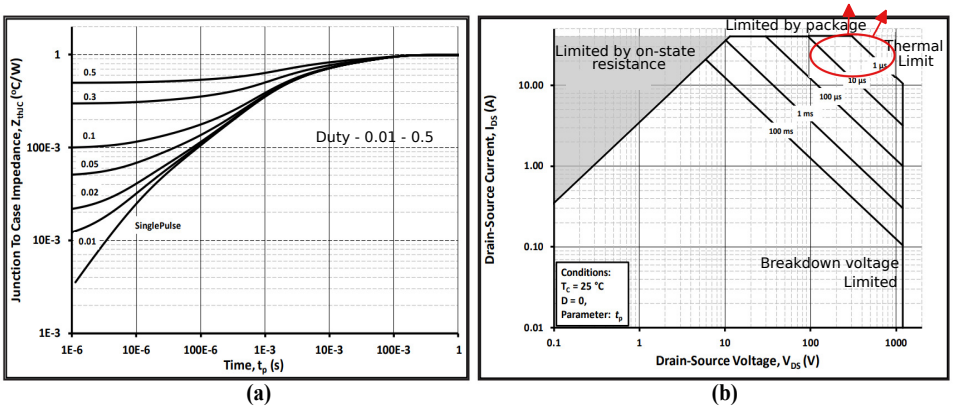

Fig. 4: C2M0160120D (a) Transient Thermal Impedances (Junction - Case) (b) Safe Operating Area

Since the requirements of the HV AWG application demands high pulse currents similar to the short circuit tests, SM devices are tested by discharging the charge stored in the capacitor into the Device Under Test (DUT) via an auxiliary loop that has minimal stray inductance and resistance to obtain the highest

peak pulse current with the fastest rise time. Various external electrical factors determine the magnitude and rise time of the peak pulse current. The factors that affect magnitude of peak pulse current are Gate to Source/Emitter voltage (V_{GS}/V_{GE}) and Drain/Collector to Source/Emitter voltage (V_{DS}/V_{CE}). V_{GS}/V_{GE} determines the thickness of the conduction channel and hence higher values of V_{GS}/V_{GE} results in a thicker conduction channel. Hence more electrons can pass through the channel. V_{DS}/V_{CE} determines the potential difference applied across the bulk of the SM device. Higher values of V_{DS}/V_{CE} results in higher potential difference applied across the bulk during the linear region of conduction and hence higher drain current. The gate resistance (R_G) determines the rise time directly as the time constant of the conduction channel is directly proportional to R_G [12]. Lower value of gate resistance results in a faster turn-on of the DUT. Thus, the lowest value of R_G is preferred. At high values of V_{DS}/V_{CE}, all DUTs undergo saturation because of pinch-off, limiting the peak pulse current magnitude to its final value [16]. Additionally, such a high magnitude of current heats up the DUT, resulting in increased bulk resistance of the DUT, reducing the peak magnitude of the current even further [17]. Therefore, first, the effect of the above-mentioned electrical parameters is studied experimentally using single SM device technology. Later, the electrical behavior of different SM device technologies with the same aforementioned electrical parameters are compared to one another to find out the most suitable technology that could satisfy the high current demand of the HV AWG application.

To achieve the goal of this article, multiple SM devices are chosen, and their details are summarized in Fig. 5. First, Cree-Wolfspeed C2M0160120D device is selected to test the experimental setup for constant V_{GS} while applying variable V_{DS} and vice-versa. Additionally, the same tests are repeated on three different devices to understand their behavior statistically. The three boxes in Fig. 5 represent different groups for comparing the pulse current behaviors of various switch technologies. IGBTs are classified into NPT, Punch Through (PT), and Trench Gate Field Stop (FS) based on the presence of an n+ buffer layer. Among these, NPT IGBT (SGW25N120) and FS IGBT (IHW40N120R5) from Infineon are selected to investigate their pulse current capabilities. Additionally, more NPT IGBTs from IXYS with higher blocking voltage capability, such as 1.7 kV (IXGH24N170) and 3.0 kV (IXBH20N300), are added to the list. MOSFETs are inherently famous for their faster switching characteristics over current carrying capacity. Therefore, Cool Si MOSFET (IPW90R120C3) from Infineon is selected to obtain a faster rise time. Since SiC MOSFET combines higher current carrying capability and fast switching characteristics, multiple devices from CREE-Wolfspeed with different current capabilities are selected to compare with other technologies.

No.	Device name	Manufacturer	V_{BR} (V)	I_D/I_C 25 °C (A)	I_{pulse} (A)	Op range for V_{GS} (V)
1.	C2M0160120D SiC MOSFET	CREE-Wolfspeed	1200	18	40	-5 /+20
2.	C3M0075120D SiC MOSFET	CREE-Wolfspeed	1200	32	80	-5 /+15
3.	C2M0080120D SiC MOSFET	CREE-Wolfspeed	1200	36	80	-5 /+20
4.	IPW90R120C3 Cool Si MOSFET	Infineon	900	36	96	± 20
5.	SGW25N120 NPT IGBT	Infineon	1200	46	84	± 20
6.	IXGH24N170 NPT IGBT	IXYS	1700	50	150	± 20
7.	IXBH20N300 (NPT IGBT)	IXYS	3000	50	150	± 20
8.	IHW40N120R5 FS IGBT	Infineon	1200	80	200	± 20
9.	C3M0016120D SiC MOSFET	CREE-Wolfspeed	1200	81	200	-5 /+15

Fig. 5: Details of the tested switches

Experimental Setup and Results

Fig. 6(a) shows the schematic of the test circuit to characterize the selected SM devices with an installed capacitance of 198 µF. In the actual test setup, the circuit is realized using a half-bridge submodule of

an MMC where the high side switch is shorted using a wire for current measurement, and the low side switch acts as a DUT. Indeed, even if the submodule PCB design is optimized, some stray inductance and stray resistance are added to the auxiliary loop. Their respective values are measured from the setup when the DUT is not inserted in the DUT holder. Hence, the stray inductances and resistances are measured with an impedance analyzer (Agilent 4294 A) in two steps. Firstly, these values are measured from the positive DC voltage to the Drain of the DUT. Secondly, these values are measured from the Source of the DUT to the negative DC voltage. By adding these values, the loop inductance and resistance can be calculated as 120 nH and 160 mΩ. This means that the different switching technologies from different manufacturers can add different inductance and resistance to the auxiliary loop. The packaging of these discrete SM devices can add significant inductance to the loop, as illustrated in [18][19]. That is why it is crucial to investigate the pulse current capability of different SM devices experimentally. Furthermore, the test circuit is studied in the LTspice with a SiC MOSFET from Cree-Wolfspeed (C2M0160120D) with its actual spice model, and the simulation results are compared with the experimental setup in Fig. 6(b). If the stray inductance and resistance are reduced from 120 nH and 160 mΩ to 30 nH and 40 mΩ in the spice model, the peak pulse current and the rise time of current waveform do not change. That means the DUT is saturating and limiting the pulse current over the stray inductance and resistance. The drain/collector current flowing through the DUT is measured using a Panasonic current sensor model 411. The V_{DS}/V_{CE} and V_{GS}/V_{GE} are measured using a differential probe from Keysight N2791A.

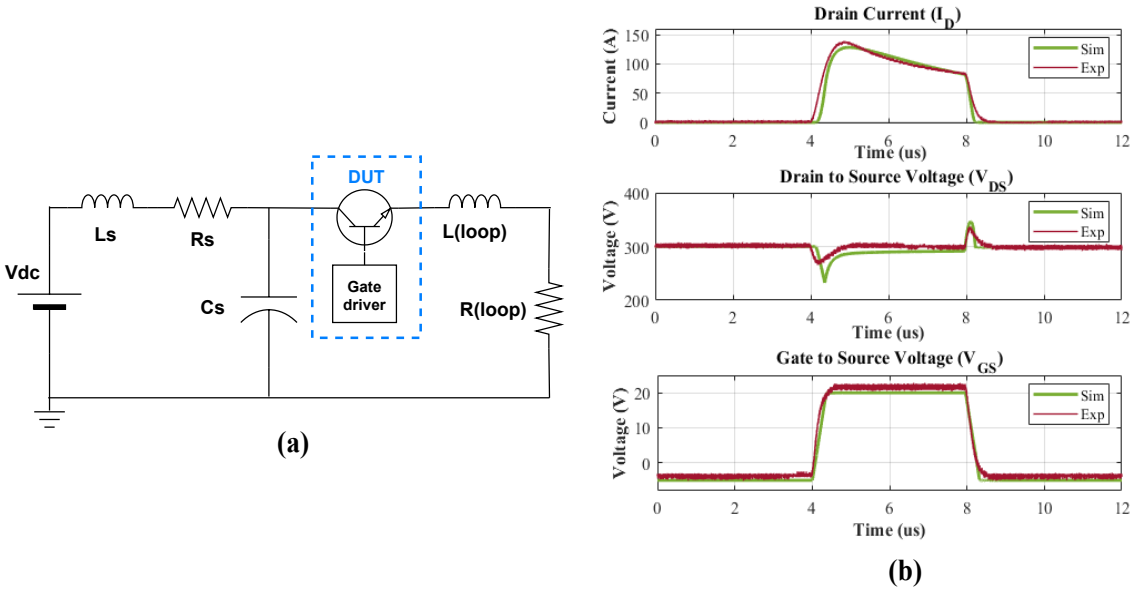

Fig. 6: (a) Schematic of the test setup (b) Comparison of LT-spice simulation and experimental results of C2M0160120D

The experimental setup is shown in Fig. 7. As discussed in the previous section, several circuit parameters affect the pulse current characteristic of the DUT, such as V_{GS}/V_{GE}, V_{DS}/V_{CE}, and the turn-on gate resistance ($R_{g,on}$). To obtain the fastest rise time from the DUT, the external turn-on gate resistance is set to 0 Ω for testing limits of all DUTs. Please note that the discrete SM devices have an internal gate resistance that limits the current rise time. However, the turn-off transient of the switch is limited by a much higher turn-off gate resistance ($R_{g,off}$), and the selected value is 10 Ω for all DUTs. The effect of V_{GS}/V_{GE} and V_{DS}/V_{CE} are studied with a SiC MOSFET (C2M0160120D), as shown in Fig. 8. With higher values of V_{GS}/V_{GE} and V_{DS}/V_{CE}, higher peak pulse currents are obtained with a faster rise time. However, the peak pulse current is more sensitive to V_{GS}/V_{GE} since it directly affects the thickness of the conduction channel that carries the current. Moreover, for the same V_{GS}/V_{GE}, the peak current capability is saturated for higher values of V_{DS}/V_{CE}, as it is visible in Fig. 8(b). These findings complement the theoretical understanding of these external electrical factors affecting the pulse current magnitude. Additionally, these tests are performed on multiple devices, their peak pulse currents are almost the same, and

a maximum difference of 1.2 % is found. Hence, for other DUTs, statistical analyses are not performed.

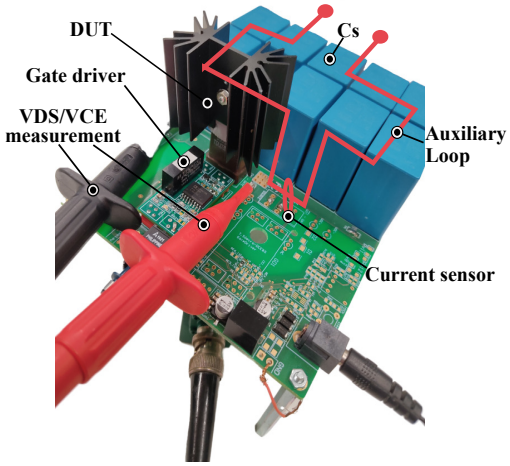

Fig. 7: Experimental Setup

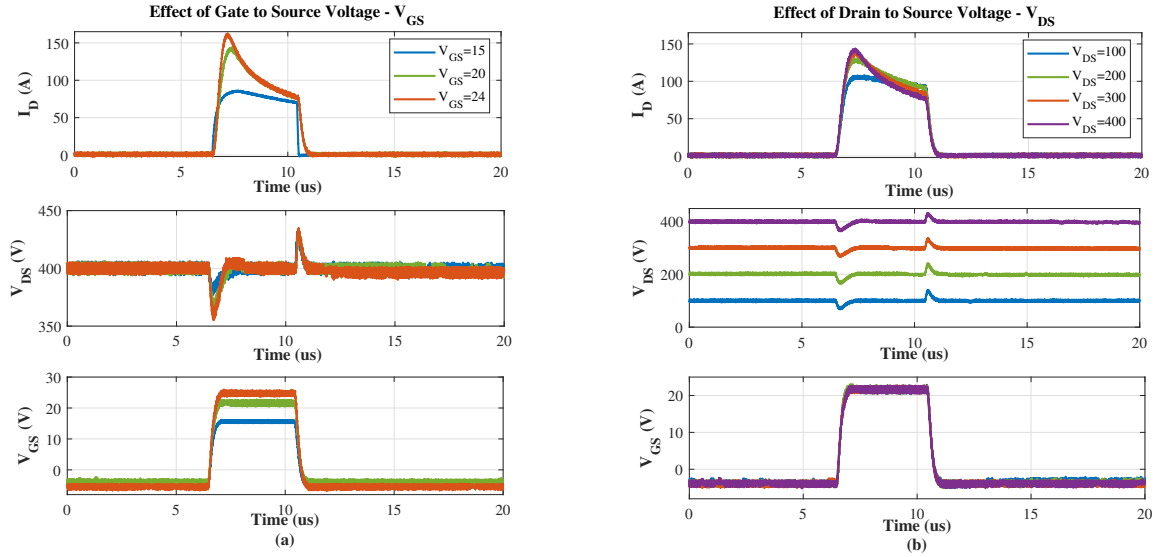

Fig. 8: C2M0160120D (a) Effect of the turn-on-gate-to-source voltage for constant V_{DS} = 400 V (b) Effect of applied drain-to-source voltage V_{GS} = 20 V

The first box from the list of tested switches consists of the NPT IGBT, Si Cool MOSFET, and SiC MOSFETs from 2nd and 3rd Generation with roughly the same rated current capability. The pulse current obtained from these four different technologies are compared at Fig. 9(a) for V_{GS} = 20 V. Since V_{GE}/V_{GS} and V_{CE}/V_{DS} waveforms follow a similar profile as shown in Fig. 8, they are excluded in Fig. 9 and further figures. It is visible that the NPT IGBT conducts a much higher magnitude of pulse current than all three technologies. However, Table III presented the rise time and obtained a slew rate, where NPT IGBT has the slowest rise time. Whereas the tested Si Cool MOSFET delivers the fastest rise time of 0.450 µs considering its superior switching performance. However, Si Cool MOSFET has an almost flat current profile compared to SiC MOSFET and Si IGBT, where higher V_{GS} values does not increase the peak current but only reduce the rise time. In the case of SiC MOSFETs, the current profile is significantly different at the peak and at the end of 4 µs. The 3rd generation SiC MOSFET performs better than the 2nd generation for V_{GS} = 20 V both in terms of the peak current and the rise time. However, this behaviour has changed at V_{GS} = 24 V in terms of the peak current obtained, as shown in Fig. 9(b). This change can be attributed to the difference in the operating range of V_{GS} of 2nd and 3rd Generation SiC

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MOSFETs.

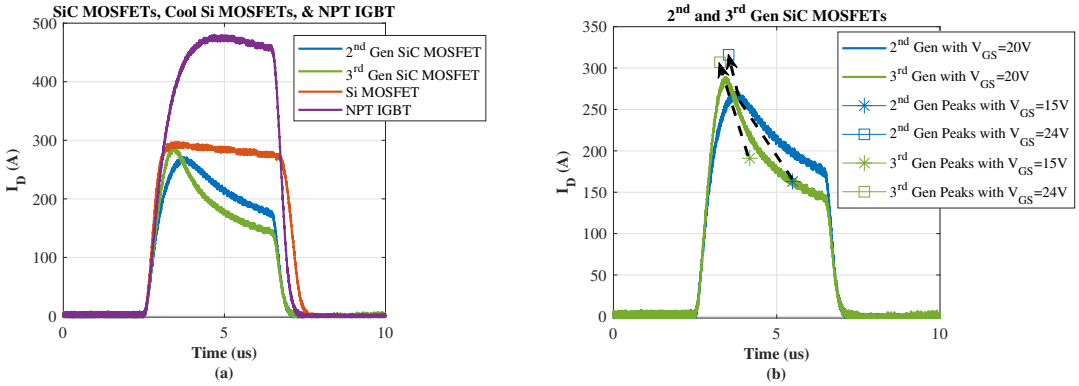

Fig. 9: V_{GS} = 20 V and V_{DS} = 300 V: Comparison of (a) SiC MOSFETs, Si MOSFET, and NPT IGBT (b) 2nd and 3rd Generation SiC MOSFETs

Table III: Comparison among 2nd and 3rd Generation SiC MOSFETs, Si MOSFET, and NPT IGBT

	C3M0075120D 3rd Gen SiC MOS I_c=32 A, I_p=80 A			C2M0080120D 2nd Gen SiC MOS I_c=36 A, I_p=80 A			IPW90R120C3 Cool Si MOS I_c=36 A, I_p=96 A			SGW25N120 NPT IGBT I_c=46 A, I_p=84 A		
VGS (V)	15	20	24	15	20	24	15	20	24	15	20	24
Pulse current obtained (A)	191	286	307	163	271	314	297	296	295	281	476	570
Times the rated current	6	8.9	9.6	4.5	7.53	8.7	8.2	8.2	8.2	6.1	10.3	12.4
Rise time (µs)	1.01	0.57	0.46	1.43	0.73	0.55	0.53	0.42	0.44	1.06	1.04	1.04
Slew rate (A/µs)	189	502	667	114	371	634	560	705	670	265	458	548

Fig. 10(a) compares the pulse current capability of NPT IGBTs with different breakdown voltage ratings. The peak current obtained from 1.7 kV rated switch is the highest. However, the rise time to reach the peak current increases as the blocking voltage rating of the devices increases since their switching performances are poorer with a higher blocking voltage rating. Fig. 10(b) compares the performance of the 3rd Generation SiC MOSFET and FS IGBT at V_{GS} = 24 V. SiC MOSFET performs much better with respect to both the peak current capability and the rise time, and it is summerized in Table IV, which was also observed in [14].

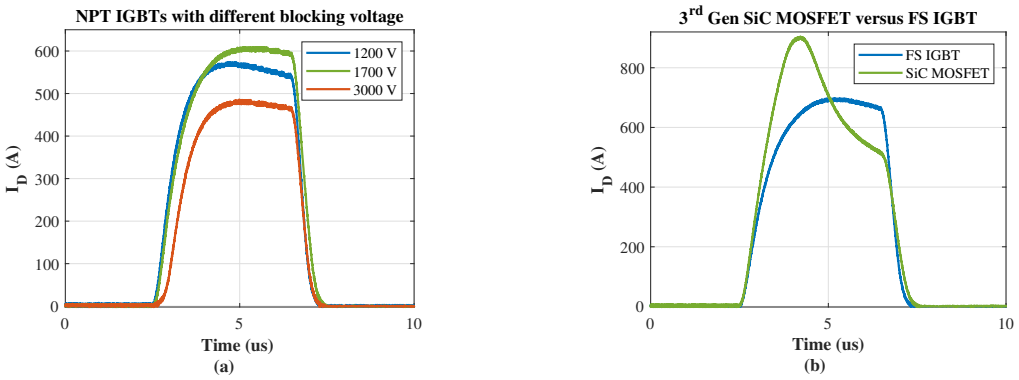

Fig. 10: V_{GS} = 24 V and V_{DS} = 300 V: (a) Effect of blocking voltage for NPT IGBTs (b) Comparison of SiC MOSFETs and FS IGBT

Table IV: Comparison between 3rd Generation SiC MOSFET and FS IGBT

	C3M0016120D 3rd Gen SiC MOSFET I_c=81 A, I_p=200 A			IHW40N120R5 FS IGBT I_c=80 A, I_p=200 A		
VGS (V)	15	20	24	15	20	24
Pulse current obtained (A)	579	809	905	287	554	697
Times the rated current	7.2	10	11.2	4.5	6.9	8.7
Rise time (µs)	2.47	1.24	1.06	1.27	1.32	1.36
Slew rate (A/µs)	234	652	854	226	420	521

Discussion

The quantitative comparison from the last section shows that the 3rd generation SiC MOSFET with 30 A current rating has a comparable rise time as the Si Cool MOSFET (0.040 µs faster). Additionally, the amplification factor of the peak current with respect to the rated current for the same SiC MOSFET is 9.6, which is 9.3 % higher than the Cool MOSFET but 30 % lower than the NPT IGBT. However, the slew rate obtained from SiC MOSFET is higher than the NPT IGBT by 17.8 %. In Table III, Cool Si MOS delivered the highest slew rate of 705 A/µs, which is 5.6 % higher than the SiC MOSFET. When the 30 A rated SiC MOSFET is compared with the 81 A rated SiC MOSFET, the latter delivers a much higher peak current, however, with a slower rise time. Additionally, the 81 A rated SiC MOSFET has achieved the highest slew rate among all tested switches, which is 17.5 % higher than the Si Cool MOSFET.

Apart from the quantitative comparison, it is important to understand qualitatively why different SM device technologies behave differently in Fig. 9 and Fig. 10. The Si MOSFET has the flattest current profile, whereas the drain current of SiC MOSFETs rises to a peak and reduces to a lower value at the end of 4 µs. Compared to these two technologies, Si IGBTs exhibit similar behavior of flat current profile with the Si MOSFET, with a much slower rise time. In all three device technologies, the DUT is saturated, and the conduction channel is pinched off considering the high value of the applied V_{DS}/V_{CE} [16]. The pinched-off state of the conduction channel adds significantly higher resistance for the drain/collector current to flow, and hence the peak value of the drain/collector current is limited. Additionally, when such a high current flows in the device, the temperature inside the substrate increases, and hence the overall bulk resistance increases. This relationship is linear in Si MOSFET and Si IGBT [20]. Hence, they have a flat pulse current profile in Fig. 9 and Fig. 10. However, SiC MOSFETs exhibit unique behaviour. When the temperature of the SiC device rises, the conduction channel exhibits a negative temperature coefficient. That is, the conduction channel resistance drops significantly, and charge carrier mobility increases in the conduction channel leading to the conduction of higher current magnitudes at the beginning of the current profile. But later, the resistance of the drift region dominates the overall resistance of the device as it starts to increase as the temperature increases leading to low values of drain current at the end of the current profile [12][20]. Due to these two effects, the current in SiC MOSFETs rises to a higher value and starts reducing to a lower value.

Apart from these dynamic factors, the obtained pulse current from various SM devices generally depends on the thickness of the device since the on-state resistance or bulk resistance directly depends on it. Among the different types of IGBTs, FS IGBT has the smallest thickness compared to NPT and PT IGBTs [21]. Therefore, it gives a comparable performance to a SiC MOSFET. With superior SiC material properties, the thickness of SiC MOSFET is significantly lowered [22]. Combining this property with the positive coefficient of channel mobility with temperature, SiC MOSFETs have superior performance. Among the Si MOSFET and IGBT which have flat profiles, the IGBT allows a higher peak pulse current considering its lower on-state resistance [16]. Nevertheless, this highest slew rate obtained from the 81 A SiC MOSFET is ten times smaller than the requirement of the application. Additionally, the obtained peak current and rise time are two times lower and five times slower than the requirement. Hence, it can be concluded that the SiC MOSFET with a lower current rating and lower voltage rating will have

superior switching performance, which may give the fast rise time of 0.2 µs. However, multiple lower current rated SiC MOSFETs need to be connected in parallel to meet the requirement of the peak current, similar to discussed in [23]. This makes the switch implementation complex to generate such a severe dv/dt stress across the capacitive load.

Conclusion

This article investigates the pulse current capability for various discrete SM devices for the MMC-based HV AWG for dielectric testing of grid assets. This application, particularly the lightning impulse tests, poses a unique operating condition for the switches with a very high peak pulse current and a very fast rise time. Among SiC MOSFETs, Si Cool MOSFET, and Si NPT IGBT with roughly 40 A current rating, NPT IGBT has the highest amplification factor for the peak current capability, and Si Cool MOSFET has the fastest rise time leading to the highest slew rate as well. 3rd generation SiC MOSFET has a comparable rise time to Si Cool MOSFET, but gives a higher amplification factor. The 81 A rated SiC MOSFET gives the highest amplification factor and slew rate among all tested devices; however, it has a rise time in the range of µs. Therefore, parallel operation of several low current rated SiC MOSFETs can be a solution to satisfy all criteria for this application.

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