A load-modulation digital data link for miniature ultrasound probes

by

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ABSTRACT

Miniature ultrasound probes, such as intravascular ultrasound (IVUS) probes, are valuable diagnostic tools and provide image guidance during minimally-invasive interventions. As more ultrasound transducer elements are built into such probes to improve image quality and frame rate, it becomes increasingly difficult to accommodate the cables needed to connect these elements to an imaging system. Among several reported cable-count reduction approaches, in-probe digitization of the received echo signals is a promising solution, as it allows digital data-link techniques to be leveraged to minimize cable count.

This work takes a previously-developed application-specific integrated circuit (ASIC) for an IVUS probe as a starting point. This ASIC employs a load-modulation datalink to transmit digitized echo signals of one element via a single micro-coaxial cable at 0.6 Gb/s. This thesis extends this work to multi-bit per-symbol signalling to increase the data rate, allowing the echo signals of multiple elements to be combined into one cable. First, the measured performance of the existing ASIC is compared to simulation results, showing the need for an S-parameter based cable model to faithfully reproduce the measured performance. Based on this simulation model, load modulation with a maximum of three bits per symbol and a maximum symbol rate of 600 MHz is investigated. The trade-off between data-transmission conditions and bit-error rate is investigated and gives a general idea about how fast the data rate can be.

An experimental setup is proposed to experimentally validate the performance of multi-bit load-modulation data links. For this, a prototype chip has been designed that includes a multi-bit load-modulation circuit and interfaces with an FPGA that provides test data. The chip has been taped out in a TSMC 0.18 um HV CMOS technology. Post-layout simulation shows that the prototype is able to generate a data rate of 1.6 Gb/s when there are two bits per symbol at the symbol rate of 800 MHz. Compared to the 0.6 Gb/s of the previous design, this is a substantially higher data rate.

Keywords: Intravascular ultrasound, one cable, load modulation, data rate.

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1 INTRODUCTION

1.1 BACKGROUND

Intravascular ultrasound (IVUS) imaging has played an important role in understanding atherosclerotic diseases in human beings [1]. It helps acquire an image of the vascular wall in Figure 1.1 and atherosclerotic plaques, which makes it easier for doctors to understand the atherosclerosis process and thus decide the proper treatment [2].

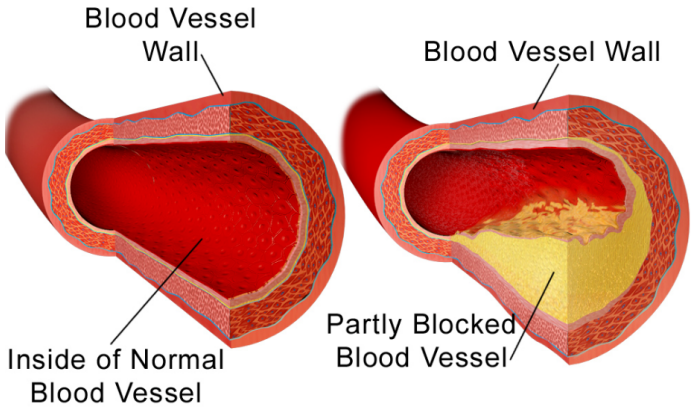

Figure 1.1: Normal and partly blocked blood vessel[2]

IVUS technology utilizes a miniature ultrasonic transducer at the tip of a catheter that is sent into the coronary arteries [3][4][5]. The transducers here are responsible for the pulse-echo measurement and can be divided into two categories by function: transmit and receive. Its timing diagram can be described in Figure 1.2. First, the transducers can be excited by electrical signals. At the same time, it converts these electrical signals to mechanical vibrations, during which the ultrasound waves are generated in transmit mode. Then, these ultrasound waves can be transmitted to target tissues and reflected inside the body. The echo signals can be reflected back to transducers where detectable electrical signals are generated. After that, these signals will be transmitted through a cable in the catheter to the imaging system where the imaging information will be transferred.

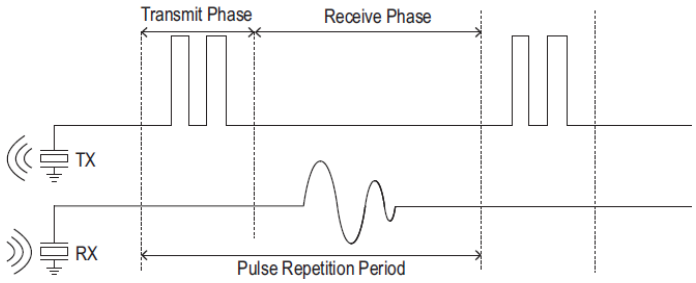

Figure 1.2: Timing diagram of a typical transmit and receive cycle [6]

Over the past few years, many efforts have been applied to acquire a more complete image of the blockage of the vessel in front of the catheter tip. Among them, there are two approaches to 3D imaging. On one hand, a mechanically-rotating single-element transducer is applied [7][8]. During

the working period, the transducer is excited at different angles to acquire the image information at the corresponding point respectively. However, it is hard to implement because it is highly dependent on a reliable rotating system. Also, it is expensive in manufacturing and slow in speed. On the other hand, the catheter can employ a transducer array at the tip of it [9]. In this case, several transducers can be excited at the same time and due to the array placement 1.3, image information at several points can be acquired at the same time. With the fixed transducers, the image can be more accurate, more time-saving and less expensive. Also, it eliminates the use of the rotation system. However, although the catheter-based IVUS ultrasound imaging has many advantages in terms of image integrity, the cable count remains a problem because of the catheter diameter limitation.

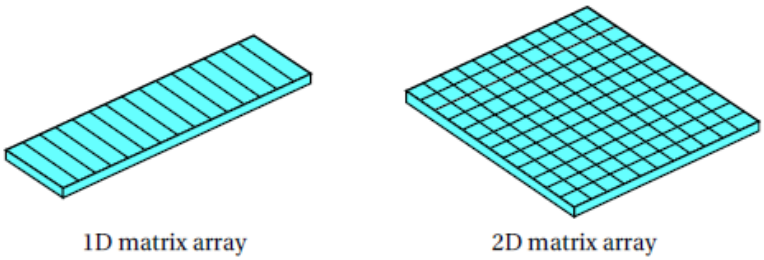

Figure 1.3: Illustration of 1D array and 2D array [10]

Also, for this catheter-based system, there is a need for a higher frame rate, especially during the surgeries. With an increased frame rate, more real-time imaging would be possible, which helps doctors conduct the surgery more precisely and reduces motion artifacts [11].

1.2 PRIOR ART

As mentioned above, transducer-array based IVUS imaging systems have the advantages that they eliminate the rotating system and are comparatively cheaper, which makes them popular among research. Several systems have been proposed in [12][13] already and some products are on the market, such as the Philips Eagle Eye Platinum digital IVUS catheter [14]. Shown in Figure 1.4, a block diagram of an example IVUS imaging system is presented [15].

In this system, there are 32 transducers for receive and 24 transducers for transmit both in an annular placement. Each transmit element is connected to a cable while the 32 receive elements are divided into four groups and then connected to four 8-1 multiplexers and buffer amplifiers. With a trans-impedance amplifier in the signal channel, the information is transmitted in an analog way through the cable. Thus, in this system, there are 24 cables for transmit, 4 cables for receive and some additional cables responsible for the power supply and control signals. In terms of further miniaturization

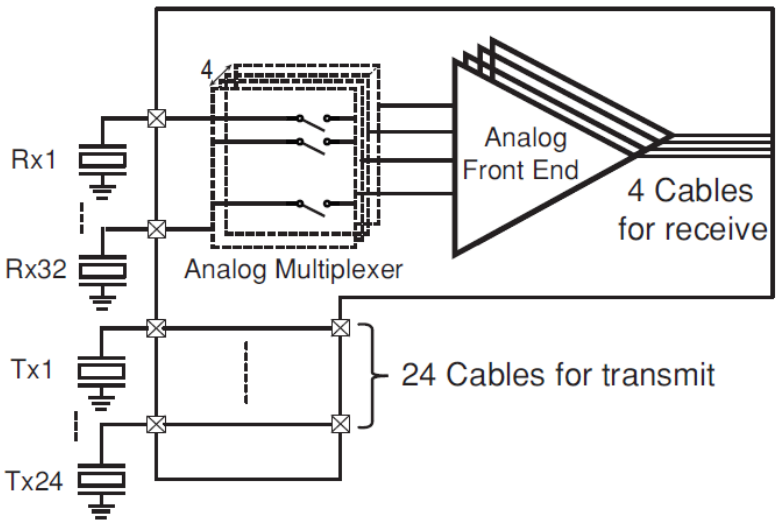

Figure 1.4: One example of the block diagram of the IVUS imaging system with more cables for transmission [15]

and cost reduction, cable-count reduction is desirable.

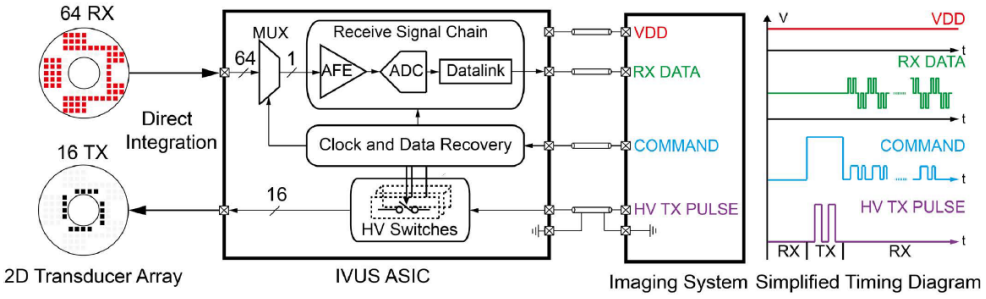

Figure 1.5: One example of the block diagram of the IVUS imaging system with four cables for transmission[16]

To make it more suitable for IVUS application, several efforts have been applied to further reduce the number of cables in the IVUS imaging system. In [16], only four cables are applied. As shown in Figure1.5, there are 64 receive elements and 16 transmit elements. For the transmit elements, instead of connecting to the cables respectively, all the transducers are connected in a multiplexed fashion to one cable and driven by a pulser on the system side. Additionally, a 64-1 multiplexer is applied to interface with the 64 receive elements rather than 8-1 multiplexers. With only one signal channel, it digitizes the signal first and sends the digitized signal to the system by load modulation. It helps achieve an effective data rate of 600 Mb/s. Also, with a modulation scheme, only one cable takes responsibility for digital signals controls.

Although the cable count is much reduced to 4, the 64-1 analog multiplexer does reduce the frame rate a lot. Acoustic pulses are transmitted using 16 TX elements and 64 RX elements receive their echo signals and digitize them

in 64 successive pulse-echo sequences. Thus, the total of 1024 (16×64) pulse-echo cycles are needed for a full synthetic-aperture image.

1.3 MOTIVATION

In terms of the limited catheter diameter in practical applications, it is necessary to reduce the cable count in IVUS ultrasound imaging systems. Although the cable count is successfully reduced to 4 [16], it utilizes an analog 64-1 multiplexer followed by only one signal channel. It is time-consuming to process the signal and transmit the data one by one, which limits its frame rate.

To reduce the cable count and make the system more real-time, the goal of this thesis is to further increase the data rate with only 4 cables. Additionally, in terms of its application in diagnosis and treatment, signals acquired at the system side should be decoded to represent the origin information accurately. Bit error rate (BER) can be introduced to describe its data accuracy.

Furthermore, although more emphasis is on IVUS imaging systems, cable-count reduction techniques discussed in this thesis can be more widely applicable. It can be valuable for other probes with cable-count limitation, including intracardiac echography (ICE) and transesophageal echocardiography (TEE).

1.4 DESIGN OBJECTIVES

In this project, several echo signals from the receive transducers should be locally digitized rather than being processed in an analog way because local digitization brings more possibility of data processing.

Also, in terms of power consumption, load modulation is more attractive than serialization and active drivers when only one cable is used for data transmission. Thus, an application-specific integrated circuit (ASIC) is proposed to investigate a load-modulation data link that can be capable of sending the digitized echo signals of multiple channels using only one micro coaxial cable.

Besides, the use of multi-level signalling to encode multiple bits per symbol will be investigated. Thus the relationship between the accuracy of data transmission and transmission conditions can be acquired. With different symbol rates or bits per symbol, its BER might be different.

An experimental setup is proposed based on a test ASIC and an FPGA. It can be used to characterize the relationship between data accuracy and transmission mode (non-return-to-zero and return-to-zero) and the trade-off between symbol rates and bits per symbol.

To conclude, a test ASIC with load-modulation data link is to be developed to achieve a data rate higher than 600Mb/s through one cable and reflects optimum transmission condition.

1.5 THESIS ORGANIZATION

The thesis presents steps to propose an architecture to further increase the data rate through one cable and present the specific data-link part. In this chapter, the need for the IVUS ultrasound imaging system with reduced cable count and high data rate has been introduced.

Chapter 2 discusses the possible ways to reduce the cable count in a broader ultrasound imaging system field and motivates the use of load modulation for a digital data link for ultrasound echo signals in miniature power-constrained devices.

Chapter 3 focuses on the existing ASIC with load-modulation data link and introduces a simulation model that enables us to reproduce the measured data link signals in simulation with good agreement.

Chapter 4 proposes a setup for evaluation of a next-generation load modulation data link with multi-bit per symbol signalling. Specifications of such signalling will be defined.

Chapter 5 shows the realization of the load-modulation test ASIC, mainly focusing on the load-modulation circuit and the data-rate doubling circuit.

Chapter 6 will provide the results of the trade-off between symbol rate and bits per signal in terms of data accuracy based on post-layout simulation. Also, it concludes the thesis and proposes ideas for future work.

2 CABLE-COUNT REDUCTION TECHNIQUES

As is mentioned in Section 1.1, the echo signals captured by receive transducers will be converted into electrical signals. In Figure 2.1, the analog signal can be directly transmitted through a coaxial cable to a imaging system. However, it leads to the cable impedance mismatch and thus causes reflections and signal attenuation. Matching networks tend to be used to deal with the impedance mismatch but they are very big.

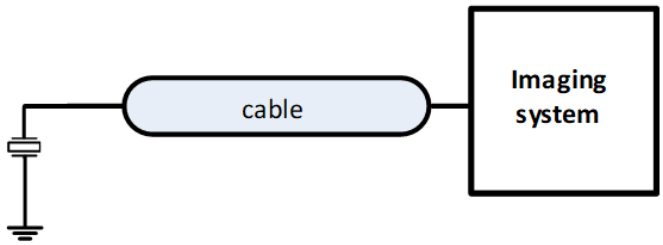

Figure 2.1: Simple signal transmission through coaxial cable

With the need for miniaturisation and robust signals, several signal processing processes have been implemented on-chip. An example of a single signal channel is shown in Figure 2.2. In this single-channel, the echo signals are captured by the analog front end (AFE) first. It mostly consists of a low noise amplifier (LNA) and a variable gain amplifier (VGA). The low noise amplifier is used as the first stage to interface with the echo signal with enough gain. It helps in attenuating noise from following stages. For the VGA, it is used to compensate for the propagation attenuation to generate a uniform signal amplitude versus time. Furthermore, with the purpose of the characteristic impedance match of the cable, a buffer or cable driver is required.

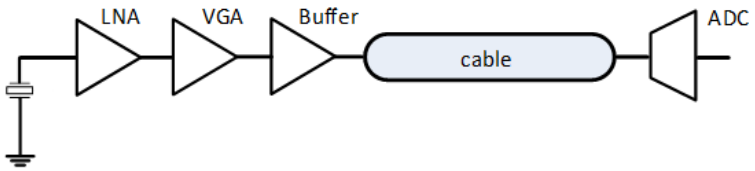

Figure 2.2: Signal transmission through coaxial cable

To get a more complete image and eliminate the need for a complex rotating system, a transducer-array is applied [9]. It means more echo signals should be processed and transmitted through the cable. Although each receive transducer can be applied to the signal channel respectively in Figure 2.3, the cables cannot be accommodated by the catheter due to its limited diameter.

Thus, with the increased number of transducers, ways to reduce the cable count should be explored to make it suitable for application.

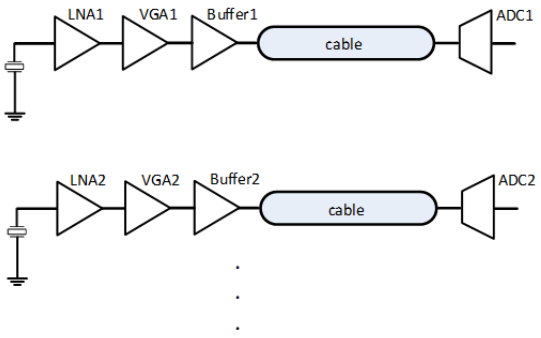

Figure 2.3: Signal transmission for multiple signals

In this chapter, both digital cable-count reduction and analog cable-count reduction methods will be discussed. Their original ultrasound imaging application might be transesophageal echocardiography (TEE) or intracardiac echocardiography (ICE), but the discussion will show whether it can be applied to the IVUS field. Also, once the cable-count reduction method is decided, the reason for increasing the data rate with load modulation will be motivated.

2.1 ANALOG CABLE-COUNT REDUCTION

The electrical signal captured from the transducer or processed after the AFE is inherently an analog signal. Thus, it is natural to consider reducing the cable-count in the analog domain.

Over the past years, beamforming, frequency-division multiplexing (FDM) and time-multiplexing have been successfully applied to reduce the cable count.

2.1.1 Beamforming

Beamforming plays an important role when there are a large number of transducers at the tip of the catheter. Although it can work in the transmit process as well as receive process, in terms of emphasis on signal processing, beamforming in receive process is explored.

When there are a lot of receive transducers, it is impossible to connect each of them to the cable directly. Thus, these transducers can be divided into several sub-arrays and with the proper delay, echo signals from transducers in the same sub-array can be combined by means of a delay-and-sum operation and then sent to the cable together, resulting in the reduction of cable count.

In [17], a signal processing architecture with beamforming technology is proposed to reduce the cable count. This technique has been applied in various research prototypes [18][19] as well as in commercial probes.

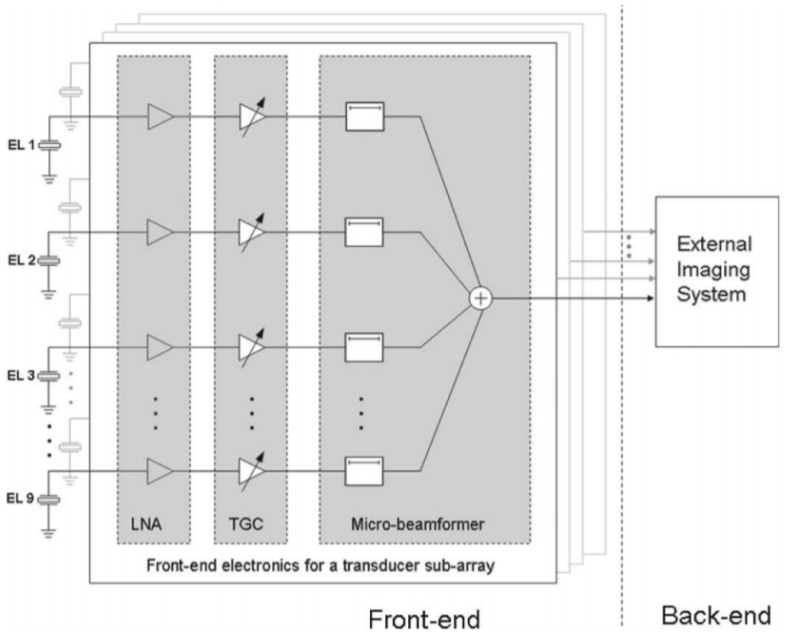

Figure 2.4: Signal processing architecture with beamforming for ultrasound imaging system [18]

Shown in Figure 2.4, nine transducers are combined as a sub-array and connected to an AFE respectively. After that, each of them is connected to the micro-beamformer cell to get the corresponding delay. This micro-beamformer consists of a programmable analog delay line (PADL) and a V/I converter. The PADL can generate delay from 40 ns to 280 ns with an increase of 40 ns each step while the converter brings convenience to the summation of the signals in the current mode. It eliminates the need for a summing amplifier and makes it more power-efficient.

For a large number of receive transducers, beamforming technology can greatly help reduce cable count. However, the sub-array beamforming does influence its frame rate and image quality.

2.1.2 Frequency-division Multiplexing

Analog orthogonal frequency-division multiplexing is the main signal processing technique to reduce the cable count here. When two information signals are mixed with a sine wave and a cosine wave of the same frequency respectively, these two signals are transferred to a certain frequency and added together. The final expression be can be expressed as follows:

$$X(w) = m_1(w) \times \cos(w_0) + m_2(w) \times \sin(w_0)$$

Thus, these two signals can be combined to reduce cable count from two to one. In the following demodulation process, when a sine wave of the same frequency is applied, the information signal m_2 can be acquired after a low-

pass filter. The mathematical process is shown below:

$$X(w) \times \sin(w_0) = (m_1(w) \times \cos(w_0) + m_2(w) \times \sin(w_0)) \times \sin(w_0)$$

$$X(w)\sin(w_0) = \frac{1}{2}m_1(w)sin(2w_0) + \frac{1}{2}m_2(w) - \frac{1}{2}cos(2w_0)$$

After the low-pass filter, the information signal m_2 remains only. It applies to signal m_1 as well when a cosine signal wave is applied.

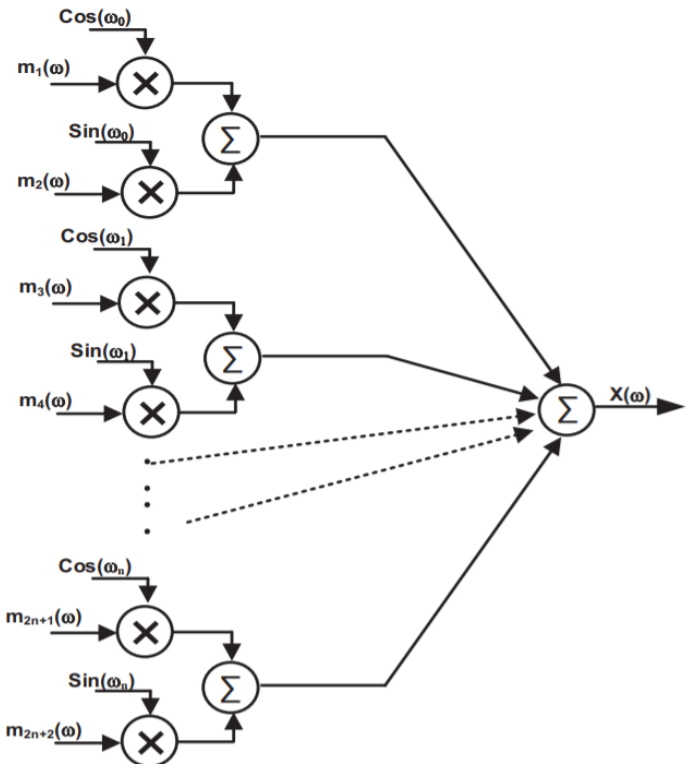

Figure 2.5: Block diagram of analog orthogonal frequency-division multiplexing [20]

In [20], the signal channels are increased to 8 and the working process including analog orthogonal frequency-division multiplexing can be expressed in Figure 2.5. The four carrier frequencies are 40MHz, 80MHz, 120MHz and 240MHz respectively and it successfully reduced the cable count responsible for signal transmission from eight to one. However, it requires more cables for clock and it suffers from cross-talk and cable non-idealities.

The frequency-division multiplexing is suitable for low-pass inputs. However, it might be difficult to work well in IVUS imaging field because of the band-pass characteristic of ultrasound signals. Also, to remain one-cable data transmission, more signals will be transmitted at the same time, which makes it difficult to leave out the influences of cross-talk and cable non-idealities.

2.1.3 Time-multiplexing

Normally, in a time-multiplexing ultrasound imaging system, like a system in Figure 2.6, several echo signals are processed by AFEs first and then sent to the sampling block with the sampling frequency f_s. After that, these signals will be sent into a high-frequency multiplexer and transmitted to the cable one by one.

In [21], echo signals from four transducers are sent to LNA and TGA first and after that, there are four sampling-capacitor arrays (SCA), which sample these analog signals at 25MHz. However, the four phase-shifted release clocks of SCAs are different. Thus, with the help of drivers, the converted currents are sent into the cable at four different time points and its sampling rate can be 100 MHz. However, the release clock limits the number of possible transducers and thus limits the data rate.

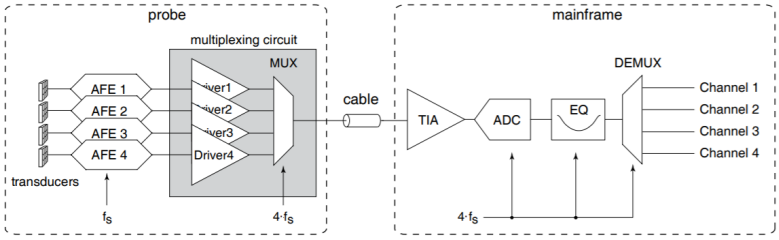

Figure 2.6: Block diagram of a time-multiplexing system [21]

However, this time-multiplexing system heavily replies on equalization on the system side to correct for the cable bandwidth limitation and its transmission-line effect. This increases complexity but limits the channel-to-channel crosstalk that can be achieved.

2.2 DIGITAL CABLE-COUNT REDUCTION

Several works have been reported to reduce the cable count digitally. The main idea behind this is to digitize the signals on-chip first with an ADC.

In [19], in terms of a large number of transducers, the idea of beamforming is applied first. Its architecture is presented in Figure 2.7. Each echo signal is processed by the LNA and TGA first and then it will be sent to a delay-line based micro-beamformer that combined the echo signals of a sub-array of 3×3 elements. However, after that, the signal is not sent into the driver directly as in [17]. Instead, they are added and digitized by a SAR ADC in the charge domain. In this case, four digital signals are acquired. With the following serialization, only one cable is responsible for data transmission. Thus, an overall channel-count reduction of 36 ($4\times3\times3$) is achieved.

Also, in [16], an ADC is applied after the AFE to digitize the signal directly, allowing for robust data transmission.

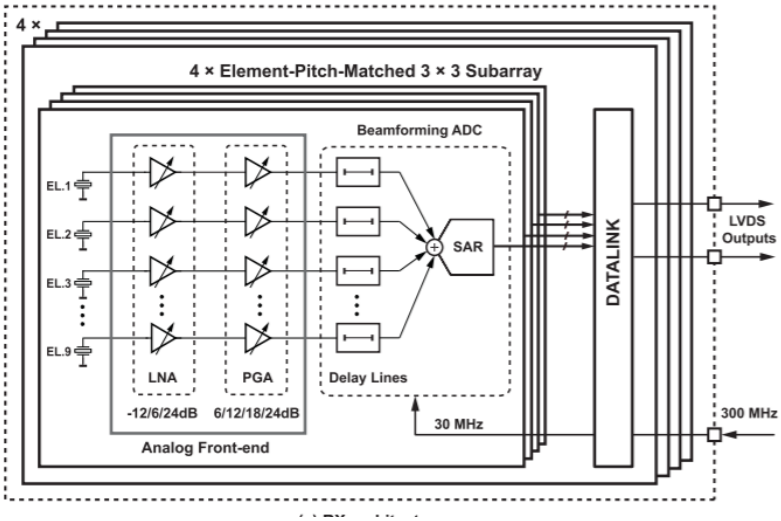

Figure 2.7: Architecture of receive electronics with digitization[19]

However, it consumes more die areas when there is an ADC after each AFE for digitization. Thus, the number of signal channels is limited.

2.3 DIGITAL DATA LINK TECHNIQUES

Compared to the analog cable-count reduction methods, digitization makes signals more robust against noise, interference and cross-talk. Considering the comparatively fewer receive transducers in an IVUS imaging system, digital cable-count reduction methods are a good candidate although ADCs might consume some die area. More importantly, with these digital signals, it brings more possibility for data processing on-chip to further reduce the cable count. In the following, ways of data processing are discussed.

First, serialization [19] has been applied to transmit the output of several digital signals to the cable one by one. A block diagram of a data link with serialization is shown in Figure 2.8. The four differential digital signals are converted into the single-bit mode with a clock-data-recovery circuit.

However, although the data-stream can be 1.5Gb/s, it requires a very accurate high-speed clock and a buffer. Also, it occupies a huge die area, which makes it difficult to transfer this technique to IVUS application.

To reduce its power consumption, post beamforming[10] can be applied in the signal processing. However, it results in a reduced imaging frame rate.

Second, load modulation [16] has been applied to transmit digital outputs through a cable by means of a variable equivalent resistance. With different input digital signals, the equivalent resistance value changes simultaneously. With the 50Ω characteristic impedance at the load side, it eliminates the power-hungry buffer. Also, it generates a voltage divider, which makes it

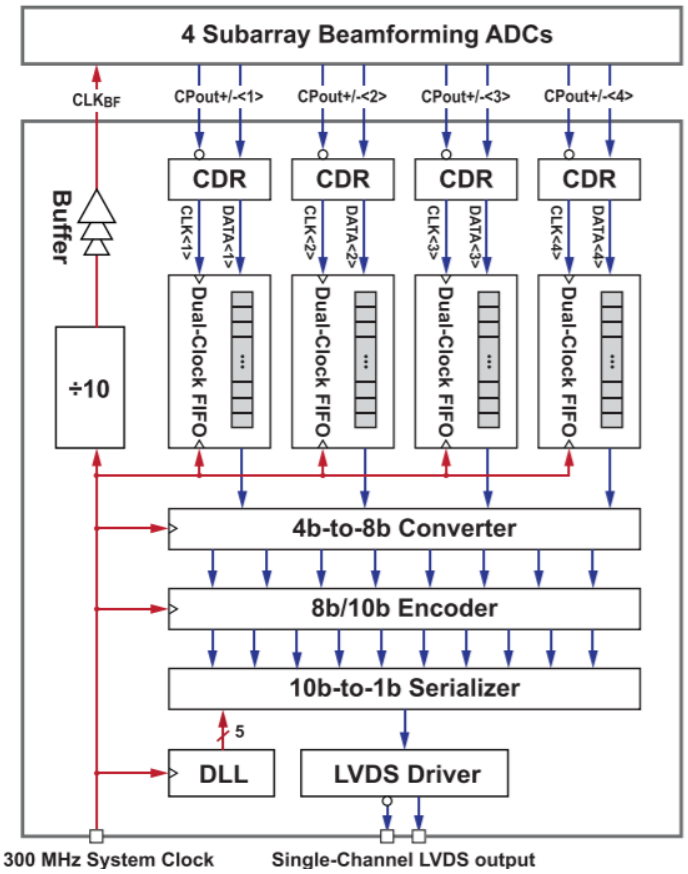

Figure 2.8: A block diagram of a data link with serialization [19]

possible to detect the changing voltage.

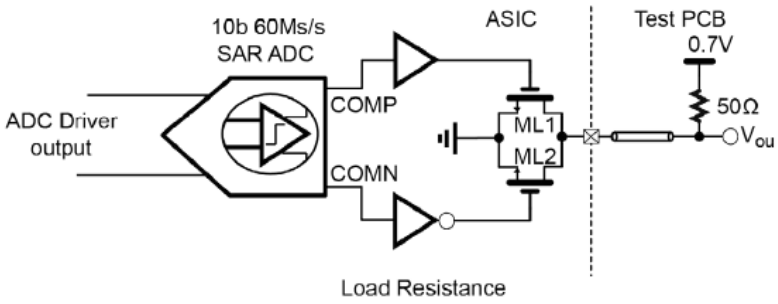

Figure 2.9: A block diagram of a data link with load modulation [16]

In Figure 2.9, the output of an asynchronous SAR ADC [16] is used directly to drive a load-modulation data link. With this differential signal, it controls two transistors respectively and thus generates three different voltage levels at V_{out}. Based on the voltage level, corresponding input data can be recovered at the system side. With this simple load modulation architecture, it generates 600Mb/s data rate without an accurate DLL and a power-hungry cable driver. Also, with an increased number of transistors, it can generate more voltage levels and thus increase the bits per symbol, which helps increase the data rate.

Besides, in terms of the multi-level signal transmission through a cable, several digital signals can be converted by a digital-to-analog converter (DAC). However, it brings circuit complexity. Worse still, it requires a cable driver or a buffer to match the cable characteristic impedance, which consumes more power on-chip. With the purpose of IVUS application, power-consumption on-chip should be as low as possible.

In this case, multi-level signalling by load modulation is more suitable for a digital data link in IVUS ultrasound systems. First, it eliminates the need for an additional cable driver, which reduces power consumption. It makes it more suitable for the low-power application. Also, in terms of circuit complexity, it is comparatively easier and gives a quick insight into the data transmission through one cable. Additionally, it transmits more than one bit per symbol. Although symbol rate is limited by the limited cable bandwidth, multi-bit per symbol can help increase data rate.

3 EXISTING ASIC WITH LOAD-MODULATION DATA LINK

3.1 INTRODUCTION TO EXISTING ASIC WITH LOAD-MODULATION DATA LINK

The availability of an existing ASIC [16] with local digitization and load-modulation data link helps to further explore the potential of such a data link for miniature ultrasound probes. The architecture is discussed below.

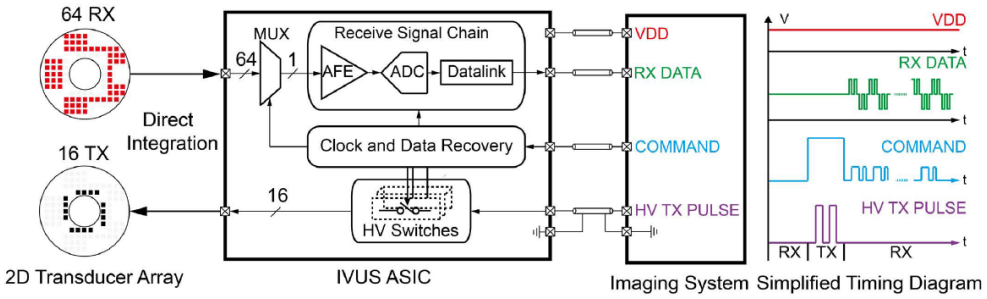

Figure 3.1: The block diagram of an IVUS imaging system with load-modulation data link [16]

In Figure 3.1, the 16 TX transducers are controlled and excited by on-chip high-voltage switches that route a HV signal generated at the system side, and the remaining 64 RX transducers are interfaced with a 64-1 analog multiplexer and an analog front end. These processed signals are connected to a SAR ADC, which transforms analog signals into digital ones. This ADC generates two differential outputs for one data.

The clock extracted from the command signal eliminates an external clock and its working principle is shown in Figure 3.2. The command signal is processed by NMOS transistor $M0$ first, followed by a continuous-time comparator. The comparator turns the signal into proper logic levels. At the rising edge, the resulting signal triggers the ADC and it working frequency is 60 MHz.

Also, with its clock generated from an asynchronous SAR logic, the differential outputs both generate a zero between two data. The SAR logic provides two phases: 'reset' and 'decision'. Each phase is around $0.5t$ and its timing diagram is presented in Figure 3.3. $COMP$ and $COMN$ are the differential outputs of the comparator.

Then, the 10-bit ADC output is transmitted through one cable. Decided by registers, t in Figure 3.3 is less than 1.6 ns. Thus, between every 10 bits signals, there is a relatively long return-to-zero stage. Shown in Figure 3.4, with a buffer and an inverter, the two comparator outputs of the ADC are connected to two NMOS transistors $ML1$ and $ML2$ respectively to act as control signals. The resistance of the two transistors changes with these control signals. Thus, it can generate three different voltage levels when it is observed at V_{out}. Each voltage level (around 200 mV, 700mV and 350 mV) can represent its corresponding ADC output information: '0', '1' and 'return-

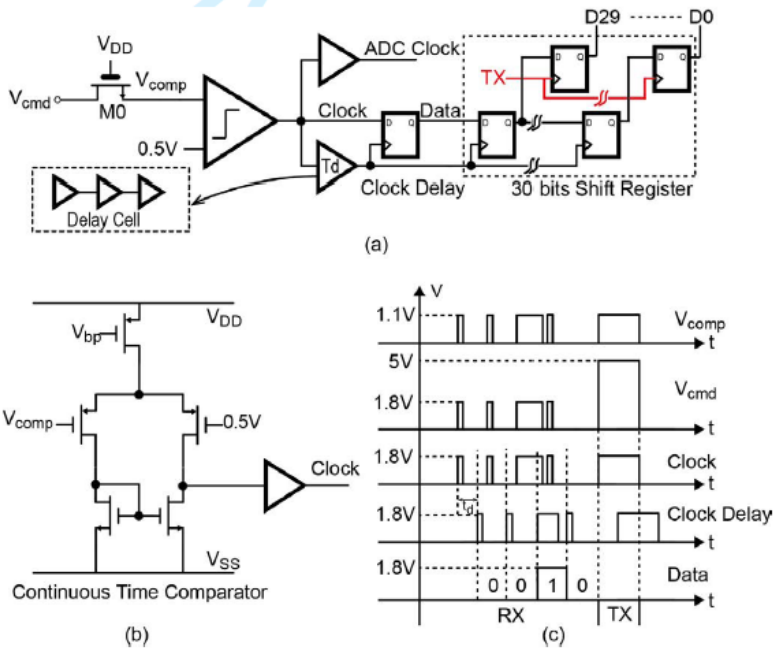

Figure 3.2: Circuit diagrams of (a) clock and data recovery; (b) the continuous-time comparator; (c) associated time diagram [16]

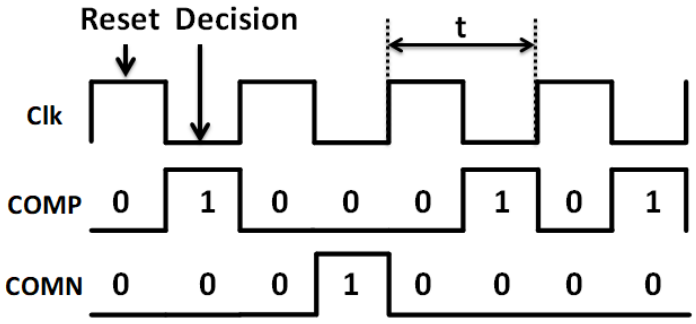

Figure 3.3: Timing diagram of the comparator [16]

to-zero". Also, due to the comparator clock, there is a return-to-zero stage, which helps distinguish two adjacent signals. It brings convenience in the decoding process.

Through load modulation, the digitized signals can be transmitted serially through only one cable in a power-efficient and simple way. Decided by the ADC specifications, the data rate is 600 Mb/s. However, 64-1 multiplexer does influence its frame rate. To acquire its image information more quickly, One possible way is to replace the multiplexer with 32-1 or smaller ones but it requires at least doubling the data rate without the increase of cable count. Multi-bit per symbol signalling can be a good choice to increase the data rate with one cable for a faster frame rate when the same technology (180 nm) is applied. Thus, to explore signal transmission through cables, the cable specification should be further analysed.

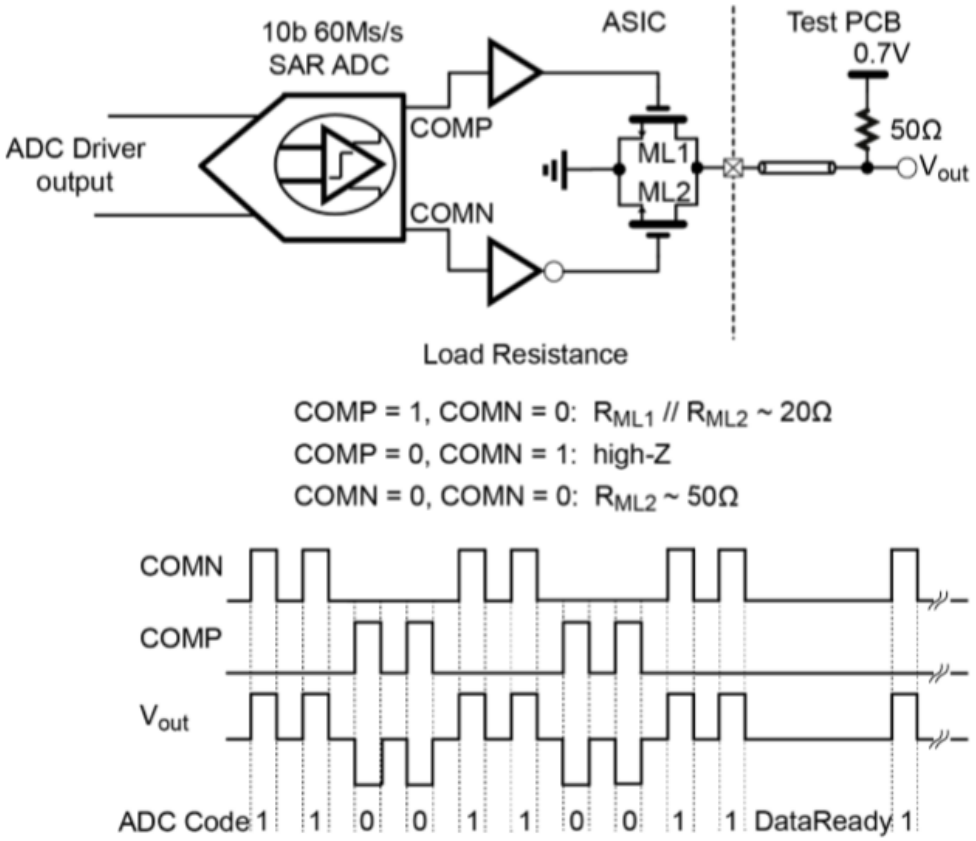

Figure 3.4: Block diagram and waveforms of the load modulation data link [16]

3.2 MEASUREMENT OF EXISTING ASIC WITH LOAD-MODULATION DATA LINK

In this section, the measurement result of the existing ASIC is presented first, followed by a discussion about its features.

With a proper setup, the waveform at the system side is captured through an oscilloscope and processed by MATLAB on a PC. In this setup, the ASIC and the oscilloscope are connected with an active probe, YOKOGAWA PBA2500. Its -3dB bandwidth is 2.5 GHz, which ensures the proper transmission for this system. However, the bandwidth of the oscilloscope (YOKOGAWA DL9710L) is 1 GHz only and it might filer out the signals because due to the return-to-zero stage, the waveform frequency is 1.2 GHz.

Shown in Figure 3.5, signals among *Level_0* and *Level_1* should represent 0 and 1 respectively. Taking the return-to-zero stages into consideration, there should be three fixed voltage levels. Signals representing 0 should have the same amplitude. However, for *Level_0*, although it can be distinguished from the other two voltage levels, there are some variations in amplitude. For one bit per symbol, it requires three voltage levels only, including two information levels and one transition level. Certain variations can be acceptable when intervals of each two are obvious. However, it might be a problem

for multi-bit per symbol because there are more voltage levels closer to each other when the supply voltage at the system side remains same.

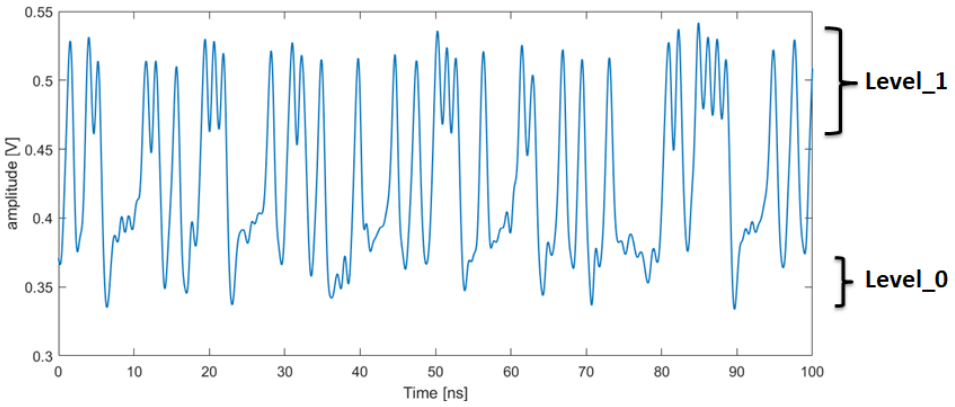

Figure 3.5: Measured waveform of the existing ASIC

There are some potential explanations for these variations. One possible reason is reflections due to impedance mismatch. This mismatch may come from impedance resistor or the parasitic effect generated from the two interfaces of the coaxial cable, where parasitic capacitance and inductance can influence the equivalent impedance seen from the system side, in Figure 3.6. In this case, there is another parasitic capacitance $C1$ at the system side. It is in parallel with 50 Ω and it results in the change in equivalent impedance. Due to the transmission effect, it will cause impedance mismatch and lead to reflection. Another possibility is that the cable itself causes these variations.

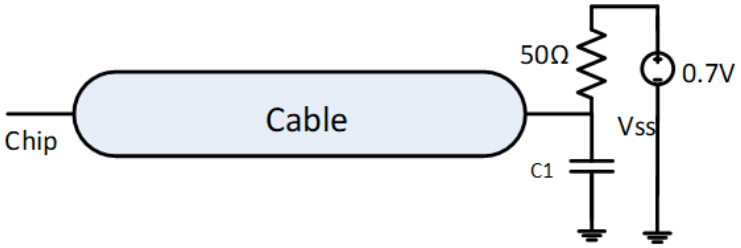

Figure 3.6: Illustration of equivalent impedance

Thus, to find out the reason behind the variations, a test experiment is carried out. It aims to test whether there is obvious reflections caused by impedance mismatch. In this measurements, with a reduced clock frequency from FPGA, the interval time between two 10-bit signals is increased, which helps observe reflections. A passive probe, YOKOGAWA 701943, is applied and its bandwidth is around 500MHz.

In Figure 3.7, there are some reflections appearing at the chip side and due to signal transmission through the cable, it takes 10 ns for reflections from signals at the system side to appear at the chip side again. In this case, these

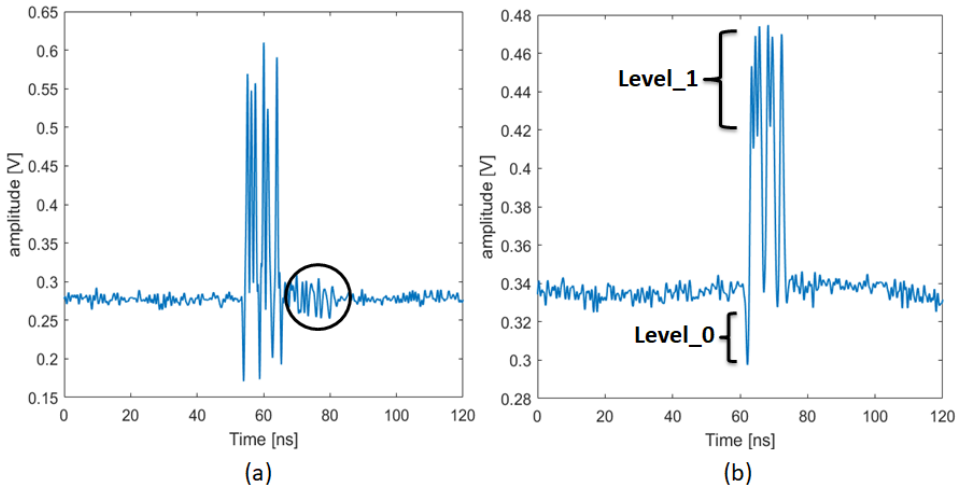

Figure 3.7: Waveform of (a) chip side of normal measurement (b) system side of normal measurement

reflections should take around another 10 ns to arrive at the system side to influence signals. However, there are not obvious changes in amplitude after the wave of a 10-bit signal. At the same time, for signal waves at the system side, there remain obvious variations at the very beginning.

Also, in Figure 3.7, obvious noise is observed during the intervals. It is generated by the oscilloscope itself. The peak-to-peak noise can be 42 mV when the probe is short-connected. To get a cleaner waveform, an oscilloscope with a lager bandwidth should be applied for measurement.

Thus, as discussed above, although there exit reflections, obvious variations can appear at the beginning when reflections cannot influence its waveform in Figure 3.5. Impedance mismatch will cause variations but it is not the dominant cause. Based on the previous assumptions, it may come from the coaxial cable itself. To investigate the load-modulation data link with one cable transmission, a reliable cable model should be applied.

3.3 RLCG CABLE MODEL

In [16], a 1.5-meter 42 AWG coaxial cable is applied for measurement. This type of cable can be modeled as a transmission line model and its parameters are presented in Table 3.1.

These parameters can be applied in the Spectre multi-conductor transmission line model for simulation to mimic the reflection measurement in 3.2. The simplified simulation test bench is shown in Figure 3.8.

COMP and COMN are control signals from outputs of the ADC comparator, in Figure 3.4. They are generated by a Verilog A model in simulation. The corresponding control signals are presented in Figure 3.9. Also, to take

Table 3.1: 42AWG coaxial cable parameters [22]

	AWG 42
R(*Ohm*/m)	7.5
C(pF/m)	110
L(nH/m)	275
G(nS/m)	660
Attenuation(dB/m)	0.7

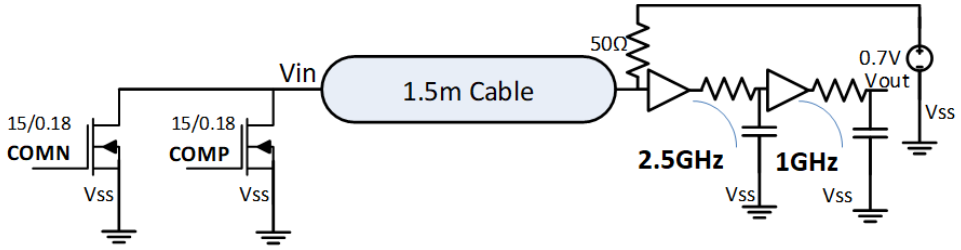

Figure 3.8: Simplified system for simulation

the bandwidth limitation of the active probe and the oscilloscope into consideration, two low-pass networks are connected in series and their -3dB bandwidth is 2.5 GHz and 1 GHz respectively. However, for this simplified system, it excludes some parasitic effects and control signals are ideal.

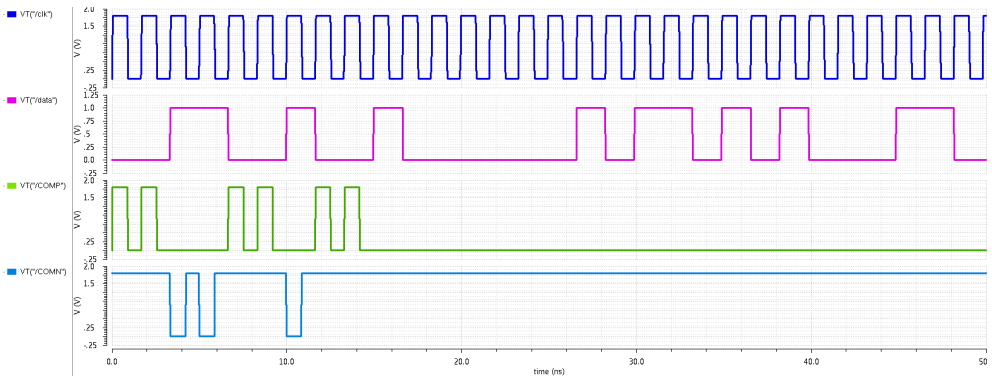

Figure 3.9: Control signals generated with Verilog A model

The corresponding V_{chip} and V_{out} are shown in Figure 3.10. For the voltage observed from the chip side, there is no reflection and for the same voltage level at the system side, there is no variation.

Also, when the waveforms of both measurement and simulation results are compared, the voltage intervals between two levels are different. The difference can be summarized in Table 3.2. Although some non-idealities like parasitic capacitance are excluded, the differences should not be too obvious.

Thus, for the RLCG model, it is too ideal to represent model function during signal transmission and it cannot predict the variations correctly.

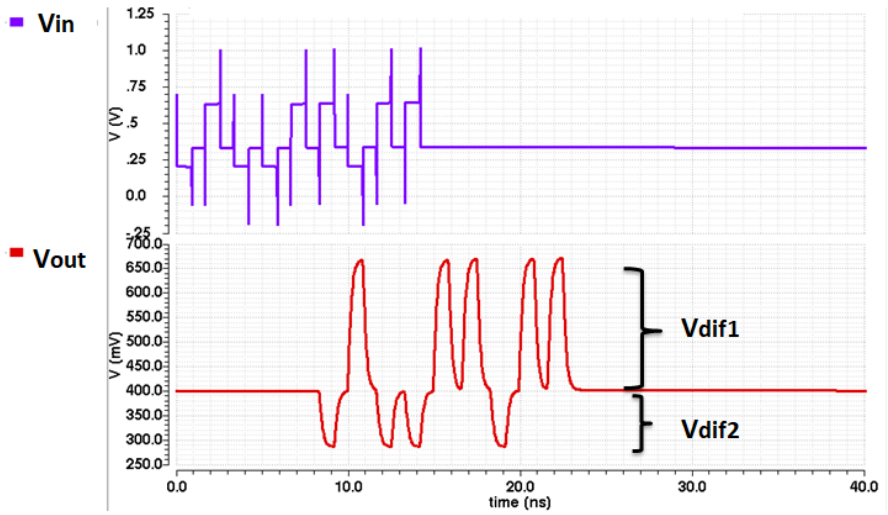

Figure 3.10: Corresponding waveforms at *Vin* and *Vout* for RLCG model

Table 3.2: Voltage change comparison between RLCG model and measurement

	Simulation	Measurement
V_{dif1}**/mV**	270	175
V_{dif2}**/mV**	120	50

3.4 S PARAMETER-BASED CABLE MODEL

A measured S parameter file can be applied in 'n2port' instance in Cadence for simulation. Compared with the RLCG model, they are both extracted from measurement, but RLCG model ignores its frequency-dependent performance. However, the limitation of the S parameter model is that only a one-meter cable measurement result is available and its accuracy is highly dependent on the measurement process.

In order to mimic load modulation performance in Figure 3.4, the same test bench in Figure 3.8 is applied. Also, two 'n2port' instances are put in series to compensate for the length difference although it might bring more attenuation.

Shown in Figure 3.11, at the chip side, there is some small reflection. Also, at the system side, there are not obvious reflections. For the same voltage level, there are some variations. These are in agreement with measurement.

To further explore the reliability of this S parameter-based cable model, another simulation with 1m cable is done to help get a rough idea about the 1.5-meter cable transmission situation. The simulation results are shown below.

From the simulation result in Figure 3.12, it shows that with the increase of cable length, the delay time increases and the attenuation effect of the cable

Figure 3.11: Corresponding waveforms at *Vin* and *Vout* for S parameter model

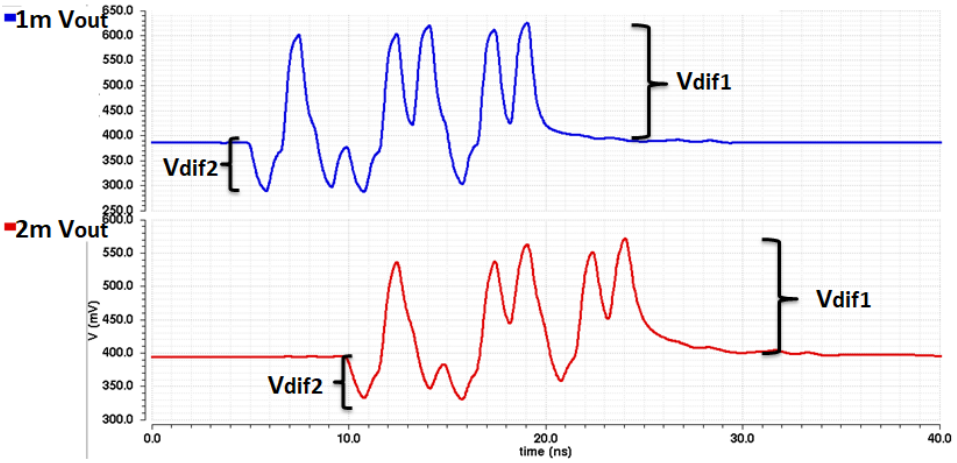

Figure 3.12: Corresponding V_{out} for 1m and 2m cable

is more severe. Although there might be some parasitic components that affect its waveform, the cable is the main reason for amplitude loss.

Also, some variations can be observed. Even when the two low-pass filter networks are removed, the variations remain. For the wave after the 9-bit signal, it is almost flat and it shows that, reflection will not lead to an obvious change in signal amplitude. Thus, the cable is responsible for the variations as well.

In Table 3.3, although the 1.5-meter S parameter-file is missing, it provides a rough value of V_{dif1} and V_{dif2} respectively. Compared to those from RLCG

Table 3.3: Voltage change comparison between two models and measurement

	Simulation-1m	Simulation-2m	Simulation-RLCG	Measurement
V_{dif1}**/mV**	236	170	270	175
V_{dif2}**/mV)**	100	60	120	50

model simulation result, S parameters-based simulation results are closer to the practical measurement results. What's more, in [16], the frequency of signals is even a bit higher than 600 MHz. It means the signals will suffer more attenuation, which will make the simulation result closer to measurement result.

4 EXPERIMENTAL SETUP FOR EVALUATION OF LOAD-MODULATION

In this chapter, several types of cables are discussed first to choose a more suitable one for this project. With the chosen type of cable, the specifications of the data link part can be derived. In this case, a complete architecture with load-modulation data link will be proposed. Furthermore, a simplified ASIC architecture with multi-bit per symbol signalling will be shown to help reduce project complexity and a rough experimental setup will be described to evaluate the load-modulation data link by comparing the data rate and its corresponding BER number.

4.1 CHOICE OF CABLE

As discussed in Chapter 3, an S parameter-based cable model is more practical to predict cable performance in simulation including inter-symbol interference and attenuation. To ensure high-quality signal transmission, types of cables should be explored to choose a more suitable one for this project.

Four types of micro-coaxial cables commonly used in catheters are considered: AWG 42[22], AWG 44[23], AWG 46[24], AWG 48[25]. The comparisons are based on their characteristic frequency-dependant attenuation and data rate per cross-sectional area.

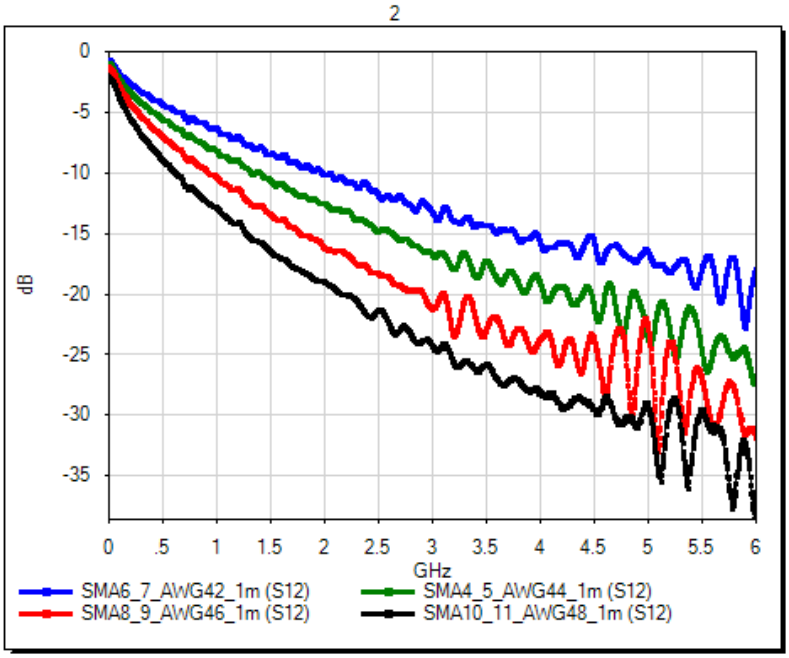

Figure 4.1: S_{12} of four types of cables

Figure 4.1 represents the measured relationship between transmission coefficients and frequency for four types of cables respectively. First, all their coefficients decrease with frequency. This complicates high-speed signal transmission because the attenuation effect becomes more severe and brings difficulty to decoding over a certain symbol rate. If there is only one bit per symbol, the achievable data rate will be limited in terms of data accuracy.

Second, compared to the other three types of cables, cable AWG 42 suffers the least attenuation at all frequencies, which is only half of the attenuation of cable AWG 48. This feature makes AWG 42 a better candidate for 1-bit signal transmission, but at the expense of a larger diameter.

Furthermore, multi-bit per symbol transmission can be explored and the schematic of 2-bit load modulation transmission is shown in Figure 4.2. Ideally, there should be four fixed levels. The sizes of these transistors are chosen to ensure that each interval between two levels is around 80 mV. Thermometer coding is applied and Table 4.1 illustrates its control logic. Figure 4.3 shows the simulated waveforms at V_{out} when AWG 48 and AWG 42 are applied respectively. Although the two waveforms at *Vout* are similar, the intervals between two adjacent voltage levels are different because of their different frequency-dependent attenuation. The average voltage interval of AWG 48 is 40 mV and that of AWG 42 is 60 mV at the symbol rate of 500 MHz under the same load-modulation structure. The larger voltage difference between two levels makes it easier to decode input data and allows some non-idealities like noise, which makes AWG 42 more suitable for multi-bit per symbol transmission as well.

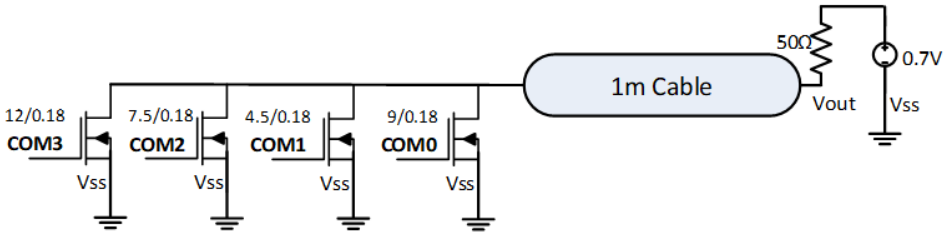

Figure 4.2: Schematic of 2-bit per symbol transmission with an interval of 80 mV

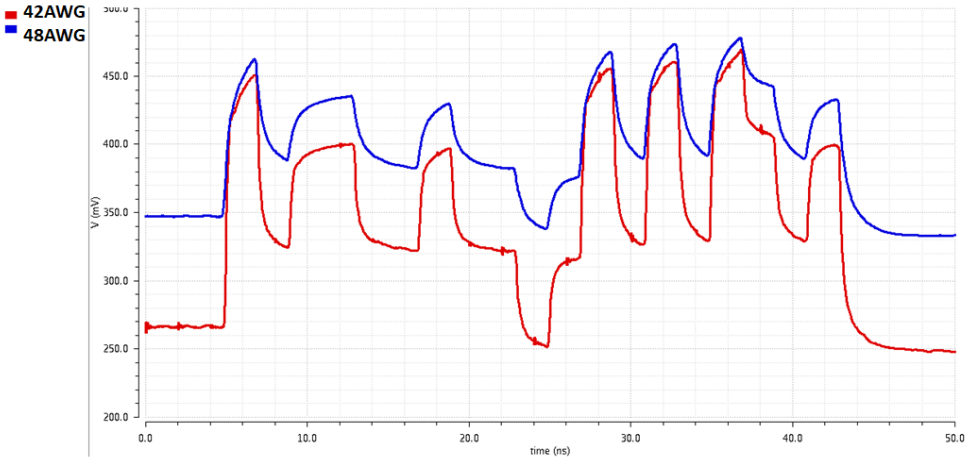

Figure 4.3: Output waveforms of AWG 48 and AWG 42 at the symbol rate of 500 MHz

Table 4.1: Thermometer coding for 2-bit per symbol transmission

Input Data	COM3	COM2	COM1	COM0
11	1	1	1	1
10	0	1	1	1
01	0	0	1	1
00	0	0	0	1

Table 4.2: Diameters of different cables[22][23][24][25]

	AWG 42	AWG 44	AWG 46	AWG 48
diameter/**mm**	0.3048	0.2667	0.1981	0.1981

The voltage intervals can be increased with changed transistor sizes or increased supply power. However, it consumes more power and die area.

On the other hand, when these cables are applied in ultrasound imaging systems for signal transmission, the number of cables is limited by the available cross-sectional area because of different cable diameters. Table 4.2 presents outer diameters of four cables. It shows the diameter of cable AWG 42 is around 50 percent larger than that of cable AWG 48 or cable AWG 46. For a certain cross-sectional area, accommodated cable counts are different and it leads to different data rates per cross-sectional area.

To compare data rate per cross-sectional area, a catheter with a 2-mm diameter is given. Figure 4.4 illustrates that around 24 AWG 42 can be accommodated in the given area while for AWG 46 or AWG 48, the possible cable count can reach 70, which is almost triple the cable count of AWG 42. However, in Figure 4.1, it can be found that, given acceptable attenuation, the corresponding frequency of AWG 42 is twice that of AWG 46 and triple that of AWG 48. For example, when the attenuation of -15dB is acceptable, the working frequency of AWG 42 can be 3.5 GHz, while that of AWG 48 is 1.2 GHz and that of AWG 46 is 1.7 GHz. Assuming that all the cables are used for signal transmission, AWG 46 would transmit more data per cross-sectional area, followed by AWG 42 and AWG 48. However, it is challenging to integrate many cables together and if each cable is linked to a signal channel, it consumes too much die area and may lead to a power consumption problem. Thus, although AWG 46 may achieve the highest data rate per cross-sectional area among these four types of cables, AWG 42 is more practical.

Thus, AWG 42 is chosen for this project because of its best transmission capacity per cable among the four candidates. Second to AGW 46, AWG 42 can achieve a comparatively high data rate per cross-sectional area as well.

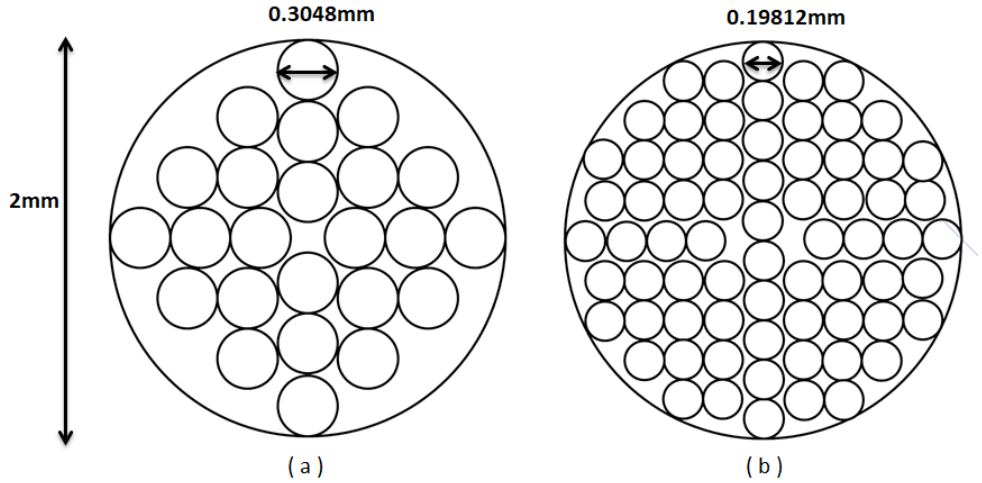

Figure 4.4: Illustration of (a) AWG 42 and (b) AWG 46 or AWG 48 accommodated in a catheter with a 2-mm diameter

4.2 ANALYSIS OF LOAD-MODULATION DATA LINK

As discussed in 4.1, cable AWG 42 is selected for this project about a multi-bit per symbol signalling because of its best transmission capacity per cable and its second highest data rate per cross-sectional area. To decide appropriate specifications of the load-modulation data link, inter-symbol interference should be further analyzed. Otherwise, it would be difficult to choose an appropriate threshold voltage in the decoding process when there are huge variations.

4.2.1 Single-bit per Symbol

The analysis starts with 1-bit per symbol transmission and the schematic is shown in Figure 4.5. The expected interval between two adjacent levels is 80 mV.

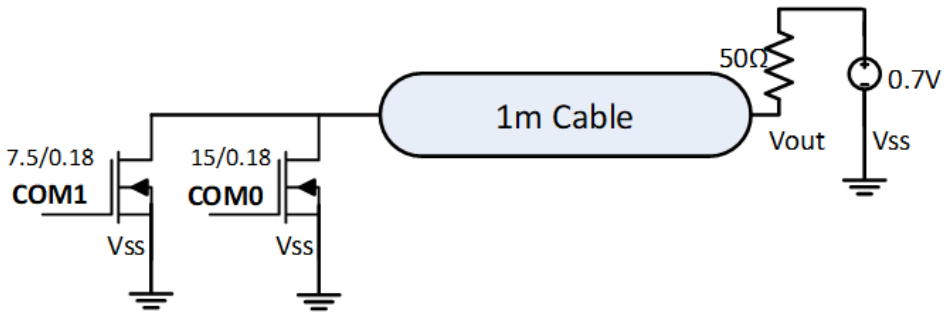

Figure 4.5: Schematic of 1-bit per symbol transmission with an interval of 80 mV

The simulated waveform at V_{out} is presented in Figure 4.6. It can be seen that the waveform associated with a given bit is always influenced by its preceding bit. For example, Point B and Point D represent the same data '1'

but their amplitudes are different. Point D is 375 mV and it is higher than Point B (372 mV). Taking their previous signals into consideration, Point C (310 mV) is higher than Point A (307 mV). Thus, inter-symbol interference leads to variations.

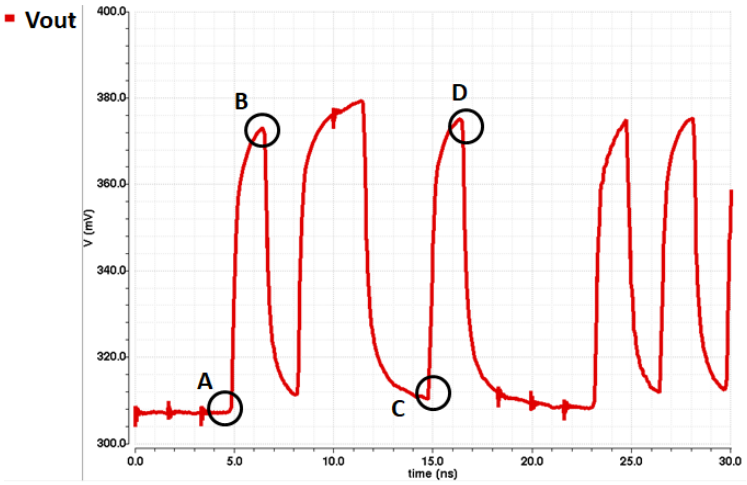

Figure 4.6: Output waveform at the symbol rate of 600 MHz for 1-bit per symbol transmission

Its eye diagrams at several symbol rates are presented in Figure 4.7. V_{range} describes average variation range of these two level and $V_{interval}$ represents the interval between two levels.

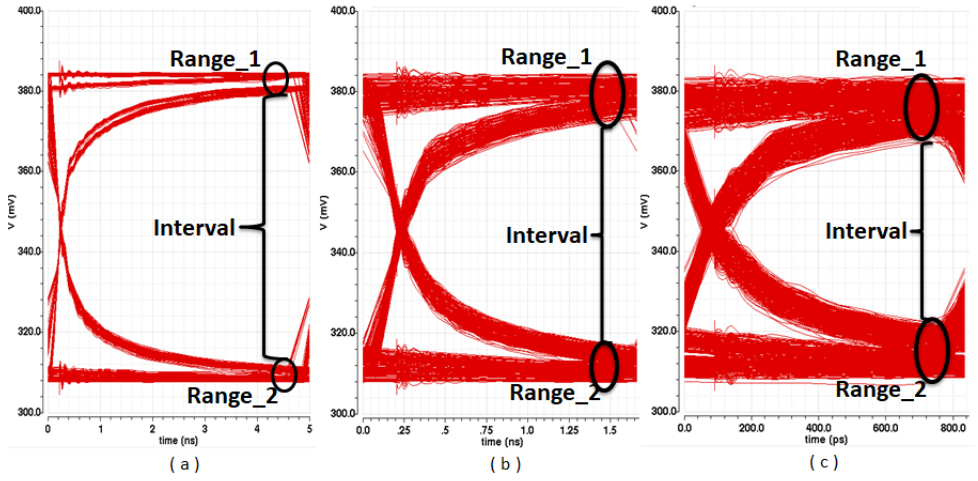

Figure 4.7: Eye diagram at symbol rate of (a) 200 MHz (b) 600 MHz and (c) 1.2 GHz

Table 4.3 shows V_{range} and $V_{interval}$ for this 1-bit per symbol transmission when the expected interval is around 80 mV. It can be found that, with an increased symbol rate, inter-symbol interference is more severe and it causes more obvious variations for the same voltage level. A larger variation range results in a smaller interval between two levels. However, with an increased

signal period, the influence of the previous symbol can be reduced and the signal can be closer to its expected voltage level.

Table 4.3: Comparison of V_{range} and $V_{interval}$ at different symbol rates with the interval of 80 mV

Symbol rate (GHz)	Data rate (Gb/s)	V_{range} (mV)	$V_{interval}$ (mV)
0.2	0.2	4	68
0.6	0.6	10	56
1.2	1.2	15	45

4.2.2 Two-bit per Symbol

The influence of a multi-bit per symbol signalling remains to be explored. A 2-bit per symbol transmission structure is shown in Figure 4.2. The voltage difference between two levels is around 80 mV.

To judge output waveform accuracy, the RLCG-based simulation result is applied to set as a reference first to give a quick idea about what the ideal waveform should be like. The rough comparison is shown in Figure 4.8. It shows that, the corresponding simulated results with a RLCG-based model and an S parameter-based model share a similar waveform.

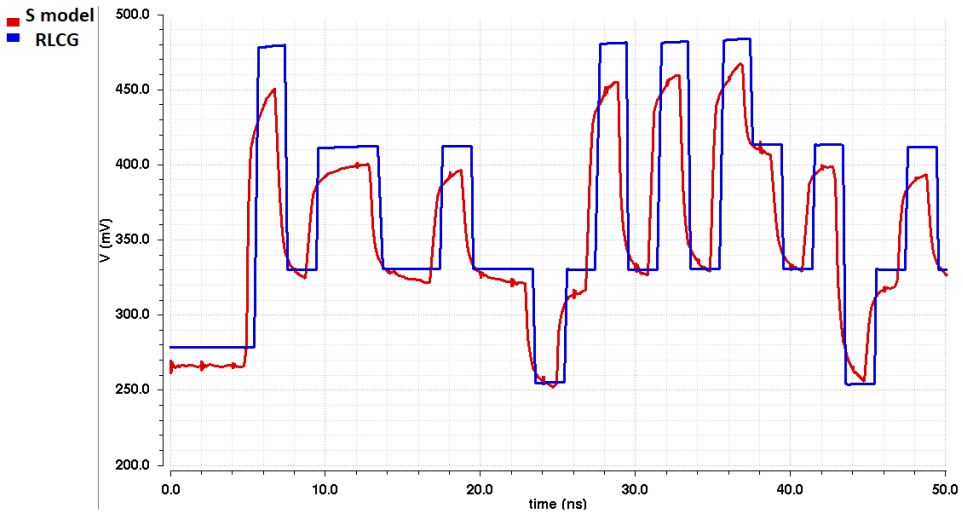

Figure 4.8: Output waveforms from an S parameter-based model and a RLCG-based model for 2-bit per symbol at the symbol rate of 500MHz

In Figure 4.8, the red line represents the output waveform with an S parameter-based cable model and the four voltage levels are between 250 mV and 450 mV. At this time, there are two bits per symbol. The sizes of transistors can be changed and the new schematic in Figure 4.9 can generate an interval of 50 mV between each two levels. The eye diagrams of these two structures at

several symbol rates are presented in Figure 4.10. More V_{range} and $V_{interval}$ at different symbol rates are summarized in Table 4.4. V_{range} describes the average range of variations for different voltage levels while $V_{interval}$ describes the average interval.

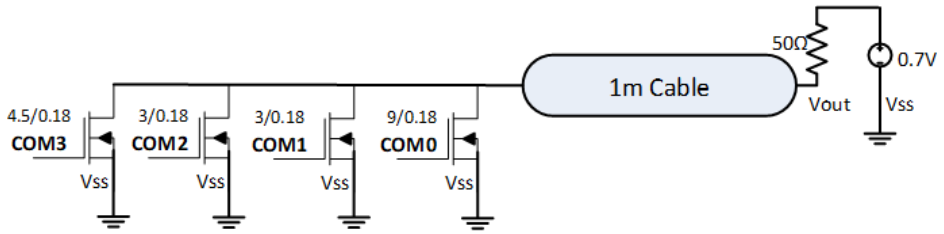

Figure 4.9: Schematic of 2-bit per symbol transmission with an interval of 50 mV

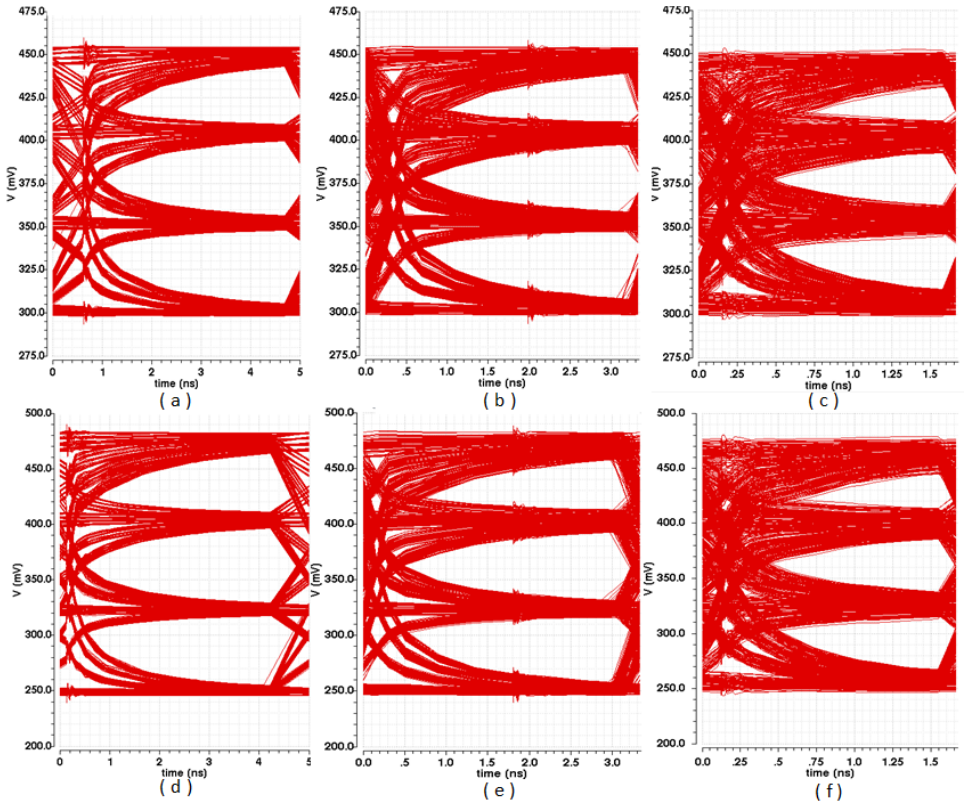

Figure 4.10: Eye diagram at the symbol rate of (a) 200 MHz with a 50 mV interval (b) 300 MHz with a 50 mV interval (c) 600 MHz with a 50 mV interval (d) 200 MHz with an 80 mV interval (e) 300 MHz with an 80 mV interval and (f) 600 MHz with an 80 mV interval for a 2-bit per symbol signalling

In Table 4.3, although intervals between two levels are different, V_{range} increases with the symbol rate. However, with a larger interval, inter-symbol interference is more severe and it leads to a larger variation. Also, the relationship between voltage levels and inter-symbol interference can be ac-

Table 4.4: Comparison of V_{range} and $V_{interval}$ at different symbol rates

		80 mV interval		50 mV interval	
Symbol rate (GHz)	Data rate (Gb/s)	V_{range} (mV)	$V_{interval}$ (mV)	V_{range} (mV)	$V_{interval}$ (mV)
0.1	0.2	7	70	5	46
0.2	0.4	14	59	8	40
0.3	0.6	18	55	11	35
0.5	1	24	45	16	29
0.6	1.2	26	43	17	27

Table 4.5: Thermometer coding for 3-bit per symbol transmission

Input Data	COM1	COM2	COM3	COM4	COM5	COM6	COM7
111	1	1	1	1	1	1	1
011	1	1	1	1	1	1	0
101	1	1	1	1	1	0	0
001	1	1	1	1	0	0	0
110	1	1	1	0	0	0	0
010	1	1	0	0	0	0	0
100	1	0	0	0	0	0	0
000	0	0	0	0	0	0	0

quired from Table 4.4 and Table 4.3. Considering the condition of an 80 mV interval, with increased voltage levels, variations increase at the same symbol rate. Thus, more voltage levels lead to more severe inter-symbol interference. This relationship also indicates the possibility that, to achieve a certain data rate, a 2-bit per symbol signalling can be better than a 1-bit signalling because the symbol rate of the 2-bit signalling is half of that of the one-bit signalling. With the same expected interval, the 2-bit signalling generates a larger $V_{interval}$ and it allows for the existence of non-idealities like noise, which increases transmission accuracy.

4.2.3 Three-bit per Symbol

To further increase the data rate, one could further increase the symbol rate but it leads to more serious attenuation and more severe inter-symbol interference. Thus, more than 2-bit per symbol can be considered. To ease comparisons, the 700 mV supply power is fixed at the system side. Thus, four more voltage levels can be used to generate a 3-bit per symbol signalling when the expected interval of 80 mV remains. The thermometer coding for this 3-bit transmission is presented in Table 4.5 and the load-modulation structure is shown in Figure 4.11. COM0 is always turned on.

Simulated output waveforms at V_{out} are shown in Figure 4.12. The red waveform represents the output signal generated from an S parameter-based cable model while the blue one represents the output signal based on a RLCG-

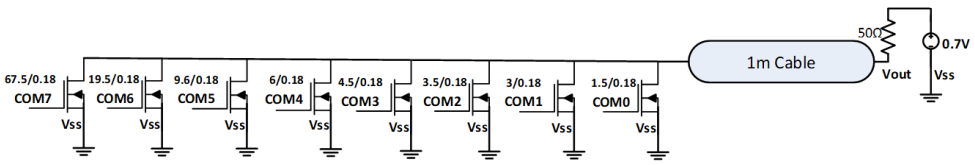

Figure 4.11: Schematic of 3-bit per symbol transmission with an interval of 80 mV

based cable model. Both of them share a similar waveform.

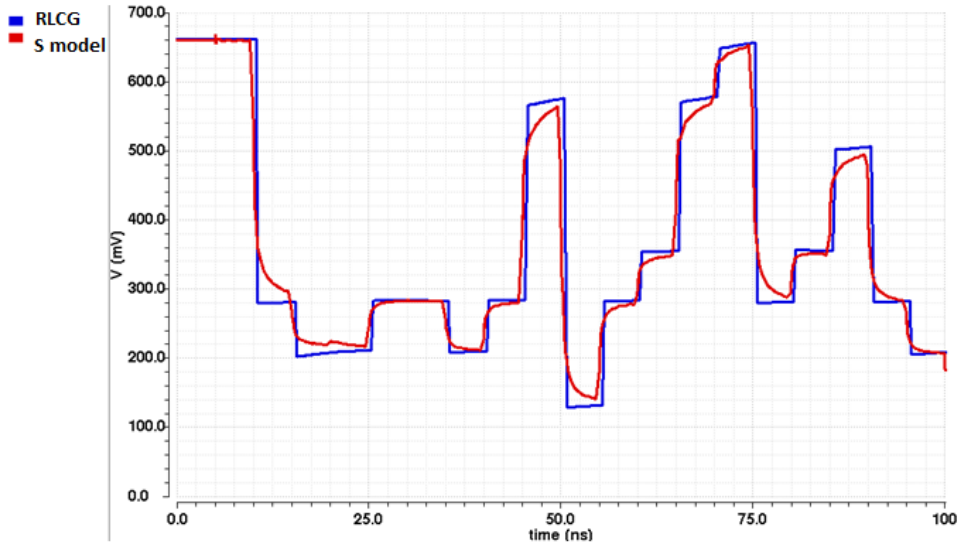

Figure 4.12: Output waveforms with S parameter model and RLCG model for 3-bit per symbol at the symbol rate of 200MHz

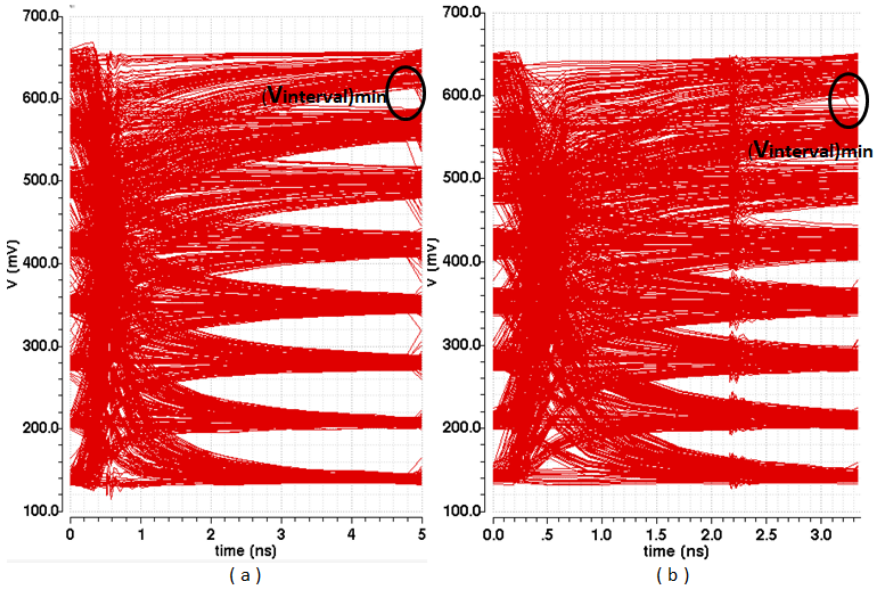

Figure 4.13: Eye Diagram of a 3-bit per symbol signalling with an interval of 80 mV at the symbol rate of (a) 200 MHz and (b) 300 MHz

In 4.13, when there are more voltage levels, the inter-symbol interference is more severe and the real interval is reduced. The minimum interval for this 3-bit per symbol signalling is 25 mV while the minimum interval for a 2-bit per symbol signalling is 53 mV at the same symbol rate. If the symbol rate of this 3-bit signalling is further increased, its minimum interval will decrease to 8 mV. However, several threshold voltages can be derived from the corresponding eye diagram at the symbol rate of 200 MHz. When the simulation time is increased to 50 µs, there is no error and its BER number is 0. It achieves the same data rate of 600 Mb/s but BER number is much lower than [16]. Thus, 80 mV might not be the optimum interval for 3-bit transmission because more levels leads to more severe inter-symbol interference but a 3-bit signalling can be a candidate to increase the data rate.

Thus, the objective bit per symbol of the load-modulation data link can be 3. Although the inter-symbol interference is more severe when there are more levels, it is worth investigating its transmission capacity through AGW 42. 3-bit signalling can achieve the same data rate with a lower symbol rate, which reduces the design specifications of other blocks like an ADC in a signal channel. Also, the target symbol rate is 600 MHz. As discussed in this section, 2-bit per symbol transmission performs well at the symbol rate of 600 MHz. With a comparatively large interval in the simulation, the signalling is robust against some non-idealities, which provides better transmission accuracy. In this case, its data rate can achieve 1.2 Gb/s and it is higher among load-modulation transmission in IVUS applications.

4.3 COMPLETE ARCHITECTURE WITH LOAD–MODULATION DATA LINK

A system architecture with a next-generation load-modulation data link with multi-bit per symbol signalling is proposed in Figure 4.14. It requires only one cable for signal transmission. Its achievable data rate is decided by the number of signal channels and the specifications of the ADC in the signal channels.

Transducers are interfaced with three signal channels and each channel is composed of an m-1 analog multiplexer, an AFE and an ADC for local digitization. ADC outputs are sent to a FIFO for synchronization. Then, the decoder will transfer three bits to seven bits to generate control signals. Using thermometer coding, these seven signals can control seven transistors with eight conditions. Thus, observed at V_{out}, there are eight voltage levels, which makes a 3-bit per symbol signalling possible. The data rate is decided by the specifications of the ADC in a signal channel. If a 60 MS/s 10-bit ADC is employed, ideally the data rate can reach 1.8 Gb/s.

With the output waveform at V_{out}, this data link can generate eight volt-

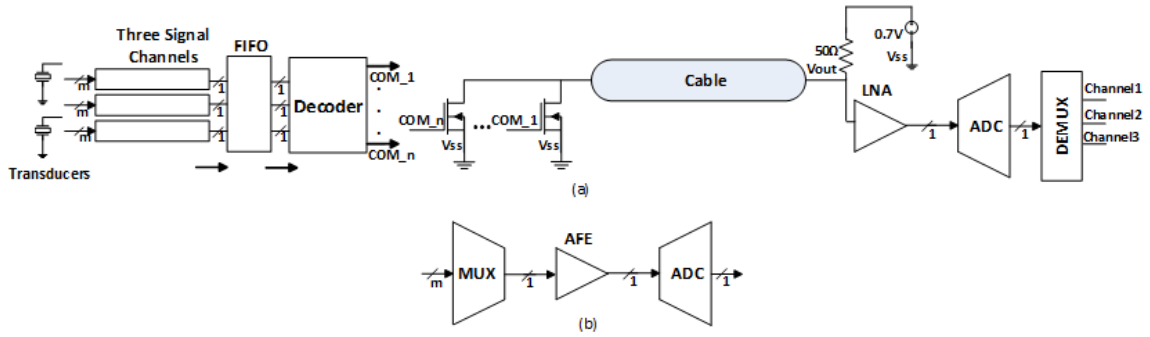

Figure 4.14: (a) A complete system architecture with load-modulation data link (b) A block diagram of a signal channel

age levels at V_{out}. IT can be amplified first and with an appropriate choice of threshold voltages, an ADC can be applied to capture the waveform from the LNA output and categorize signals into eight groups. Each group has its corresponding combination of three ADC outputs.

4.4 LOAD-MODULATION DATA LINK WITH MULTI-BIT PER SYMBOL SIGNALLING

To simplify this project, signal channels in Figure 4.14 will be replaced by an FPGA to mimic ADC outputs and only the data link part will be integrated on a test chip.

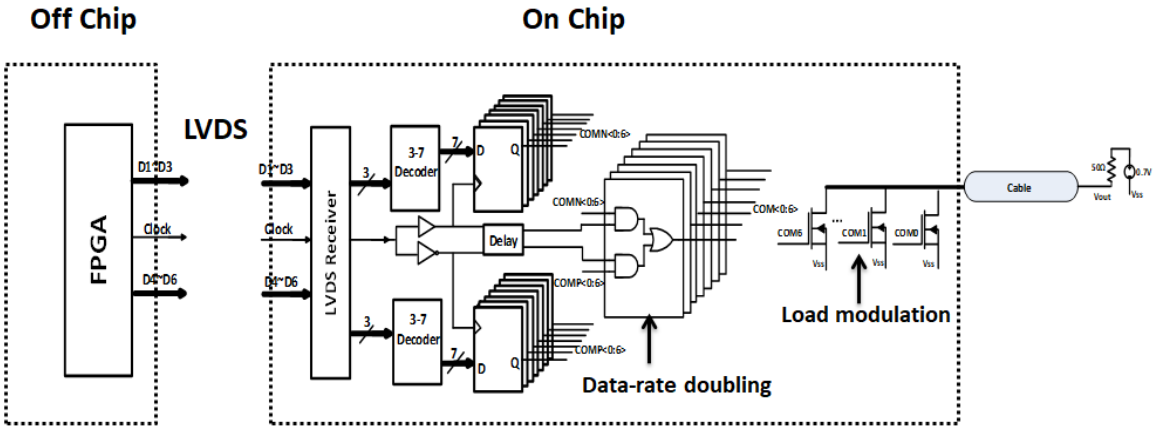

Figure 4.15: Architecture of a load-modulation data link with multi-bit per symbol signalling

A random number sequence will be used to evaluate the data link performance. The random numbers is generated off-chip. On one hand, compared with on-chip number generators, it eases design complexity. On the other hand, they can be generated by Pseudo-Random Number Generators (PRNGs) on FPGA. These numbers can be recorded to provide a reference for BER calculation. Also, some numbers can be fixed as '0' or '1', which

brings more possibility of investigating signal transmission capacity with this load-modulation data link. More specifically, there are three PRNGs to generate three-bit random numbers. To analyse a two-bit per symbol signalling, one of them can be fixed so that there will be only two-bit random numbers and it results in a 2-bit per symbol signalling. It applies to 1-bit per symbol signalling as well. However, the data rate of random numbers is limited by the clock generated on FPGA. It is difficult to implement a high-speed clock on a normal FPGA and thus it limits the symbol rate in signal transmission.

To reduce the data rate between the FPGA and chip, two parallel data paths are applied. In Figure 4.15, six random numbers are generated according to the clock on FPGA and the data rate of each number is equal to clock frequency. Three of them are generated at the rising edge of the clock while the others are generated at the falling edge, which naturally generates two parallel data paths. In every data path, three data are sent to a 3-7 decoder on chip first. With a proper timing diagram in Figure 4.16, data from two paths can be combined into one path, which doubles data rate. Also, with this data-rate doubling structure, return-to-zero stages can be generated when three numbers in one data path are fixed.

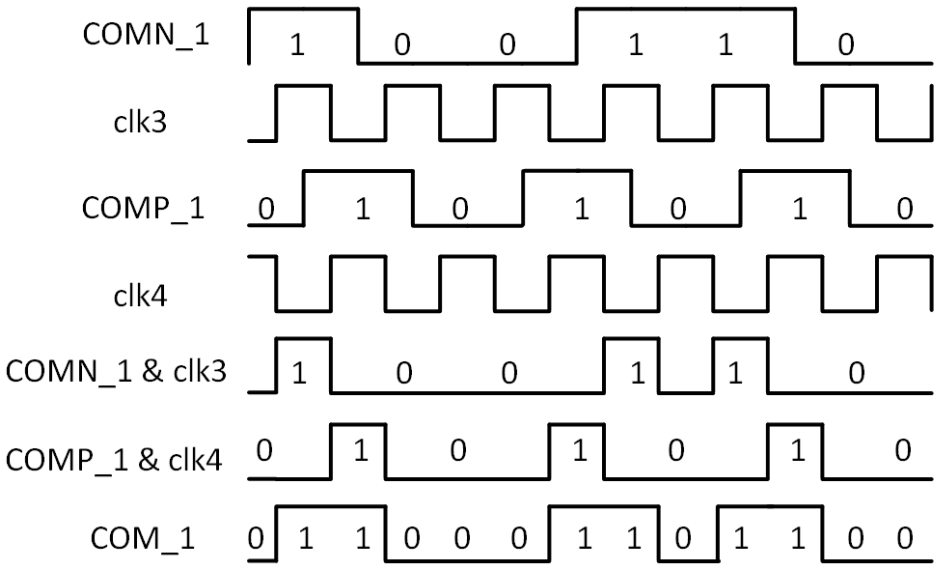

Figure 4.16: Timing diagram of data-rate doubling

Seven data streams are used to drive seven MOS transistors. It can generate eight different voltage levels at V_{out}. The waveform can be acquired by an active probe with 2.5-GHz bandwidth (YOKOGAWA PBA25000) and a high-performance oscilloscope with 2-GHz bandwidth (Infiniium DSO80204B) and then decoded in MATLAB on a PC. Moreover, with recorded random numbers on FPGA, a BER number can be calculated to judge the accuracy of signal transmission.

Furthermore, this data link is versatile in investigating different transmission conditions with tunable FPGA setup. First, the clock frequency can be

changed to provide different symbol rates. Second, several input data can be fixed to investigate the 1-bit or 2-bit per symbol signalling. Also, as mentioned above, it can generate return-to-zero stages although the maximum bit per symbol is reduced to 2.

5 LOAD-MODULATION TEST ASIC

This chapter describes implementation details of different blocks in this test ASIC. These blocks can be divided into two main parts: load modulation and data-rate doubling. For load modulation, its topology is the main concern. Apart from thermometer decoding that has been applied in previous chapters, one-hot coding will be explored. The data-rate doubling part starts with a description of an ideal data-rate doubling circuit. More sub-blocks like synchronization and overlapping clocks are applied to make it more robust against non-idealities. After the discussion about components integrated on chip, the floor plan and layout of this ASIC will be discussed.

5.1 SYSTEM DESCRIPTION

In the previous chapter, an experimental setup for evaluating a load-modulation data link with multi-bit per symbol signalling has been proposed. For flexibility, the data-transmission side of this setup has been divided into two parts: an ASIC with the load-modulation circuit, and an FPGA that controls the ASIC and provides a data stream for test.

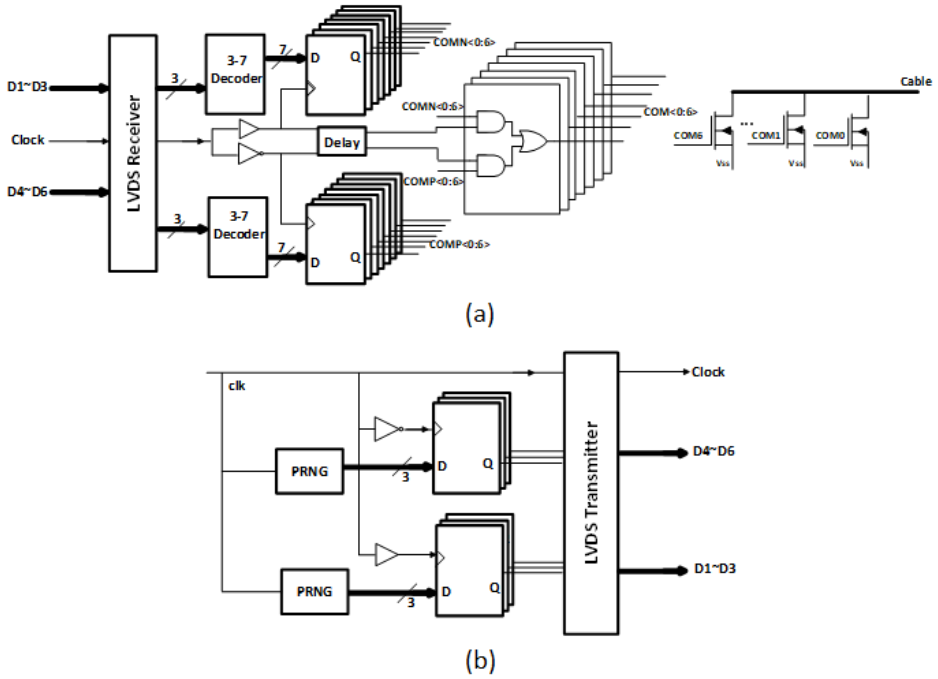

Figure 5.1: A block diagram of (a) the on-chip circuitry and (b) the FPGA

A complete architecture is shown in Figure 5.1. LVDS is applied to transmits a clock signal and six random data streams from the FPGA to the chip. LVDS receiver circuits are adopted to convert differential signals to single-ended signals on chip. Seven signals, COM1-COM7, are used to control load modulation to generate eight different equivalent resistance.

This system requires only one cable for signal transmission and helps investigate the multi-level signalling transmission capacity. With manageable

FPGA setup, it allows for a symbol rate up to 600 MHz and the maximum bits per symbol can be 3.

5.2 LOAD MODULATION

In this section, the load-modulation topology will be decided. One-hot coding will be compared with thermometer coding first, which leads to the specification of a decoder. Furthermore, the linearity of this load modulation will be discussed. In terms of die area, the size of transistors will be optimized.

5.2.1 Thermometer Coding

In 4.2, thermometer coding has been applied in the load-modulation data link to help investigate the multi-bit per symbol transmission capacity through AWG 42. Table 5.1 gives an example of thermometer coding with seven control signals. When there are seven control signals, it can generate eight different cases.

Table 5.1: One example of thermometer coding with seven control signals

	COM7	COM6	COM5	COM4	COM3	COM2	COM1
$Case_1$	1	1	1	1	1	1	1
$Case_2$	0	1	1	1	1	1	1
$Case_3$	0	0	1	1	1	1	1
$Case_4$	0	0	0	1	1	1	1
$Case_5$	0	0	0	0	1	1	1
$Case_6$	0	0	0	0	0	1	1
$Case_7$	0	0	0	0	0	0	1
$Case_8$	0	0	0	0	0	0	0

For a 3-bit binary code, its corresponding thermometer code has 7 control signals. Each signal controls one MOS transistor and it can generate eight different equivalent impedance at the chip side. To reduce complexity, a unit transistor will be applied to implement load-modulation schematics with different requirements in this chapter. The unit size is 1.5µm/0.18µm.

The schematic with thermometer coding in Figure 4.11 is proposed for comparison with one-hot coding. It allows for 3-bit per symbol signalling and its interval between two levels is around 70 mV. Compared with an 80 mV interval in 4.2, 70 mV suffers less from inter-symbol interference. With a large desired interval, it is worth investigating its transmission capacity.

Another potential coding method is one-hot coding. To generate 3-bit per symbol signalling, eight control signals are required. Each of them controls one MOS transistor respectively. Its coding logic for 3-bit per symbol trans-

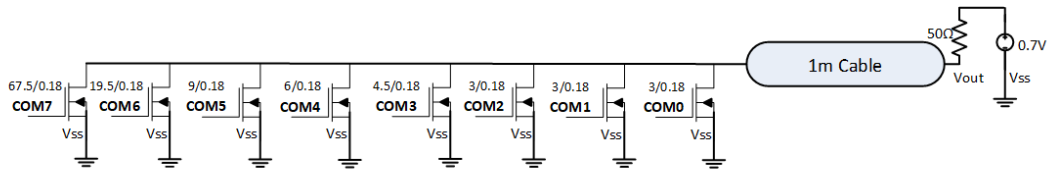

Figure 5.2: Schematic of 3-bit per symbol transmission with thermometer coding

mission is shown in Table 5.2. To compare with the load-modulation with thermometer coding, its corresponding schematic is presented in Figure 5.3. For the same 3-bit binary input, the corresponding expected voltage values V_{out} in these two schematics are almost same.

Table 5.2: One-hot coding for 3-bit per symbol transmission

Input Data	COM1	COM2	COM3	COM4	COM5	COM6	COM7	COM8
111	0	0	0	0	0	0	0	1
011	0	0	0	0	0	0	1	0
101	0	0	0	0	0	1	0	0
001	0	0	0	0	1	0	0	0
110	0	0	0	1	0	0	0	0
010	0	0	1	0	0	0	0	0
100	0	1	0	0	0	0	0	0
000	1	0	0	0	0	0	0	0

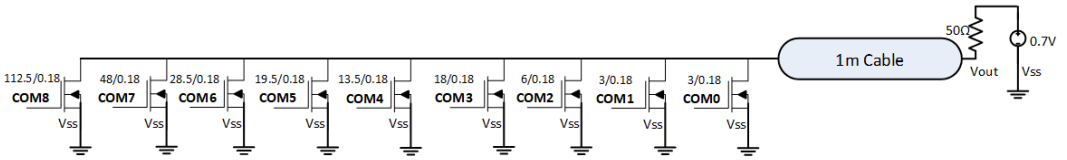

Figure 5.3: Schematic of 3-bit per symbol transmission with one-hot coding

Figure 5.4 shows V_{out} in two load-modulation schematics with different coding methods. The red line represents V_{out} when one-hot coding is applied while the other represents V_{out} generated with thermometer coding. These two waveforms are almost overlapped.

In addition, several inverters should be applied to drive the gates of transistors. The gate drivers for two schematics are presented in Figure 5.5. Due to the larger size of transistors in the one-hot coding structure, it requires the gate driver with a stronger driving ability.

To verify the driving ability of gate drivers, eight signals are all replaced by a pulse wave in two schematics. Thus, corresponding driving signals COM_0 -COM_7 processed by gate drivers in two schematics are presented in Figure 5.6. In each schematic, there is no obvious delay between two driving sig-

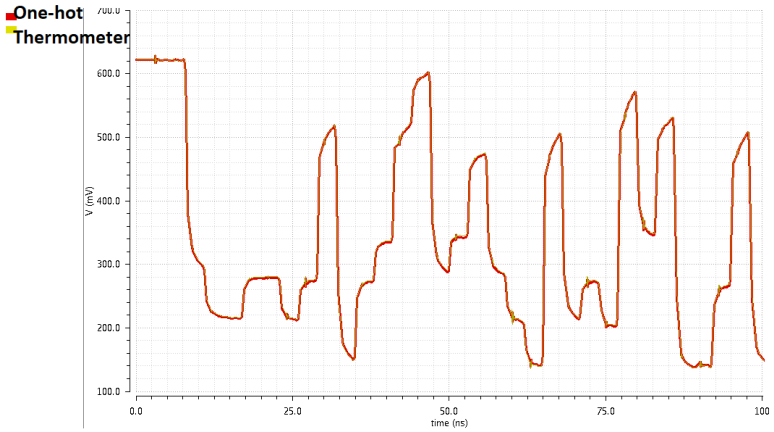

Figure 5.4: V_{out} of schematics with one-hot coding and thermometer coding at the symbol rate of 333 MHz

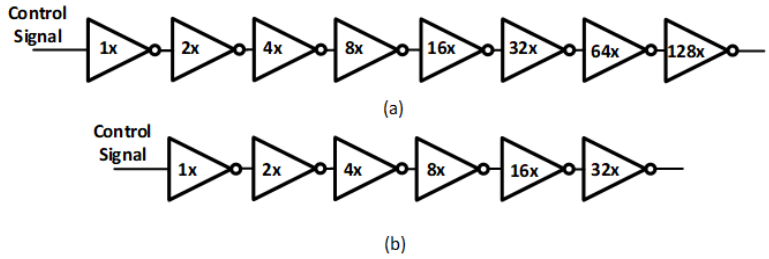

Figure 5.5: (a) Gate driver for one-hot coding structure data link (b) Gate driver for thermometer coding structure data link

nals. Also, a stronger gate driver leads to a longer delay.

Power of this data link is consumed by the load-modulation circuit itself and gate drivers. For these two schematics with different coding methods, they have the same voltage levels and the power consumption of each load-modulation circuit is around 1.46 mW. However, due to different driving abilities, the gate driver for one-hot coding structure consumes 3.12 mW while the other consumes 1.472 mW.

Also, it terms of their die areas, thermometer coding requires 75 unit transistors while one-hot coding requires 160 unit transistors. Implementation of thermometer coding saves much more die area.

Thus, thermometer coding is adopted for the load-modulation data link in terms of power consumption, response time and die area.

5.2.2 Resistive Degeneration

For a MOS transistor, its on-resistance is influenced by the voltage drop between its drain and source. With different V_{ds}, its on-resistance is different. At the supply voltage of 700 mV, intervals between two adjacent voltages can be fixed in previous load-modulation data link schematics. However, when the supply voltage changes, each voltage level at V_{out} cannot change linearly

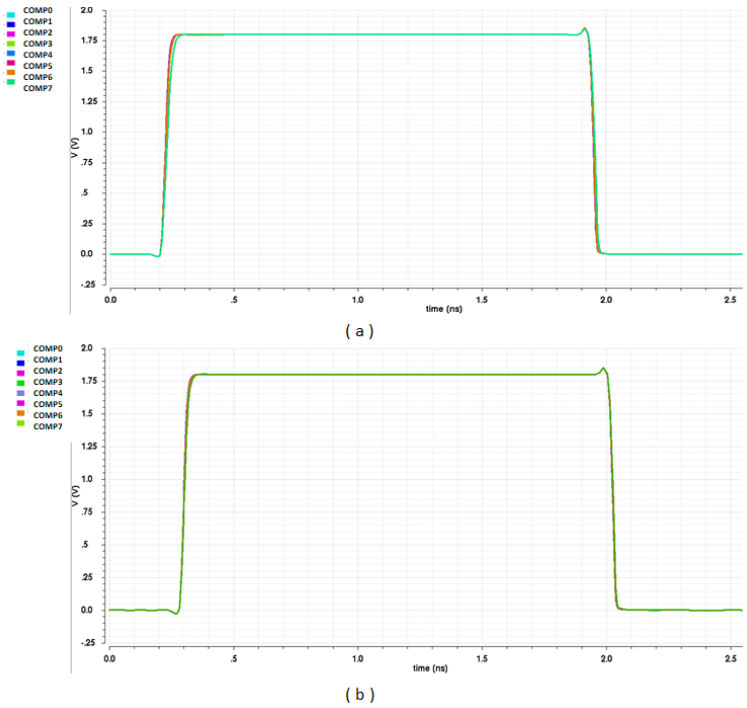

Figure 5.6: (a) Driving signals of transistors with one-hot coding (b) Driving signals of transistors with thermometer coding

because the on-resistance of MOS transistors changes. Thus, in this section, the linearity of the load-modulation data link is analyzed.

In previous schematics, resistance is provided by MOS transistors. When they are turned on, they can be seen as resistors with certain resistance values but this value is relevant to V_{ds}. This relevance brings non-linearity. To increase the linearity of the data link, the influence of MOS resistance should be minimized. Thus, each transistor in Figure 4.11 can be replaced with a switch and a resistor with a fixed value. The switch is implemented by a large-size transistor. The new schematic with resistive degeneration is presented in Figure 5.7.

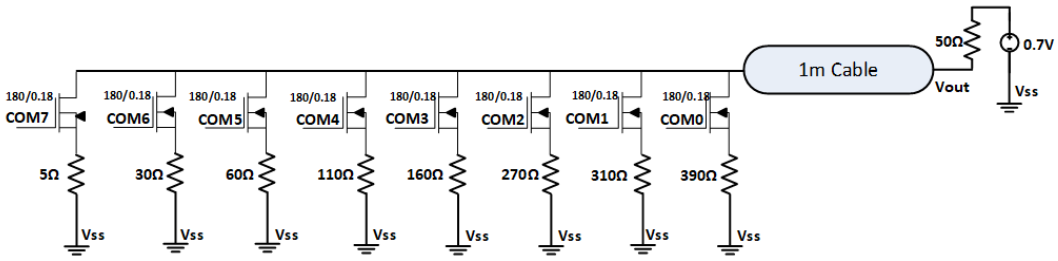

Figure 5.7: Schematic of a 3-bit signalling with resistive degeneration

When the supply voltage is increased to 0.8 mV, the new voltage levels of schematics with and without resistive degeneration can be summarized in Table 5.3. V_{new1} describes the new voltage levels for the load modulation

Table 5.3: Comparison of voltage levels at 800 mV supply voltage

Expected voltage level (mV)	V_{new1} (mV)	V_{new2} (mV)
709	718	710
627	642	626
555	572	552
467	482	465
384	395	384
305	312	300
220	223	223
137	138	137

without resistive degeneration while V_{new2} describes the new voltage levels for the load modulation with resistive degeneration. It can be found that when the supply voltage increases, values of new levels generated in a load-modulation data link with resistive degeneration are almost same as expected voltage values. Thus, resistive degeneration increases linearity of load modulation.

However, in terms of die area, each switch requires 120 unit transistors, which occupies much more die area. Also, as discussed in the last subsection, a large-sized transistor requires a strong gate driver. It consumes more power and leads to a longer response delay.

To conclude, resistive degeneration brings more linearity but it is at the expense of power, speed and die area. Compared with linearity, die area and power can be more important in ultrasound applications and thus, resistive degeneration will be not applied to this load-modulation data link.

5.2.3 Die Area Optimization

The 3-bit per symbol transmission that has been discussed in Figure 5.3 requires 75 unit transistors. The interval between its two adjacent voltage levels is around 70 mV. However, as discussed in 4.2, with increased voltage levels, inter-symbol interference is more severe and for multi-bit signalling, an increased expected interval between two levels suffers more from inter-symbol interference as well. To further increase the symbol rate when there are three bits, the interval should be decided and it is relevant to transistor sizes. Also, when the interval is fixed, the placement arrangement of eight levels should be analyzed. When all these levels are comparatively lower, it schematic will require more transistors because of smaller equivalent impedance. Thus, in this section, sizes of transistors can be further optimized for die area optimization.

First, the interval between two adjacent is discussed to choose a comparatively suitable value for three-bit signalling. Another three schematics with different intervals (40 mV, 50 mV and 60 mV) are proposed to compare with the load-modulation structure with an interval of 70 mV. With an in-

creased interval, the number of required unit transistors increase. Three new schematics require 36, 59 and 63 transistors for implementation. To compare their transmission ability, the symbol rate is set as 250 MHz. Their corresponding eye diagrams are presented in Figure 5.8. In each eye diagram, there is a black curve and it represents the smallest variation and the largest interval. $V_{average}$ describes the average variation while $V_{interval}$ represents the smallest interval. They are represented in Table 5.4.

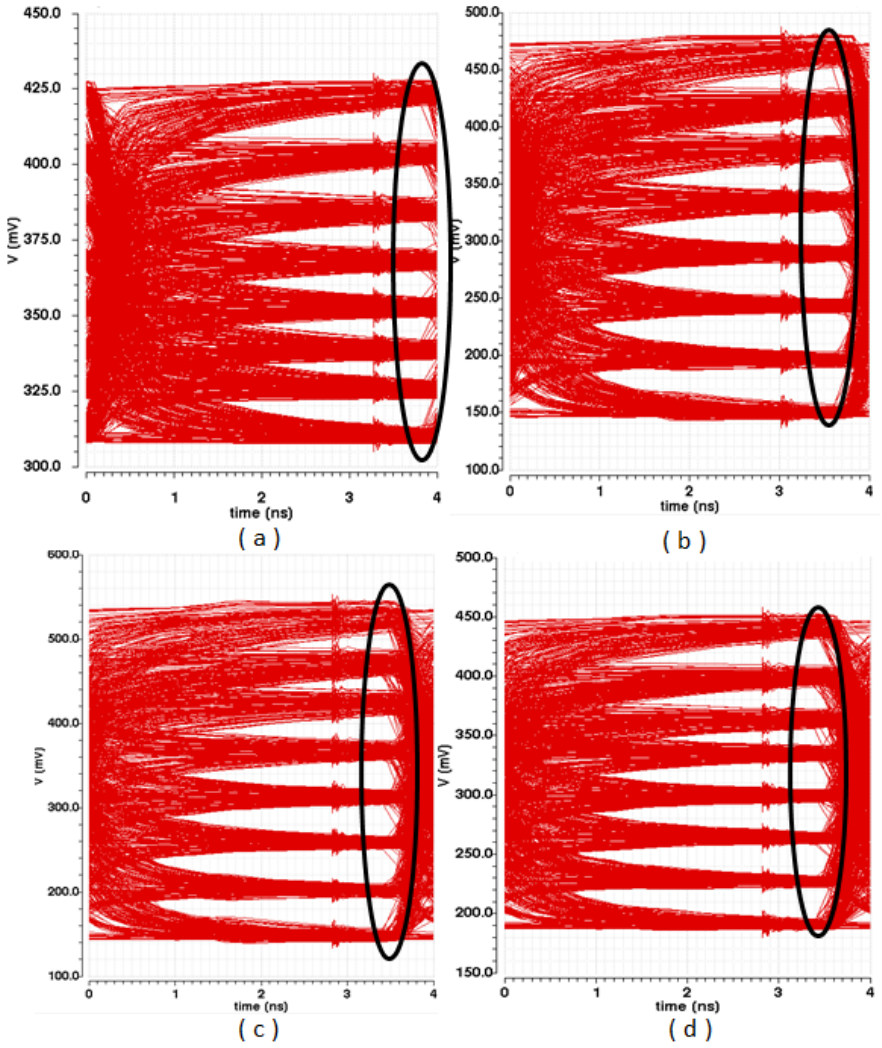

Figure 5.8: Eye diagram of schematics with an interval of (a) 40 mV (b) 50 mV (c) 60 mV and (c) 70 mV at the symbol rate of 250 MHz

In Table 5.4, it can be found when the interval is 50 mV or 60 mV, $V_{interval}$ is the highest and the number of unit transistors are similar. Thus, they can be good candidates. Shown in Figure 5.9, when the symbol rate is further increased to 300 MHz, both variations become larger and the intervals are further reduced. $V_{interval}$ of the schematic with an interval of 50 mV is 10 mV and it is reduced to 8 mV when the interval is 60 mV. It verifies that the larger interval suffers more from inter-symbol interference and the interval of 50 mV should be applied in this load-modulation data link.

Table 5.4: Comparison of intervals between expected situations and real situations

Expected interval (mV)	$V_{interval}$ (mV)	$V_{average}$ (mV)
40	14	16
50	17	17
60	17	23
70	14	31

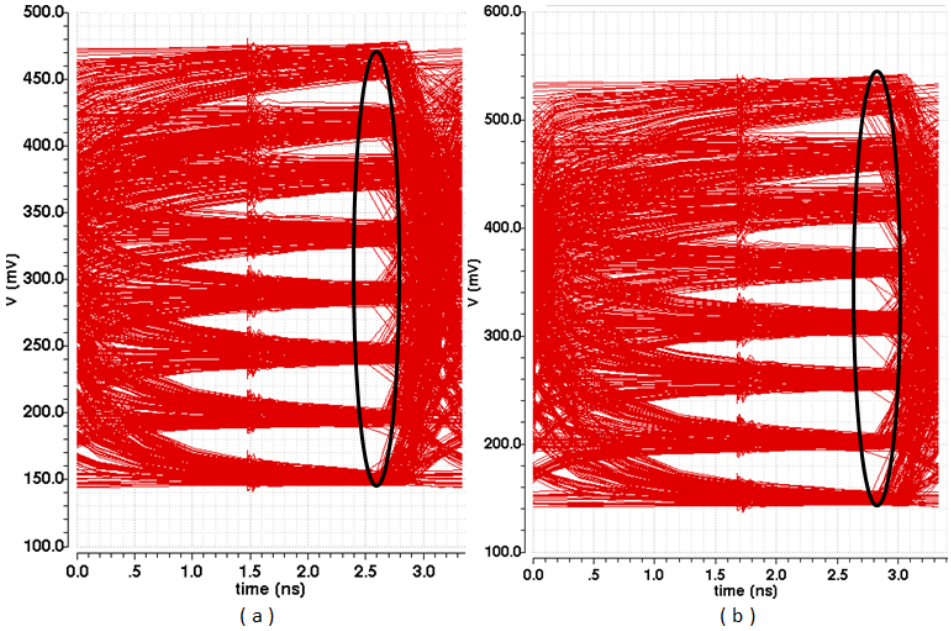

Figure 5.9: Eye diagram of schematics with an interval of (a) 50 mV and (b) 60 mV at the symbol rate of 300 MHz

Furthermore, with a fixed interval, eight levels can be placed in the upper side of 700 mV or in the lower side. In Figure 5.10, it shows the eye diagrams when the eight levels are placed at different places.The actual intervals are similar. However, when the eight levels are placed in the upper side, the average interval is higher but it consumes 1.824 mW, which is higher than the other two situations. When eight levels are placed in the lower side, it consumes 1.248 mW only. However, it occupies too much die area and also the sizes of transistors are large. The large-sized transistors require power-hungry gate drivers. Thus, in terms of power consumption and die area, eight levels are placed around the middle. Figure 5.11 describes its implementation.

5.3 DATA-RATE DOUBLING

The data-rate doubling is another important part of this system. It combines two parallel 3-bit data streams into one data stream and helps increase the symbol rate. An ideal doubling circuit is described first, followed by some sub-blocks to make data-rate doubling more reliable.

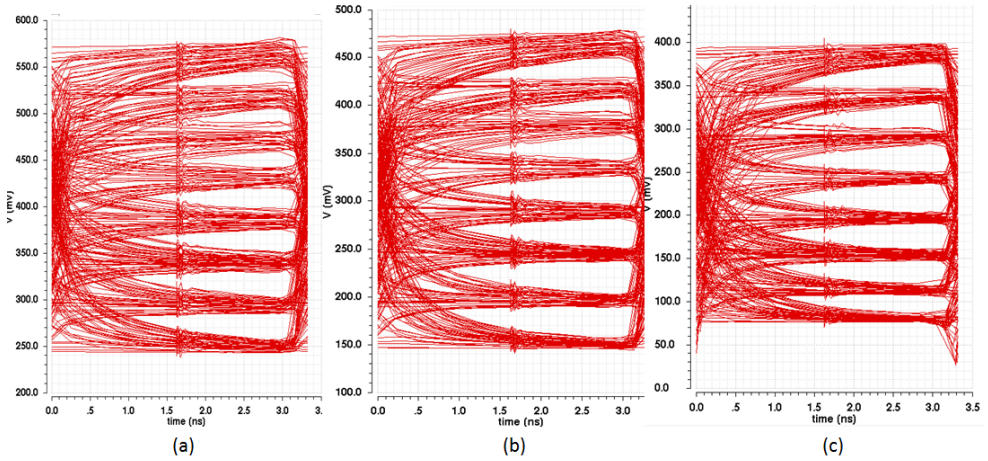

Figure 5.10: Eye diagram of schematics with levels (a) in the upper side (b) in the middle and (c) in the lower side at the symbol rate of 300 MHz

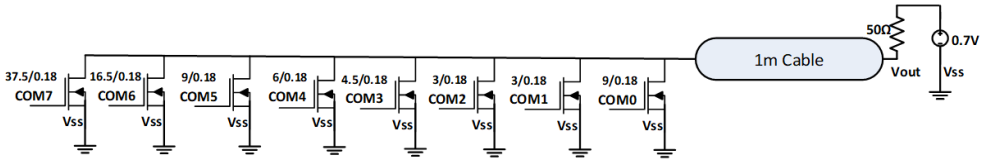

Figure 5.11: Implementation of a load-modulation data link with an interval of 50 mV

5.3.1 Ideal Data-rate Doubling Circuit

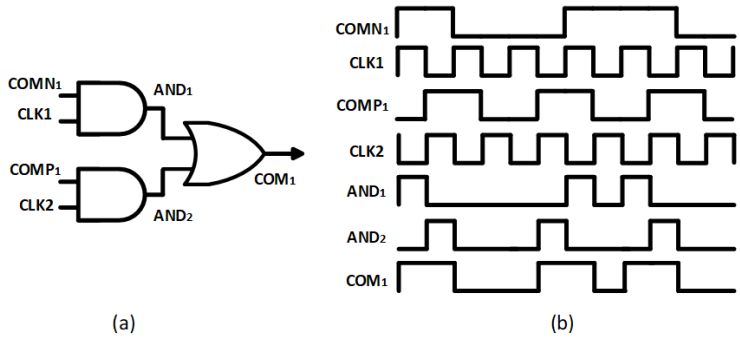

Figure 5.12: (a) Logic cells of data-rate doubling and (b) Timing diagram of data-rate doubling

In Figure 5.12, data-rate doubling is implemented with two AND gates and one OR gate. Two overlapping clocks, $CLK1$ and $CLK2$, are sent into two AND gates respectively. Signal $COMP_1$ is half a clock period slower than $COMN_1$. Outputs of AND gates, AND_1 and AND_2 can be combined together.

This doubling circuit is implemented by cells in the standard digital library in Cadence and it eliminates a complex design like serialization. However, the timing diagram indicates that the performance of this schematic can be

easily influenced by some non-idealities like non-overlapping clocks. They will be discussed and compensated to increase its working reliability.

5.3.2 Overlapping Clock

In Figure 5.12, two clocks $CLK1$ and $CLK2$ are overlapping and it reduces the possibility of glitches in the output wave. A new timing diagram in Figure 5.13 illustrates the generation of glitches when these two clocks are non-overlapping.

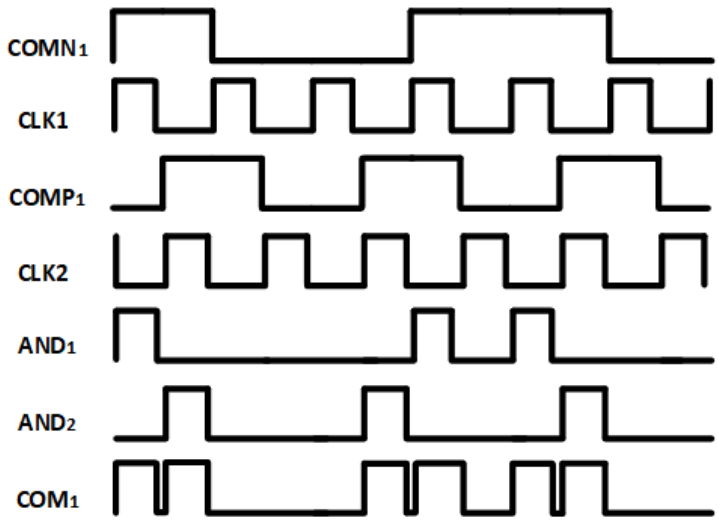

Figure 5.13: Timing diagram of data-rate doubling with non-overlapping clocks

Due to non-overlapping clocks, there might be a short period of a low-level stage between two high-level stages at COM_1. The equivalent resistance is changed during this short period and it will cause a glitch between two voltage levels. Also, due to the existence of a short period of the low-level stage, the period of the two high-level stages is less than half of the clock period. Their corresponding signal frequency increases and it leads to more attenuation.

Thus, overlapping clocks should be applied to the data-rate doubling cell and they can be generated by the LVDS receiver in Figure 5.1 directly.

The receiver circuit is composed of a positive-feedback latched comparator, common-source amplifiers and buffers in Figure 5.14. Normally, it transforms small differential signals from LVDS transmission to single-ended signals. In terms of its fully symmetrical structure, it can generate overlapping clocks when both of its outputs are used. The recovery circuit eliminates another block to generate overlapping clocks on chip, which reduces system complexity and saves die area.

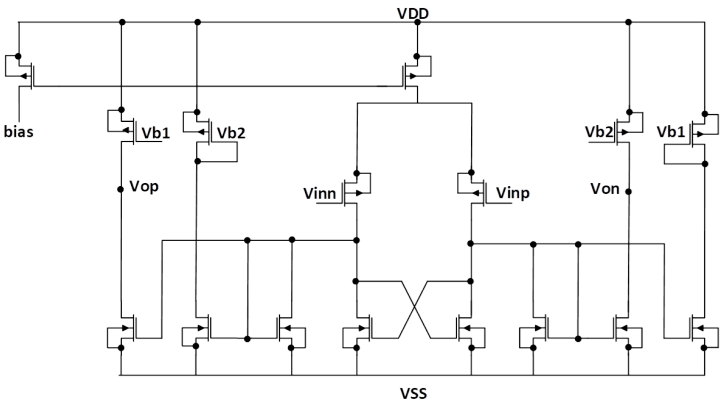

Figure 5.14: Circuit of LVDS receiver

5.3.3 Synchronization

Two parallel 3-bit data streams are transmitted and processed at the same time. For each data stream, 3-bit random numbers are generated according to the same clock and ideally there is not any delay between two bits. In terms of transmission delay from LVDS transmission, these three bits might arrive at the input of a 3-7 decoder at different times. As is shown in Figure 5.15, due to different transmission delay, D_2 arrives at the input of the 3-7 decoder later than D_1 and D_3. Thus, the decoder will decode '100' first and then '110'. The additional '100' will generate an error. Thus, 3-bit random numbers should be synchronized.

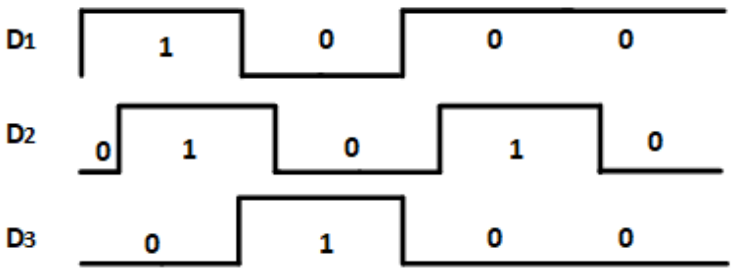

Figure 5.15: Three data streams with some delay at the input of 3-7 decoder

Also, before being sent into the inputs of a data-rate doubling cell, outputs of a 3-7 decoder should be synchronized. The reason is that these seven data don't experience the exactly same processing process and it might lead to some delay between each other. This uncertainty makes it more difficult to sample seven signals with the same sampling clock correctly in the data-rate doubling process.

These two synchronization can be both realized on chip. A clock can be applied to synchronize inputs of a 3-7 decoder first and outputs of this decoder can be synchronized when additional delay is applied to the clock.

However, due to different transmission time of signals and clock and different number generation time of the decoder, it is hard to decide the additional delay accurately. Any variations may lead to a system failure. Thus, a more reliable synchronization structure should be applied.

A 2-FlipFlop synchronizer can be applied in this test ASIC for synchronization and its working principle is illustrated in Figure 5.16. There are two kinds of paths. One is for signals while the other is for clock.

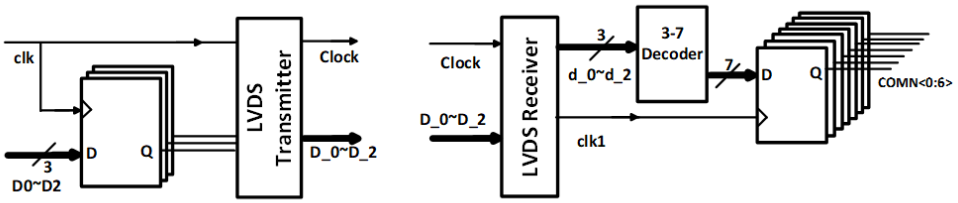

Figure 5.16: A synchronization structure

D_1,D_2 and D_3 are synchronized first off-chip. With the same processing process, it can be assumed that it takes them the same time to arrive at the input of FlipFlop1. The transmission time of d_0 and $clk1$ can be expressed as follow:

$$t_{d_0} = t_{FlipFlop} + t_{LVDStransmitter} + t_{wire} + t_{LVDSreceiver} + t_{decoder}$$

$$t_{clk1} = t_{LVDStransmitter} + t_{wire} + t_{LVDSreceiver}$$

The main difference between these two transmission time comes from $t_{FlipFlop}$ and $t_{decoder}$. It can be represented in Figure 5.17. t is the combination of $t_{FlipFlop}$ and $t_{decoder}$. The rising edge of the next clock cycle is always t ahead of the end of a signal cycle, which provides reliable synchronization.

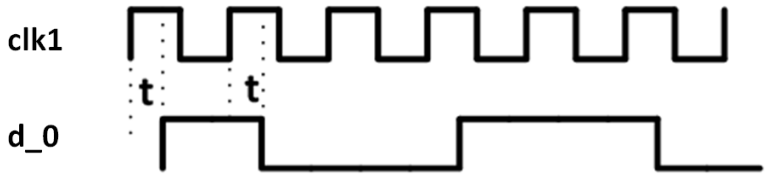

Figure 5.17: Inputs of FlipFlop

5.3.4 Delay Cell

In Figure 5.16, $CLK1$ is used to sample data and $COMN_1$ is acquired. Then, $CLK1$ and $COMN_1$ will be sent into the data-rate doubling circuit to increase the data rate. In terms of the processing time of a FlipFlop, a certain delay should be applied to compensate for the delay between $CLK1$ and $COMN_1$.

The delay also helps ensure that, the clock can 'hold' the data in half a clock period. A new timing diagram with delayed clocks is presented in Figure 5.18.

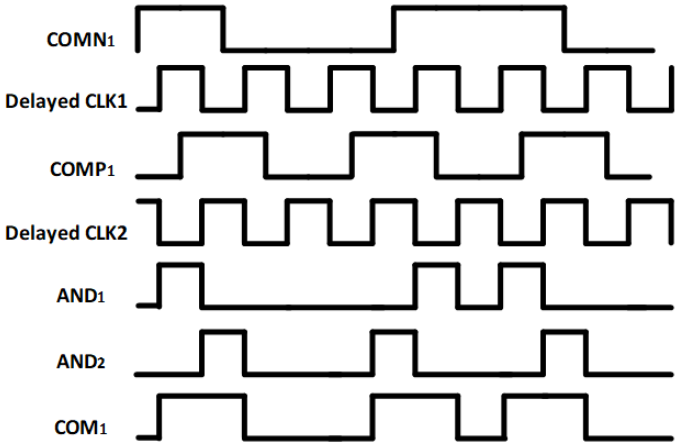

Figure 5.18: Timing diagram of clocks with delay

The appropriate delay time is relevant to one data period t. If the delay time is longer than $\frac{1}{2}t$, as shown in Figure 5.19, part of signals are missing or some glitches appear. Also, delay time should longer than the processing time of FlipFlop. The processing time is around 200 ps in simulation.

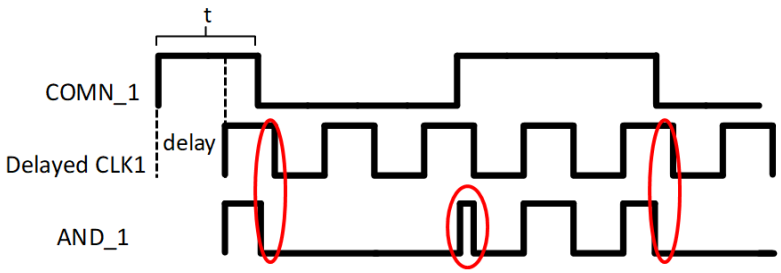

Figure 5.19: Timing diagram of a clock with delay over $\frac{1}{2}t$

To generate a symbol rate of 600 MHz from 300Mb/s data, t is around 3.3 ns. Thus, delay time should be between 200 ps and 1.6 ns. Taking process variations and wire length during layout into consideration, 800 ps can be a good choice because it leaves some margins in case the signal is a bit faster or slower. 800 ps delay can be provided with standard digital delay cells (DEL0BWP7T and DEL1BWP7T). The simulated result is shown in Figure 5.20 and it can generate a delay around 800 ns.

5.4 LAYOUT

Figure 5.21 shows the layout diagram of this load-modulation data link with several sub-blocks, including the load-modulation circuit and the data-rate

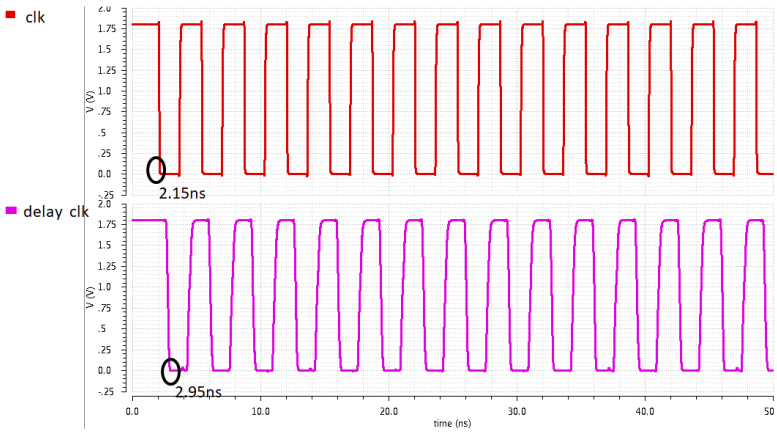

Figure 5.20: Clock without a delay cell and clock with a delay cell

doubling circuit. The digital processing part includes a 3-7 decoder and FlipFlop. Considering these blocks only, it requires 0.02 mm^2 die area. This chip is implemented with TSMC 180 nm technology.

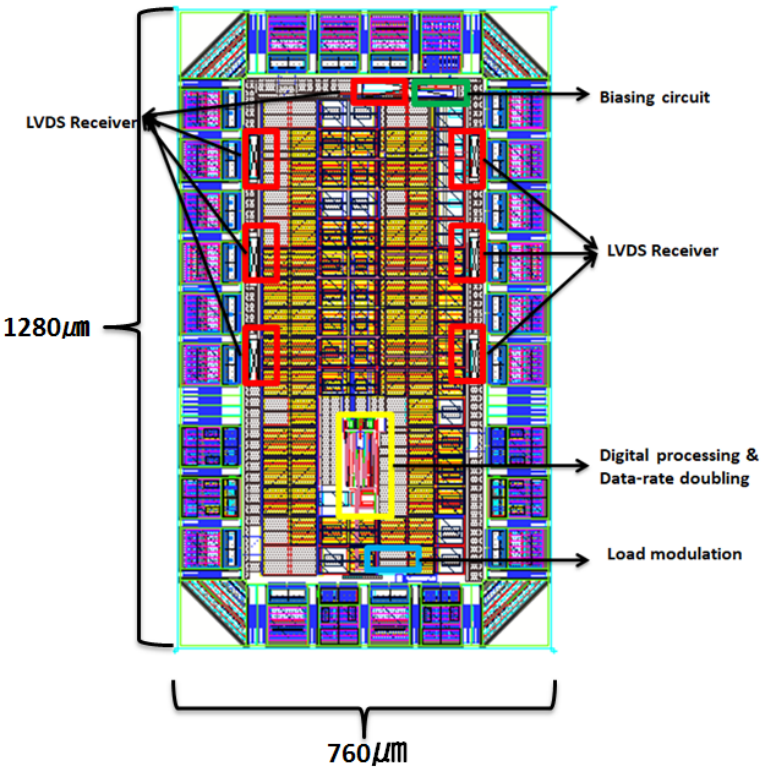

Figure 5.21: Layout diagram

LVDS receivers are placed close to the pads to generate digital signals. Compared with analog signals, digital signals are more robust against noise. Also, load-modulation circuit is placed close to the pad as well to reduce the influence of on-chip noise on the multi-level signalling.

In this test ASIC, several signals are sent to the inputs of one component

for processing. If there is any obvious delay between these input signals, glitches might be generated at the output or the chip might fail. Thus the delay between each input signal should be minimized. In the layout process, keeping the wire lengths of each signal same is helpful in the reduction of delay.

Also, to transmit signals or power, this chip requires 26 pads. The arrangement of this pads is presented in Figure 5.22. To accommodate 26 pads, the die area is much larger than 0.02 mm^2. The functions of each pads are described in Table 5.5.

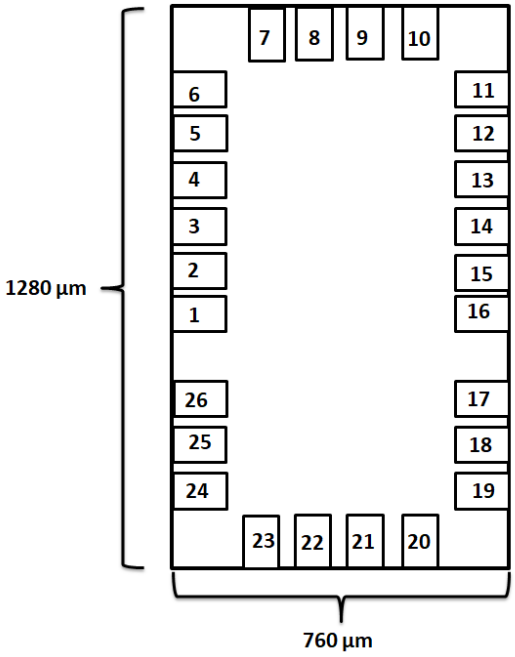

Figure 5.22: Pad ring arrangement

Table 5.5: Descriptions of pads

No. of pads	Description	Required signal level (V)
1-6, 11-16	Random data	0,0.35
8,9	Clock	0,0.35
7 23	Analog supply	1.8
10, 20, 22	Analog ground	0
17, 26	Digital ground	0
18, 25	Pad supply	1.8
19, 24	Digital supply	1.8
21	Output	

Especially, two analog ground pads are placed near Pad_{21} to avoid the parasitic inductance between the analog output and digital ground.

6 RESULTS AND CONCLUSIONS

This chapter will present simulation results of the completed circuit including extracted parasitics from layout first. It verifies multi-bit per symbol signalling and explores the relationship between the BER number and the transmission conditions (bits per symbol and symbol rates). In the end, conclusions and future work will be presented.

6.1 POST-LAYOUT SIMULATION

In this section, multi-bit per symbol signalling is applied to generate a data rate of 600 Mb/s first. With a fixed bit per symbol, its symbol rate will be adjusted to further increase the data rate. The quality of data is judged by its BER number.

6.1.1 3-bit per symbol signalling

To generate 3-bit per symbol signalling, two groups of random numbers are generated by PRNGs and sampled at the rising edge and falling edge respectively on an FPGA. In simulation, this is simulated by Verilog A code. Each group consists of 3-bits and they are generated according to two overlapping clocks, as shown in Figure 6.1. Table 6.1 presents the 3-bit input codes and their corresponding expected voltage levels.

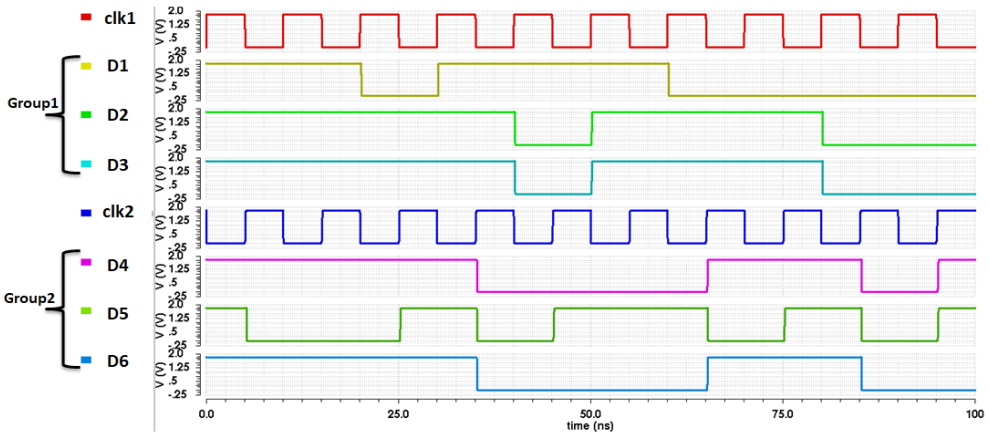

Figure 6.1: Random number generation

The post-layout simulation can be compared with pre-layout for rough judgement first. Their output waveforms are presented in Figure 6.2 and they share a similar waveform. Due to the in-chip interconnection, the waveform from the post-layout simulation is a bit slower. Also, each signal value can be compared with the expected values in Table 6.1 for decoding. When these decoded data are compared with the simulated code sequence shown in Figure 6.1, it shows as expected that this data link transmits data in two groups properly.

Table 6.1: Input code and their corresponding voltage values for 3-bit per symbol signalling

Input Code	Expected voltage value (mV)
111	137
011	186
101	236
001	286
110	336
010	388
100	430
000	483

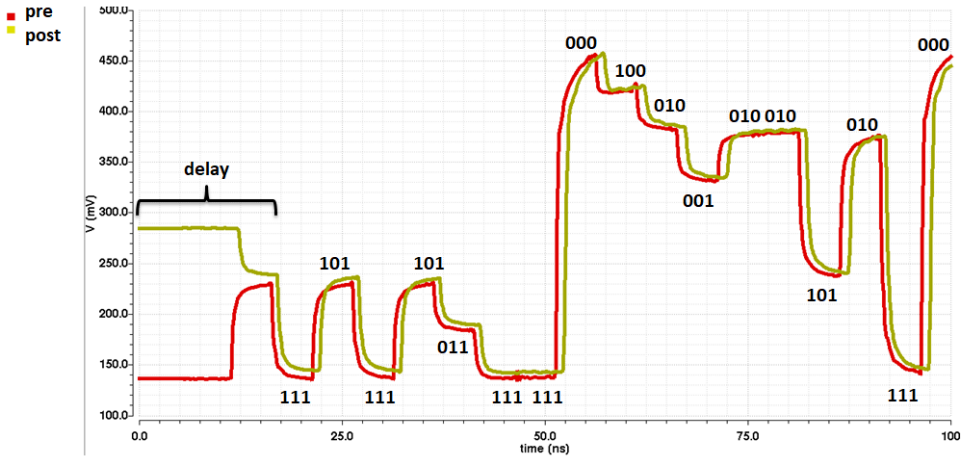

Figure 6.2: Comparison between pre-layout and post-layout simulation at the symbol rate of 200 MHz

To further explore the transmission accuracy, an eye diagram is extracted in Figure 6.3. The voltage levels in the middle of each interval are chosen as threshold voltages.

With a Verilog A model, this output waveform can be decoded automatically, which can be compared with input data later to compare its BER number. With enough simulation time to generate over 10000 samples, the BER is 0 when the symbol rate is 200 MHz. However, the noise performance is not considered in this simulation.

At this time, the total power consumption on chip is around 7 mW. Load-modulation circuit consumes 1.7 mW. Analog blocks (LVDS receivers and the biasing circuit) consume 4.78 mW while digital blocks (decoders, FlipFlops, date-rate doubling circuits and gate drivers) consume 0.52 mW.

With an increased symbol rate, the intervals between two adjacent levels become smaller due to inter-symbol interference. Table 6.2 shows the relationship between symbol rate and its corresponding BER number. When the symbol rate is no higher than 333 MHz, the corresponding BER number remains acceptable for ultrasound applications.

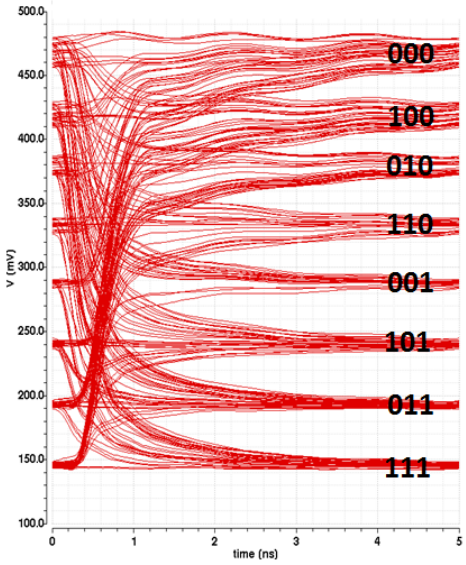

Figure 6.3: Eye diagram of 3-bit signalling at the symbol rate of 200 MHz

Table 6.2: BER at several symbol rates for 3-bit per symbol signalling

Symbol rate (MHz)	Data rate (Gb/s)	BER
100	0.3	0
150	0.45	0
200	0.6	0
250	0.75	0
300	0.9	0
333	0.99	0.0015
356	1.07	0.0107

Table 6.3 shows the simulated power consumption of the load-modulation circuit, analog blocks, digital blocks and the chip respectively. It shows that the change in chip power consumption mainly comes from the digital blocks. With an increase in working frequency, digital blocks consume more power.

Table 6.3: Power consumption distribution at several symbol rates for 3-bit per symbol signalling

Symbol rate (MHz)	Data rate (Mb/s)	Load modulation (mW)	Digital blocks (mW)	Analog blocks (mW)	Total (mW)
100	300	1.727	0.269	4.71	6.789
150	450	1.736	0.395	4.74	6.871
200	600	1.701	0.52	4.71	6.931
250	750	1.728	0.655	4.77	7.153
300	900	1.698	0.81	4.834	7.338
333	1000	1.698	0.889	4.874	7.461
356	1068	1.699	0.938	4.85	7.487

6.1.2 2-bit per symbol signalling

To allow 2-bit per symbol transmission, each 3-bit data group consists of one fixed number and two random numbers. An example is presented in Table 6.6. The last bit in each code is fixed to '1'. The interval between two adjacent levels is around 50 mV.

Table 6.4: Input code and their corresponding voltage values for 2-bit per symbol signalling

Input Code	Expected voltage value (mV)
11(1)	137
01(1)	186
10(1)	236
00(1)	286

The symbol rate is set as 300 MHz first to achieve a data rate of 600 MHz. The corresponding eye diagram can be derived in Figure 6.4. All the intervals are larger than 35 mV and it brings convenience to decode data. With enough simulation time, its corresponding BER is 0 as well.

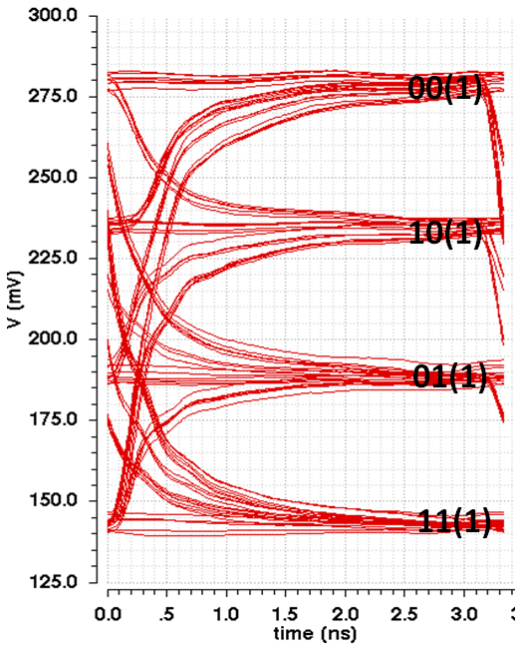

Figure 6.4: Eye diagram of 2-bit signalling at the symbol rate of 300 MHz with a 50 mV interval

At this time, the total chip power consumption is around 6.824 mW. The load-modulation circuit consumes 1.375 mW. The analog blocks consume 4.779 mW while the digital cells consume 0.670 mW. Compared with 3-bit per symbol signalling, 2-bit per symbol signalling consumes less power to achieve the same data rate of 600 MHz. Although digital cells consumes more power at a higher working frequency, the load-modulation data link

consumes more power for three bits per symbol transmission.

This structure applies to a higher symbol rate as well. The corresponding BER number remains 0 when the symbol rate increases to 800 MHz and generate a 1.6 Gb/s data rate. Figure 6.5 represents its eye diagram and the smallest interval can reach 13 mV. It provides some noise margin.

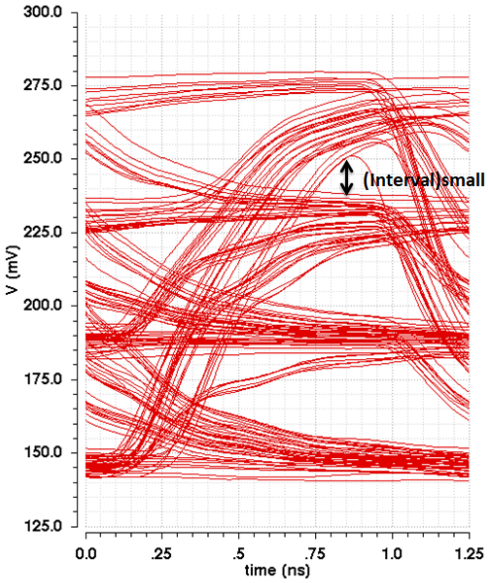

Figure 6.5: Eye diagram of 2-bit signalling at the symbol rate of 800 MHz with a 50 mV interval

Table 6.6 presents the distribution of power consumption at several symbol rates. It shows that, with the increase of a symbol rate, digital cells consume more power and it leads to the change of the total chip power consumption.

Table 6.5: Power consumption distribution at several symbol rates for 2-bit per symbol signalling

Symbol rate (MHz)	Data rate (Mb/s)	Load modulation (mW)	Digital blocks (mW)	Analog blocks (mW)	Total (mW)
150	300	1.345	0.298	4.716	6.358
225	450	1.342	0.514	4.787	6.643
300	600	1.375	0.670	4.779	6.824
375	750	1.341	0.802	4.7	6.843
400	800	1.369	0.8456	4.8	7.014
450	900	1.345	0.971	4.849	7.165
500	1000	1.336	1.062	4.954	7.352
600	1200	1.407	1.246	5.01	7.663
800	1600	1.389	1.636	5.036	8.061

With this test ASIC, another type of 2-bit per symbol transmission with an interval of 100 mV can be acquired. Its eye diagrams at the 300 MHz and 800 MHz is presented in Figure 6.6. When the symbol rate is increased, inter-symbol interference is more worse and it leads to the reduction of an actual interval. Compared with Figure 6.4 when the symbol rate is both 300 MHz, it can be found that, with an expected interval of 100 mV, its average varia-

tion for each level is around 12 mV. When the interval is reduced to 50 mV, the average variations reduce to 8 mV. However, due to the lager expected interval, the condition of 100 mV provides more margins for noise. At this time, it consumes 7.218 mW, which is larger than that of an 50 mV situation.

When the symbol rate is further increased to 800 mV, the 100 mV interval transmission suffers more from inter-symbol inference and it performs worse compared to the 50 mV situation.

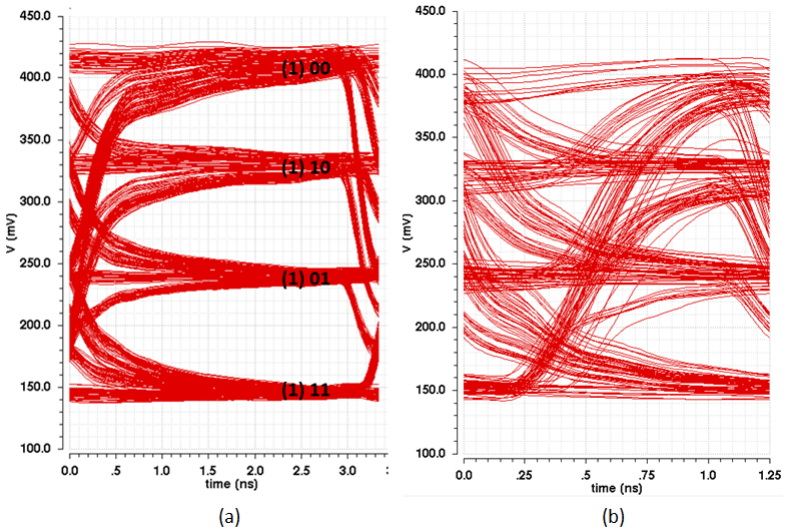

Figure 6.6: Eye diagram of 2-bit signalling at the symbol rate of (a) 300 MHz and (b) 800 MHz with an 100 mV interval

Table 6.6 summarizes the total power consumption $P4$ for conditions of different intervals at a certain data rate. It shows to achieve a same data rate, an larger interval consumes more power.

Table 6.6: Power consumption at several symbol rates with different intervals

Data rate (Gb/s)	With an 100 mV interval (mW)	With a 50 mV interval (mW)
0.3	6.588	6.358
0.45	6.927	6.643
0.6	7.227	6.824
0.75	7.339	6.843
0.8	7.514	7.014
0.9	7.704	7.165
1	7.828	7.352
1.2	8.232	7.663
1.6	8.7	8.061

Thus, it can be concluded that, for 2-bit transmission, a higher interval consumes more power, but at a lower symbol rate, its large interval allow for some inter-symbol interference. It provides larger noise margin. However, when the symbol rate is further increased, the influence of inter-symbol inter-

ference on a larger interval situation cannot be ignored and 2-bit signalling with a smaller interval can perform better.

6.1.3 1-bit per symbol signalling

In each group of three-bit numbers, when only the first data is random and the others are fixed as '0' and '1', it allows for 1-bit per symbol signalling. One example is shown in Table 6.7. 50 mV is the expected voltage interval as well.

Table 6.7: Input data and their corresponding voltage values for 1-bit per symbol signalling

Input Code	Expected voltage value (mV)
1(01)	236
0(01)	286

To generate a data rate of 600 Mb/s, this signalling requires a symbol rate of 600 MHz. The eye diagram can be derived in Figure 6.7. Although the signal levels are reduced, the actual interval does not improve a lot due to the increased symbol rate. At a higher frequency, the signal suffers more from attenuation. Within enough simulation, the signals can always be decoded correctly and the BER is 0.

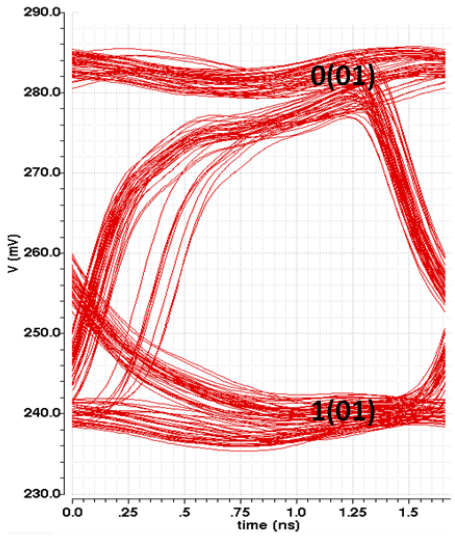

Figure 6.7: Eye diagram of 1-bit signalling at the symbol rate of 600 MHz

At this time, the total power consumption on chip is about 7.717 mW, which is lager than multi-bit per symbol transmission at the data rate of 600 Mb/s. The load-modulation circuit consumes 1.796 mW and analog cells consume 4.955 mW. With a high working frequency, digital cells consume 0.966mW. When the symbol rate increases to 800 MHz, the data rate changes simultaneously to 800 Mb/s. The number number remain 0.

The distribution of power consumption is listed in Table 6.8. The increase in power consumption with the data rate mainly comes from the digital cells.

Table 6.8: Power consumption distribution at several data rates for one-bit per symbol signalling

Symbol rate (MHz)	Data rate (Mb/s)	Load modulation (mW)	Digital blocks (mW)	Analog blocks (mW)	Total (mW)
300	300	1.797	0.5	4.752	7.049
450	450	1.801	0.71	4.817	7.336
600	600	1.796	0.966	4.955	7.717
750	750	1.784	1.21	5.03	8.024
800	800	1.785	1.256	4.969	8.01

6.1.4 Return-to-zero Transmission

The test ASIC allows for RTZ transmission as well when three data in one group are fixed. The maximum bits per symbol is two. One example of 2-bit NRZ transmission is presented in Figure 6.8.

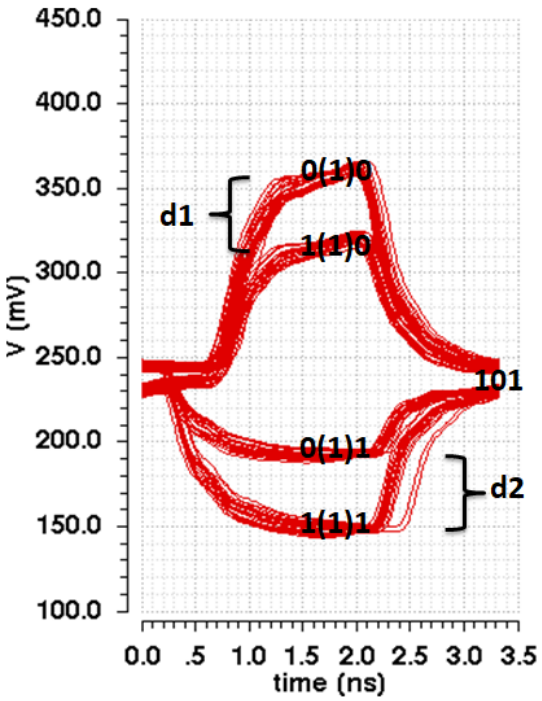

Figure 6.8: One example eye diagram of 2-bit RTZ transmission at the symbol rate of 600 MHz

The return-to-zero stage is generated by signal level '101'. Due to setup, this stage cannot be actually placed in the middle and this brings asymmetry. This partly contributes to the difference of $d1$ and $d2$ in Figure 6.8. The

ideal interval is around 50 mV.

Due to the existence of RTZ, the actual symbol rate is only 300 MHz and it allows a data rate of 600 MHz. Figure 6.9 illustrates the eye diagrams of 2-bit per symbol NRZ transmission at the symbol rate of 300MHz and 600 MHz respectively. It shows at the symbol rate of 300 MHz, the actual interval is around 40 mV, which is similar to that in Figure 6.8. At this time, their data rate are same. For NRZ transmission, when the symbol rate is increased to 600 MHz, the period of each signal is around 1.66 ns, which is almost equal to the useful signal period in Figure 6.8. With the increased symbol rate, inter-symbol interference is more severe and the actual interval is reduced to 33 mV. Although the interval is smaller, it is suitable for decoding and it has a faster data rate.

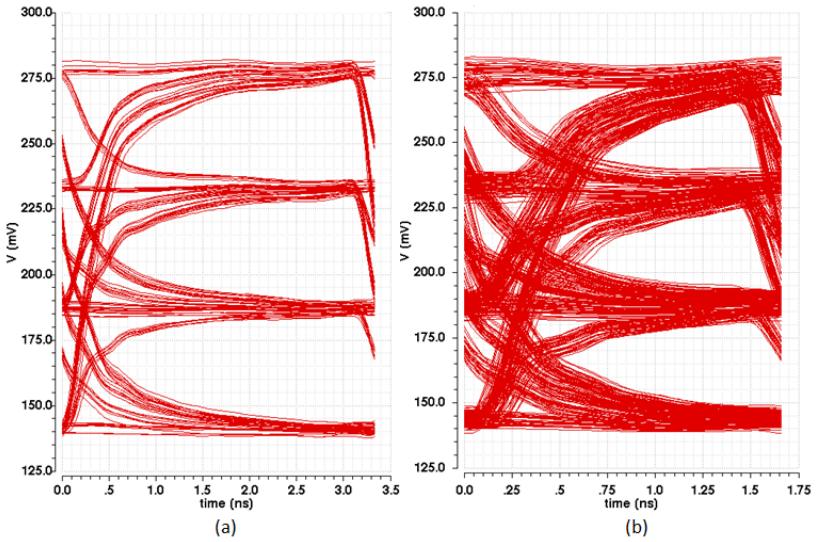

Figure 6.9: Eye diagram of 2-bit NRZ transmission at the symbol rate of (a) 300 MHz and (b) 600 MHz

In terms of its power consumption,it requires 7.932 mW to generate a useful data rate of 600 Mb/s. It is larger than NRZ transmission.

Thus, although return-to-zero transmission helps reduce the effect of inter-symbol interference, it is at the sacrifice of power and transmission speed.

6.2 CONCLUSION

This thesis describes the design of a load-modulation data link. It aims to further increase the data rate, thus making ultrasound imaging more real-time. To achieve this, several works have been done.

First, modeling of AWG 42 cable is compared among a RLCG model and an S parameter model. Compared with a RLCG model, the S parameter

model can predict the cable transmission better. Frequency-dependant attenuation and the resulting inter-symbol interference simulated using this model are in better agreement with measurements.

Also, a versatile load-modulation data link has been proposed. It allows for investigation of different transmission conditions such us symbol rates and bits per symbol. Attention should be paid to inter-symbol interference in the process of designing the load-modulation circuit. More voltage levels lead to worse inter-symbol interference and it can be compensated at the expense of more power consumption.

Based on post-layout simulation results, this data link can achieve a data rate of 1.6 Gb/s when 2-bit per symbol signalling is applied. In terms of power consumption and data speed in Table 6.9, 2-bit per symbol signalling performs better.

Table 6.9: Power consumption at different data rates for different bits per symbol

Data rate (Gb/s)	1-bit (mW)	2-bit (mW)	3-bit (mW)
0.3	7.02	6.358	6.789
0.45	7.328	6.643	6.871
0.6	7.717	6.824	6.931
0.75	8.024	6.843	7.153
0.9		7.165	7.338
1		7.352	7.461

In the end, this test chip has been taped-out and is currently being fabricated for experimental verification.

6.3 FUTURE WORK

Potential futher improvements of this load-modulation data link can be be summarized as follows.

The load-modulation circuit should be optimized to obtain equally-spaced voltage levels, so as to minimize the noise margin. In this work, the intervals are not exactly same and it limits the further increase of data rate for 3-bit per symbol signalling.

Second, the speed of input data should be further increased. In this work, random numbers are generated according to the FPGA clock and the symbol rate is doubled on chip. Limited by the available FPGA clock, it is hard to further investigate the potential of 2-bit per symbol signalling at a symbol rate higher than the maximum of 600 MHz.

Third, the data-rate doubling circuit can be further improved. For now, the period of each signal is not exactly same and smaller signal period leads to

more attenuation and it might lead to decoding difficulty.

Also, measurements will be done after the chip is back. It helps verify the experimental setup and investigate the transmission capacity of different cables when some non-idealities like noise are included.

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