Nano Optomechanical Read-out for Microcantilever Sensors

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CONFIDENTIAL

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Faculty of EEMCS

Nano Optomechanical Read-out for Microcantilever Sensors

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For the degree of Master of Science in Microelectronics at Delft University of Technology

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Abstract

This thesis demonstrates a novel displacement sensor with photonic structure a micro ring resonator with a micro cantilever. This device uses the working principle of micro ring resonator and transfer the mechanical signal into optical signal. The goal of this project is to design, fabricate and measure such a device. Fabrication process is not so complex, but as processing at chip level introduces additional complexity as not all machines can handle small pieces, several problems needed to be settled and most time was spent on fabrication, this is discussed in detail. This new design should have a same sensitivity as the micro ring resonator.

Keywords: micro ring resonator, micro cantilever, fabrication.

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Chapter 1 Introduction

1.1. Motivation

Cantilever –like micro/nanomechanical sensors are very promising candidates for sensing physical, chemical and biological matters. These sensors have many advantages over the conventional sensors in terms of high sensitivity, low cost, simple procedure and so on [1]. In this thesis, I will introduce a novel displacement sensor based on a silicon cantilever

There are many methods to measure displacement like laser displacement sensor and capacitive displacement sensor, and this thesis will introduce a novel displacement sensor based on a cantilever. Cantilever –like or micro/nanomechanical sensors are very promising for sensing and are also widely used in scanning probe microscopy. A good example is the atom force microscopy (AFM) [2]. In this thesis, I introduce a micro ring resonator based on a micro cantilever as a displacement sensor. This sensor has many advantages over others. First, as an AFM it does not need any alignment when scanning the surface. Second, integrated sensors are suitable for cantilever arrays due to their compactness, simplicity and potential for mass production [2].Third, since this kind of sensor is based on a structure without any electrical circuit only waveguides made of silicon can be used in harsh environments such as ultra-high vacuum (UHV) systems and in the presence of electromagnetic interference. Moreover, these cantilever sensors can be cheap, portable, ultra-sensitive and easily used as multi-array sensors. That is why researchers show their interest in this new field.

1.2. MRR as displacement sensor

Micro ring resonators are compact wavelength selective devices [3]. Figure 1-1 is a picture of this device. There is a closed loop coupled to light at the input and output.

The ring has a variety of geometries, such as folded ring, race-track ring or just circle ring, as shown Figure 1-2.

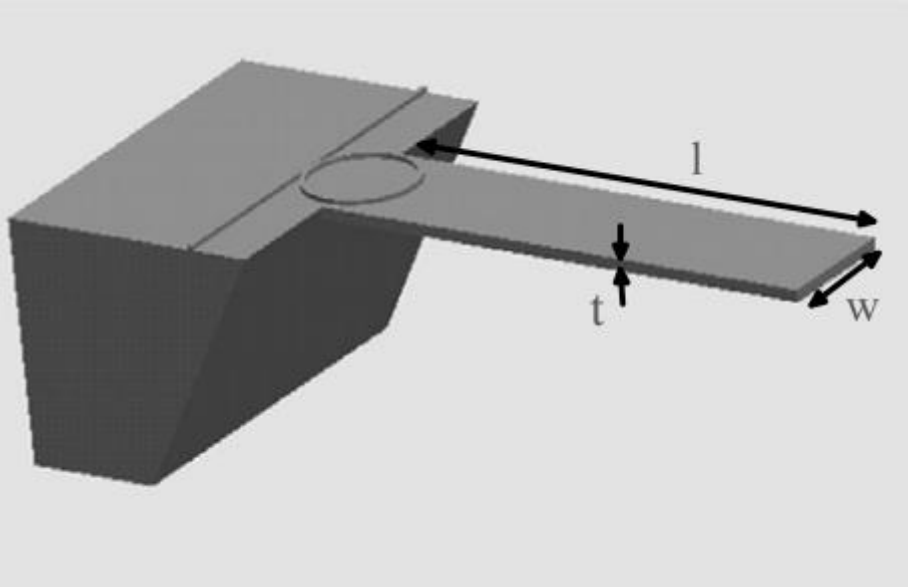

Figure 1-1 A picture of a MRR device[2].

In this sensor refractive index changes are related to the deflection of the beam. From the output port via analysis of the data, it is possible to know how much displacement happens to the beam. Figure 1-3 depicts this operation principle. Light at a certain wavelength is injected into the straight waveguide. As the gap between the straight waveguide and the ring resonator is very narrow, 200 nm, this makes the light couple into the ring resonator. When the cantilever bends, stress due to deflection of the beam changes the refractive index on the ring resonator due to the photo-elastic effect and thus leading to modification in the transmission characteristics of the optical waveguide. Then by detecting and analyzing the intensity modulation through the waveguide, it is possible to measure the cantilever displacement with high accuracy [2].

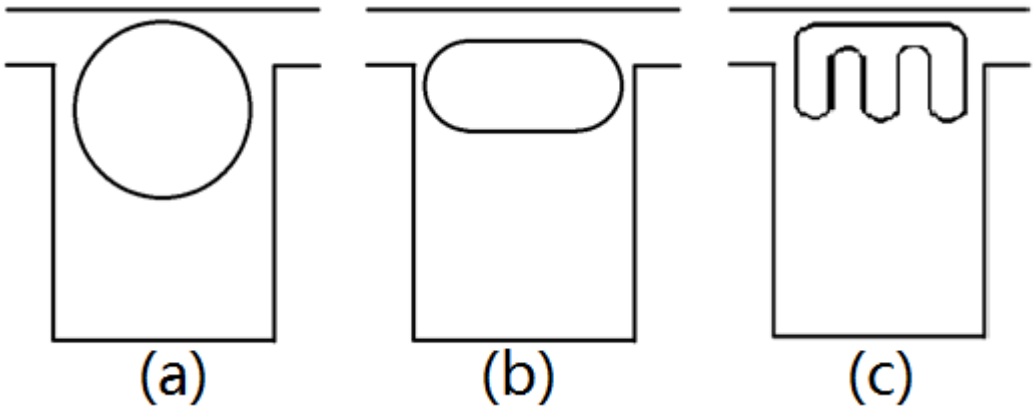

Figure 1-2 Three different geometries of the ring resonator :(a) circle ;(b) race-rack ring resonator ;(c) folded ring resonator.

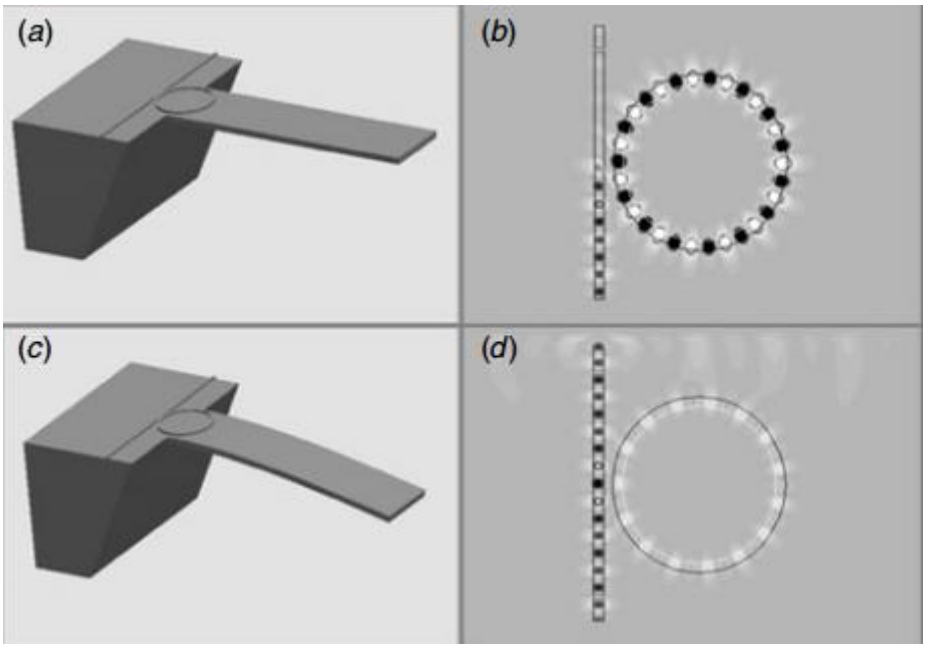

Figure 1-3 A schematic illustration of the operational principle for this device: (a), (c) the cantilever for unbent and bent conditions; (b), (d) the field distribution on the ring resonator on the cantilever.[2]

1.3. The goal of the project

The goal of this project is to study, design and fabricate a micro/nano-mechanical cantilever integrated with nano-photonics, as a read-out technique for translating the mechanical motion of the nanomechanical sensor. Because this sensor is based on MRR, the requirements for the device are the same as for the MRR. Thus, aim at

an optical sensitivity is larger than $\frac{d\lambda}{d\varepsilon}=0.478\frac{pm}{\mu\varepsilon}$ (this will be show in chapter 2).

1.4. Outline of the thesis

As the title suggests, this thesis I introduces a novel displacement sensor by using MRR based on a micro cantilever.

Chapter 2 describes the mechanical theories involved and also presents the working principle of the MRR. This chapter will also show the design process of the cantilever. Moreover, calculations for the most suitable cantilever length, thickness and targeted displacement sensitivity are shown.

Chapter 3 introduces the layout of the MRR chip and the materials used in this chip. Because this project requires etching a cantilever on the MRR chip, so a deep understanding of the layout and the thickness of each layer is necessary.

In chapter 4, the basic process modules that are used in the fabrication of the device are illustrated. Then detailed process flow charts will be presented, and some issues related to the fabrication are discussed.

Chapter 5 describes the testing of the device after fabrication. In this chapter, the measurement set up and procedure is shown together with discussion on the reported results.

Finally chapter 6 presents the conclusion of the thesis and gives recommendation for future reseach.

Reference

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[2] Kiyat I, Kocabas C, Aydinli A. Integrated micro ring resonator displacement sensor for scanning probe microscopies[J]. Journal of Micromechanics and Microengineering, 2004, 14(3): 374.MLA

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Chapter 2 The cantilever based MRR

2.1 The working principle

In this project, a micro ring resonator (MRR) integrated on a cantilever is designed to measure the deflection of the cantilever (see Figure 1-1). When the cantilever bends, there is a stress on the surface and this stress increases linearly along the cantilever, which means the maximum stress happens at the supporting point of the cantilever. Consequently, for the micro ring resonator to get the highest sensitivity, it is better to integrate it at the base of the cantilever. An optical waveguide is coupled to the MRR. When the optical signal goes through the waveguide it will couple to the MRR. When the cantilever is under bending condition, the optical signal coupled to the MRR will change, which means that the wavelength of the optical signal has changed due to the refractive index change [1]. The displacement can be calculated through the detectable wavelength shift at the output.

2.2 Relevant mechanical theory

A cantilever is a beam with one end fixed as illustrated in Figure 2-1. When there is a transverse loading applied on the cantilever, this induces bending. Bending is an important form of stressing a structure. The cantilever is stretched on one side and compressed on the other, as illustrated in Figure 2-1 [2].

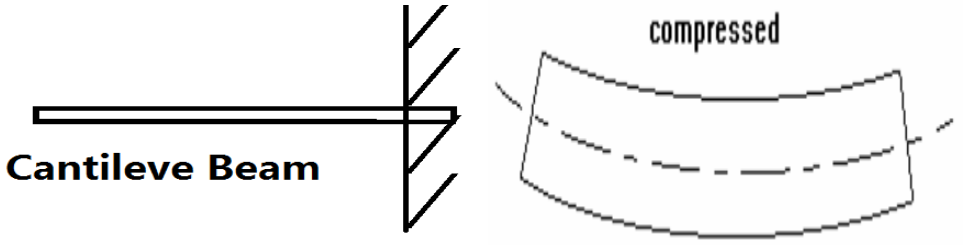

Figure 2-1 Cross section of the cantilever and the stretching under bending condition

There are some parameters related to bending condition: *M* denotes bending moment, I is moment of inertia, σ represents stress at a certain position, ε is the stain due to bending moment, *d* the distance between the surface of cantilever and

the neutral axis and *y* is a certain position along the cantilever beam. The bending moment is a reaction induced in a structural element when an external force or moment is applied to the element causing the element to bend [3][4]. The moment of force, *M* is defined as:

$$M = F \cdot z \tag{2-1}$$

Where M is the vector of bending moment and z is the position vector from the reference point to where the force (*F*) is applied. I is also called the second moment of area. This is a geometrical property of an area which reflects how its points are distributed with respect to an arbitrary axis. For standard shapes the second moment of area can be deduced.

For this project the micro mechanical cantilever is consider as a solid rectangle. The formula deduced for a solid rectangle is shown below:

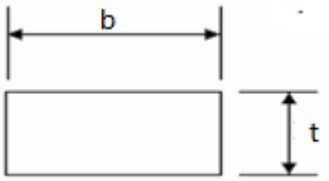

Figure 2-2.The cross section of a beam

$$I = \frac{b \times t^3}{12} \tag{2-2}$$

In this formula, b is the width of the beam and t is the thickness of the beam. Strain can be expressed as: $\varepsilon = \text{change in length/ original length}$, which can be defined as:

$$\varepsilon = \frac{\Delta l}{l} \tag{2-3}$$

Another important concept is the neutral axis. This is an axis along the length of the cantilever which keeps unstressed, neither compressed nor goes into tension. Usually, this axis passed through the centroid of the cross section area. If the beam consists of not only one single material, but two or more materials, this neutral axis will change. How to determine the position of this axis will be introduced in next section. The most important relationship between these parameters is:

$$\frac{M}{I} = \frac{\sigma}{d} \tag{2-4}$$

This will be used for detail simulation in section 2.3.

The last but very important formula that will be used to calculate the dimension of the beam is the Euler-Bernoulli beam theory. The Euler-Bernoulli equation can be written as:

$$EIy`` = EI\frac{d^2y}{dz^2} = M = F \cdot z \tag{2-5}$$

This formula shows the relationship between the deflection of the cantilever and the applied force to the beam. This will be an important element to design the cantilever and in the next section the detailed design will be presented.

2.3 Feasibility calculations

Figure 2-3 shows the operating principle of this displacement sensor. This chart depicts the relationships of displacement, stress, index and other parameters relevant to this sensor. So displacement can be calculated by detecting the wavelength shift, which is also called transmission shift. To understand this more clearly, some mechanical analysis will be introduced, following the scheme depicted in Figure 2-3.

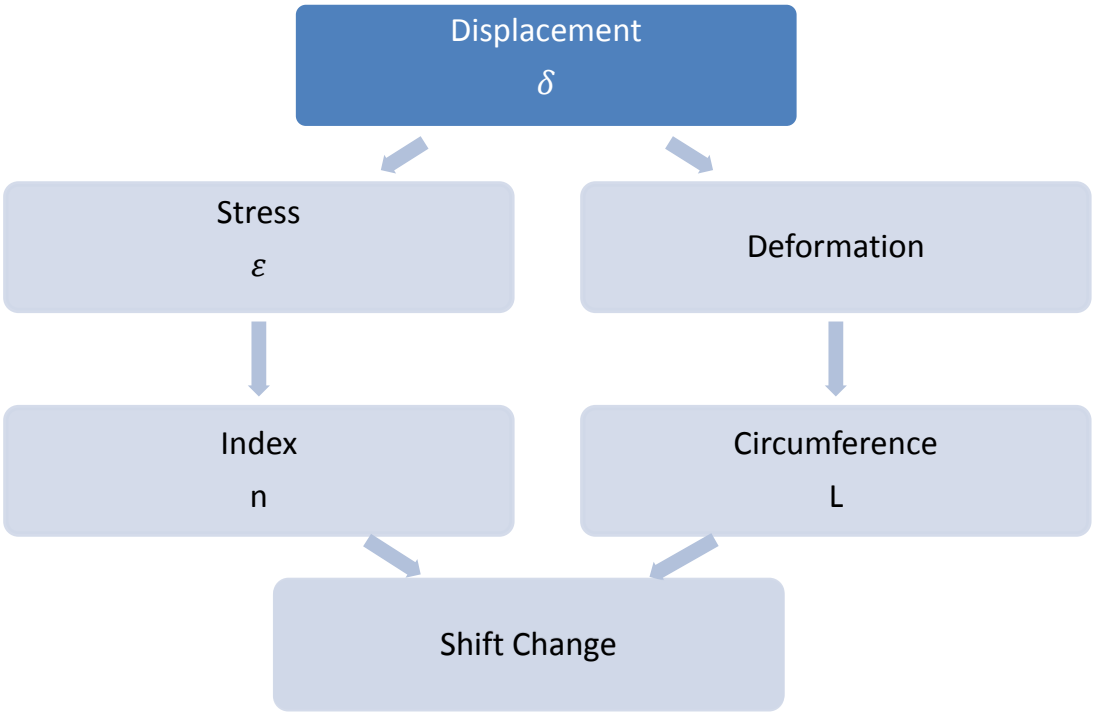

Figure 2-3 Working principle of MRR

The cantilever is a beam fixed at only one end as shown in Figure 2-1. In order to calculate the stress and strain in the cantilever, Euler-Bernoulli beam theory is used. For a beam with beam length direction as z, deflection direction as y:

$$EIy`` = EI\frac{d^2y}{dz^2} = M = F \cdot z$$

Where *E* is elastic modulus for this equation (Young 's modulus),

I is the second moment of area also known as moment of inertia,

M is bending moment,

F is the force applied to the cantilever at the position z.

So deflection can be integrated as:

$$y = \frac{F \times (L - z)^2}{6EI} \times (2L + z) \tag{2-6}$$

The definition for I is:

$$I = \frac{b \times t^3}{12}$$

Consider the expression for I (equation (2-2)), and for *z*=0, we derive the following expression for *F:*

$$F = \frac{3EIy}{L^3} = \frac{yEbt^3}{4L^3} \tag{2-7}$$

Thus the moment in the beam becomes:

$$M = F \times z = \frac{yzEbt^3}{4L^3} \tag{2-8}$$

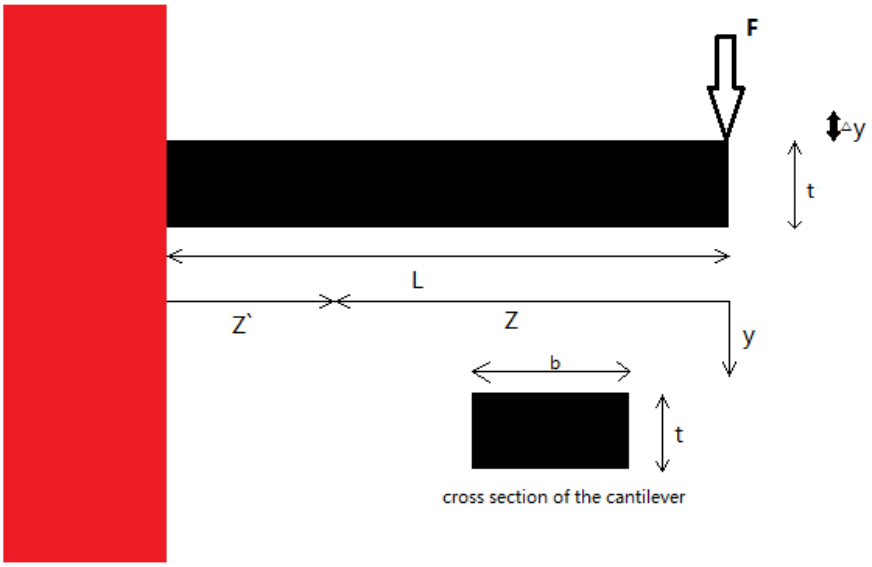

Figure 2-4 Cross section of the cantilever for calculate

Combining equation (2-4) and equation (2-10) the stress then can be expressed as:

$$\sigma = \frac{M \cdot d}{I} \tag{2-9}$$

Young's modulus is a measure of the stiffness of an elastic material using Hooke's law and it is a material property. It can described as

$$E = \frac{stress}{strain} = \frac{\sigma}{\varepsilon} \tag{2-10}$$

Combining (2-9) and (2-10), when *z*=L which means the stress at the base of the cantilever is then:

$$\sigma_{base} = \frac{z}{I} d \cdot \frac{3EIy}{L^3} = \frac{3Edy}{L^3} \cdot z = \frac{3Edy}{L^2} \tag{2-11}$$

An important issue that should be taken into account is the fracture strength, also known as breaking strength. Because when the cantilever is bending whether this

beam is functional or not depends on its completeness. The unit of this parameter is MPa, so it is related to the stress. Moreover, higher numbers mean this material is more robust, in other words, it is not easy to break. In our case the cantilever is made of two materials: silicon and silicon dioxide. The value of fracture strength for silicon is 7000MPa and that of silicon dioxide is 364MPa. Therefore, it is important to guarantee the maximum stress in the beam is smaller than the fracture strength of silicon dioxide, while from equation (2-11) the stress is linear along the beam when a given deflection y happens. To make sure when the cantilever bends and no break happens to this device, the following should yield:

$$\sigma \cdot n \leq 364MPa \tag{2-12}$$

Where *n* is a safety factor, always bigger than 2. Here for safety design, we assume *n*=4.

$$\frac{3Edy}{L^2} \cdot n \leq F_s \tag{2-13}$$

F_s denotes fracture strength for silicon dioxide. Thus, from this relationship, it is obvious to get a restrictive condition for the length of the beam:

$$L \leq \sqrt{\frac{3Edy}{F_s} \cdot n} \tag{2-14}$$

For a single material $d = \frac{t}{2}$, t is the thickness of the cantilever. In our case the beam consists of two layers: a top layer, device layer, made of silicon and a buried silicon dioxide layer below the device layer. In this case, the *d* does not equals to $\frac{t}{2}$. To calculate *d*, here comes the concept of neutral axis.

The neutral axis is an axis or shaft in the beam with no longitudinal stresses or strain. When bending the beam, the neutral axis passes through the centroid. The stress varies from top to bottom over the structure. One edge is at the maximum tensile, and the other edge has the maximum compressive, as depicts in Figure 2-5:

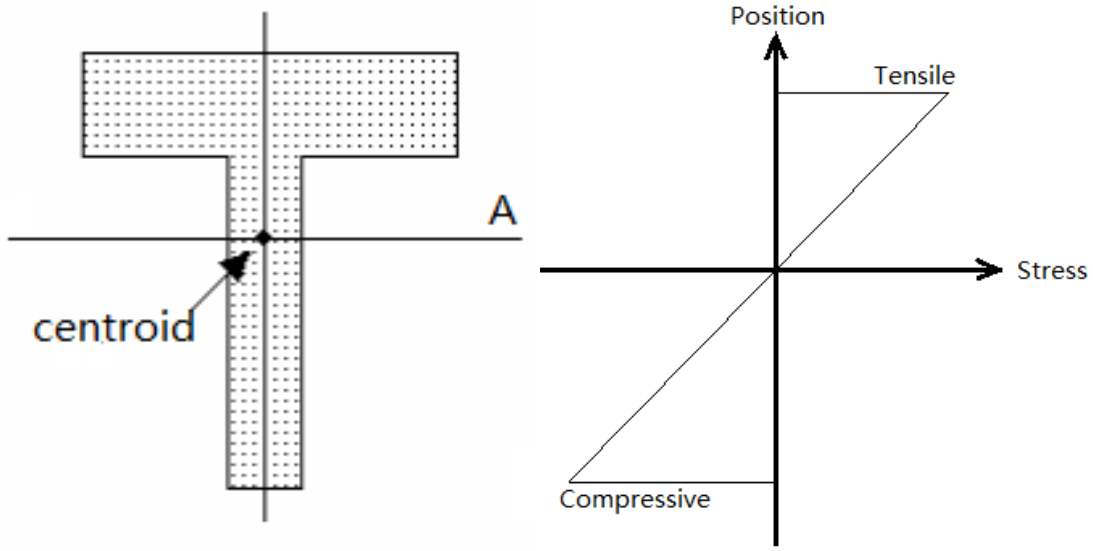

Figure 2-5 stress distribution in a beam

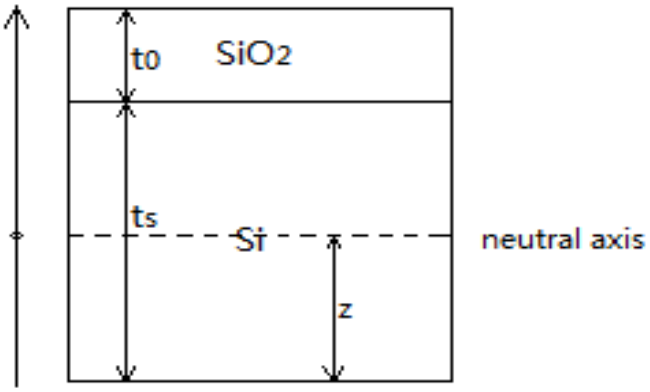

Figure 2-6 The cross section of the beam

Assuming that t_0 is the thickness of silicon dioxide, t_s is the thickness of silicon and z is the distance between the edge of silicon and the neutral axis, then:

$$\int_{-z}^{t_s-z} E_{Si} y dy + \int_{t_s-z}^{t_s+t_0-z} E_o y dy = 0 \tag{2-15}$$

Where E_{Si} is the Young's modulus of silicon and E_o represents the Young's modulus of silicon dioxide. Therefore the neutral axis can be expressed as:

$$Na = \frac{\frac{t_s^{\,2}}{2} + \frac{E_o t_0}{E_{Si}}\left(t_s + \frac{t_0}{2}\right)}{t_s + \frac{E_o t_0}{E_{Si}}} \tag{2-16}$$

Thus *d* can be described as:

$$d = t_s + t_0 - Na \tag{2-17}$$

Since t_0 is known, so if t_s and *y* is a certain value, the length can be calculated by equation (2-14). From equation (2-10) and (2-11) the strain at any location *z* in a beam as a result of a bending moment is:

$$\varepsilon_z = \frac{M}{EI} d = \frac{12M}{Ebt^3} = \frac{3yd}{L^3} z \tag{2-18}$$

Thus the strain sensitivity become:

$$\frac{d\varepsilon}{dy} = \frac{3d}{L^3} z = \frac{3d}{L^2} \cdot \frac{z}{L} \tag{2-19}$$

It is obvious that for a given deflection, the strain increases linearly along the beam. So the maximum strain sensitivity is at the base when *z*=*L*,

$$\frac{d\varepsilon}{dy} = \frac{3d}{L^2} [\frac{strain}{displacement}] \tag{2-20}$$

For the MRR designed by TNO the accuracy of ring resonator with our current setup is 1 pm and the optical sensitivity is $\frac{\mathrm{d}\lambda}{\mathrm{d}\varepsilon} = 0.478[\frac{pm}{\mu\varepsilon}]$, then the minimum detectable strain is:

$$\varepsilon_{\min} = 1 \div \frac{d\lambda}{d\varepsilon} = 1pm \div 0.478 \left[\frac{pm}{\mu\varepsilon} \right] = 2.128\mu\varepsilon \tag{2-21}$$

If the strain at the base is bigger than this value, the design is feasible. The strain at base of the cantilever is:

$$\varepsilon_{z,base} = \frac{3dy}{L^2} = 3dy \cdot \frac{F_s}{3Edyn} = \frac{F_s}{En} = 1213\mu\varepsilon \tag{2-22}$$

It is apparent that for this design $\varepsilon_{z,base}$ $\varepsilon_{\min}$, so it meets the requirement for minimum detectable condition. From Table 2-1 we can see that increasing the length will decrease the displacement sensitivity. Since the displacement sensitivity is:

$$\frac{d\lambda}{dy} = \frac{d\varepsilon}{dF} \cdot \frac{d\lambda}{d\varepsilon} \cdot \frac{dF}{dy} = \frac{Ld}{EI} \cdot 0.478 \cdot \frac{3EI}{L^3} = 0.478 \cdot \frac{3d}{L^2} \tag{2-23}$$

This means the cantilever cannot be too long, or it will lose displacement sensitivity.

Now considering all mentioned above a table of different lengths with a certain

maximum deflection and thickness can be generated:

y / t_s	0.1	10	20	30	40	50	60	70	80	90	100
5	99.1	313.4	443.2	542.8	626.8	700.8	767.7	829.2	886.4	940.2	991.0
10	126.9	401.2	567.4	694.9	802.5	897.1	982.9	1061.5	1134.8	1203.7	1268.8
15	149.4	472.3	668.1	818.2	944.8	1056.3	1157.1	1249.8	1336.1	1417.2	1493.8
20	168.9	534	755.2	924.9	1068.0	1194.0	1308.0	1412.8	1510.4	1602.0	1688.6
sd	580	58.0	34.8	24.9	19.3	15.8	13.4	11.6	10.2	9.2	8.3

Table 2-1 Detail designs of different length with a certain maximum deflection and thickness

Note: The unit for y is μm

The unit for t_s is μm

The unit for length is μm

The unit for Wavelength Shift is pm

The unit for *sd* (displacement sensitivity) is pm/μm

As an example if the thickness is $5\mu m$ and the maximum deflection at the tip is $80\mu m$, then the maximum length is calculated to be $886.4\mu m$.

2.4 Conclusion

This chapter introduces some basic theories related to the beam geometry calculation. From Euler-Bernoulli beam theory, the length of the cantilever has been determined as shown in Table 2-1. For the fabrication of the devices we select a length of $668.1\mu m$ and a thickness of $15\mu m$ because this geometry is very hopeful to achieve the same optical sensitivity as MRR. So far the length of the cantilever has been determined, while for the width the layout of the MRR needs to be considered. This will be discussed in chapter 3.

Reference

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[4] *Beer, F.; Johnston, E.R. (1984), Vector mechanics for engineers: statics, McGraw Hill, pp. 62–76.*

Chapter3 Design of the MRR with cantilever

3.1 The layout of the MRR

The goal of this project is to design and fabricate a cantilever containing the MRR made by TNO. To design this cantilever, it is important to have a clear understanding of the MRR layout. Figure 3-1 is a picture of a single structure. The micro ring resonators in the TNO are all folded micro ring resonators. This geometry makes the "optical path" longer than the circle one. Consequently, the optical sensitivity of the MRR is enhanced. The red line in Figure 3-1 represents a multimode interference coupler (MMI) and the purple line denotes the waveguides. Figure 3-2 is the over-all chip layout containing many folded micro ring resonators and waveguides structures, and they are different MRRs. More detailed specifications will be given later.

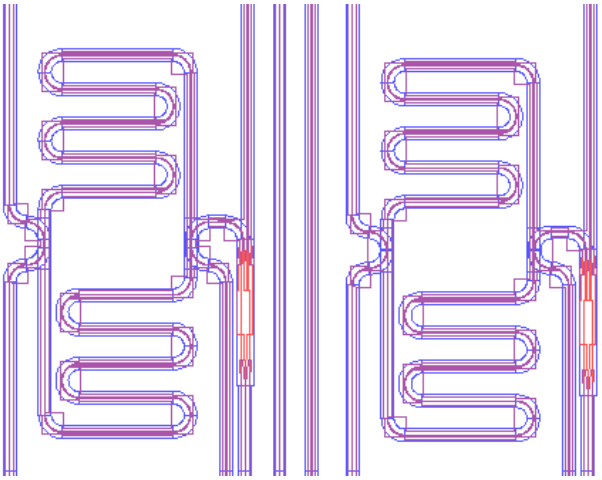

Figure 3-1 Layout of the folded ring.

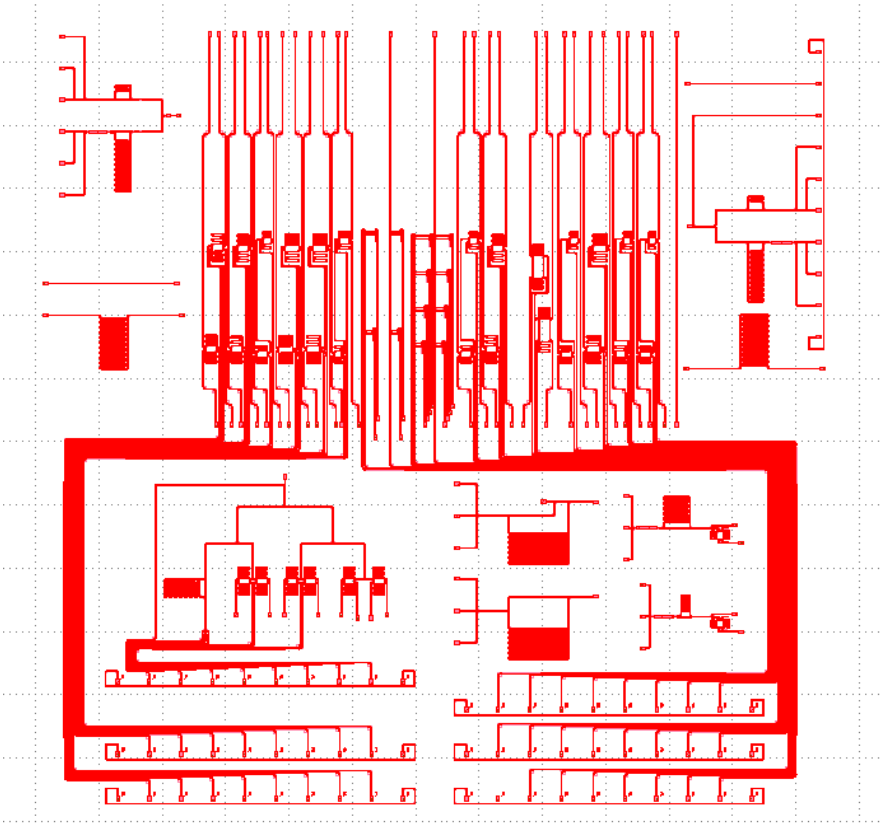

Figure 3-2 Overall layout of the MRR.

In this chip there are three types of ring configurations: type C (coupler), type S (serial) and small rings (serial). Type C configuration is shown in Figure 3-3. The input waveguide is split in 1×2 multimode interference coupler (MMI) to address two ring resonators to be used in "through" mode, a ports "in", while R and S are available for free-space coupling and ports A and D can be used for testing. Through port "in" to R is an operation for this reference ring, in this situation ports A and B are used for testing. And for the sensing ring, port "in" to S is the operation, meanwhile C and D can be used for testing.

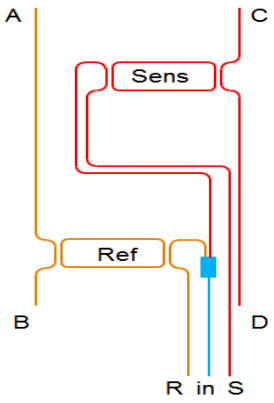

Figure 3-3 Configuration of Type C.

Type S, shown in Figure3-4, is almost the same as Type C, the difference is whether there is a MMI coupler or not. This type input waveguide from R to S addresses two ring resonators in series. Port R and S are available for free-space coupling, and A, D is used for testing. All rings in Type C and Type S are folded as illustrated in Figure 3-1, this enables rings have larger length, therefore, increasing the resonator sensitivity to defection.

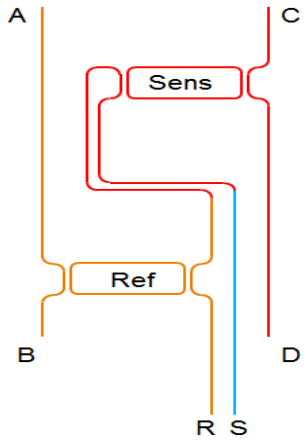

Figure 3-4 Configuration of Type S

Type small rings in serial configuration, illustrated in Figure 3-5 has input waveguides addressing two ring resonators in series, while the rings of Type C and Type S are actually folded rings. For this type the rings are much smaller than layout od S or C, because this configuration is only used for testing.

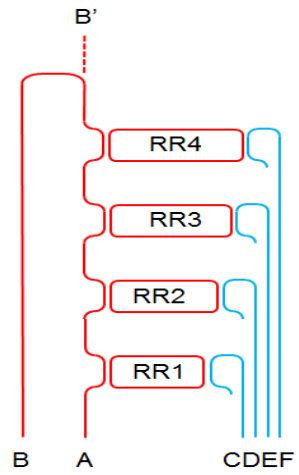

Figure 3-5 Configuration of Type small rings.

This layout has two different polarizations: TE and TM mode. Rings always come in

pairs: one for sensing and the other one for reference. They are connected in series or parallel by means of MMI coupler. Table 3-1 reports in detail the implemented configurations. TE mode is selected because the input laser that is used for this device is compatible with this mode. So from the table ring resonator C1, C2, C3, C7, S1, S2 and S3 are reasonable for further design of the cantilever. Moreover, taken the overall layout of the chip into account, only C1 is suitable for positioning in the cantilever (from Figure 3-8 it is obvious that for a long beam only C1 fits the beam).

		C1	C2	C3	C4	C5	C6	C7		S1	S2	S3	S4	S5	S6
design FSR	[nm]	0.50	0.50	0.50	0.50	0.50	0.50	0.50		1.00	1.00	1.00	1.00	1.00	1.00
polarization	[-]	TE	TE	TE	TM	TM	TM	TE		TE	TE	TE	TM	TM	TM
desinged for ambient index	[-]	1.0	1.3	1.5	1.0	1.3	1.5	1.0		1.0	1.3	1.5	1.0	1.3	1.5
ring coupler	[-]	dir	dir	dir	dir	dir	dir	MMI		dir	dir	dir	dir	dir	dir
dual ring configuration	[-]	MMI	MMI	MMI	MMI	MMI	MMI	MMI		serial	serial	serial	serial	serial	serial
directional coupler length (both rings)	[um]	5	2.5	1.1	0	1	2	MMI		2.5	0.8	0	0	1	2
directional coupler gap (both rings)	[um]	0.18	0.18	0.18	0.5	0.5	0.5	MMI		0.18	0.18	0.18	0.5	0.5	0.5
physical length sensing (top) ring	[um]	1124.16	1119.16	1116.16	1364.16	1366.16	1368.16	1377.76		573.50	570.10	568.50	538.50	690.50	542.50
physical length reference (bottom) ring	[um]	1124.16	1119.16	1116.16	1364.16	1366.16	1368.16	1377.76		693.50	690.10	688.50	688.50	540.50	692.50
FSR sensing (top) ring	[nm]	0.496	0.498	0.499	0.496	0.495	0.495	0.405		0.972	0.978	0.981	1.257	0.980	1.247
FSR reference (bottom) ring	[nm]	0.496	0.498	0.499	0.496	0.495	0.495	0.405		0.804	0.808	0.810	0.983	1.252	0.977
delta FSR / mean FSR	[-]	0.000	0.000	0.000	0.000	0.000	0.000	0.000		0.189	0.190	0.191	0.245	0.244	0.243

Table 3-1 Implemented configuration of ring resonator

Figure 3-6 is a layout of a ring resonator test port. When the device is finished, using this table and reading the configuration of all these three types, it is possible to find the proper port for testing or operation.

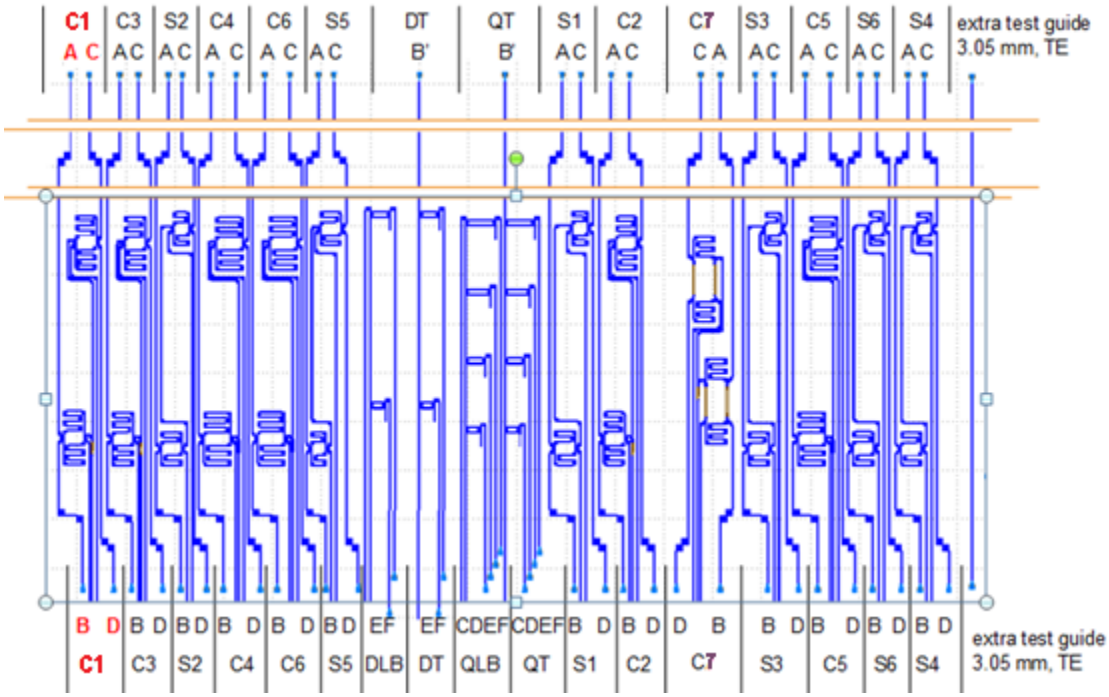

Figure 3-6 Ring resonator test port layout.

Given the gap between each ring resonator is about 50μm (see Figure 3-7), this value compared to the length of the cantilever is very small (from Table 2-X the length of the shortest cantilever is 99.1μm) and the light used for this project is TE mode. Considering all above it is better to put the cantilever on the left edge of the chip and use C1 for sensing. Because the sensing ring resonator and the reference ring resonator have the same working performance (see Figure 3-8), for each chip two cantilevers are available, as also shown in Figure 3-8.

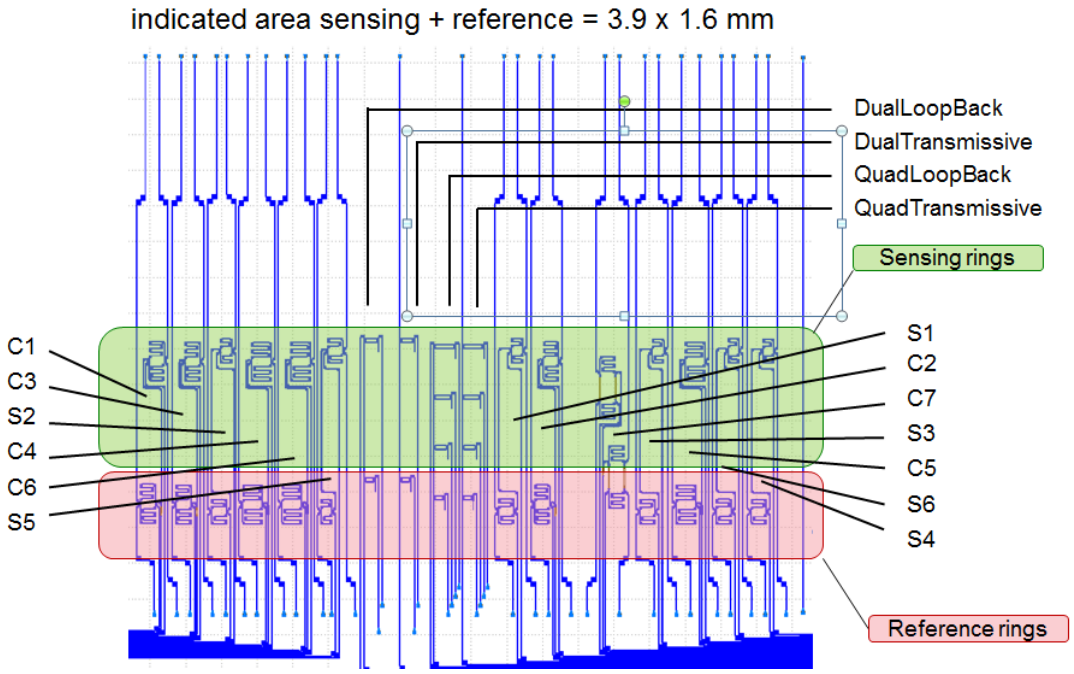

Figure 3-7 Location of ring resonators on the chip.

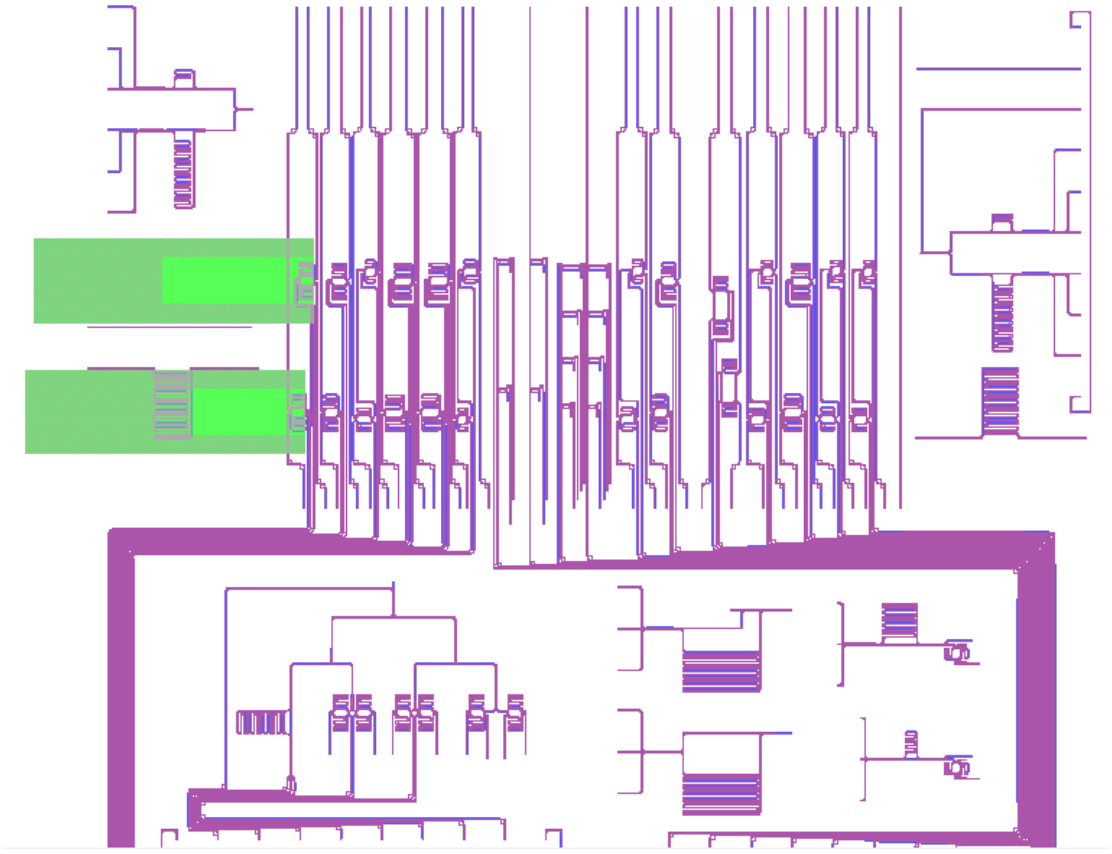

Figure 3-8 Layout of the cantilever and the whole chip.

In Figure 3-8, on the left side of the layout there are 2 cantilevers (green areas). The

shadow part is the mask for the back side, and the light green one is the mask for front side. These masks are shown below in Figure 3-9 and Figure 3-11, and Figure 3-10 is a zoomed in picture of a single pair cantilevers.

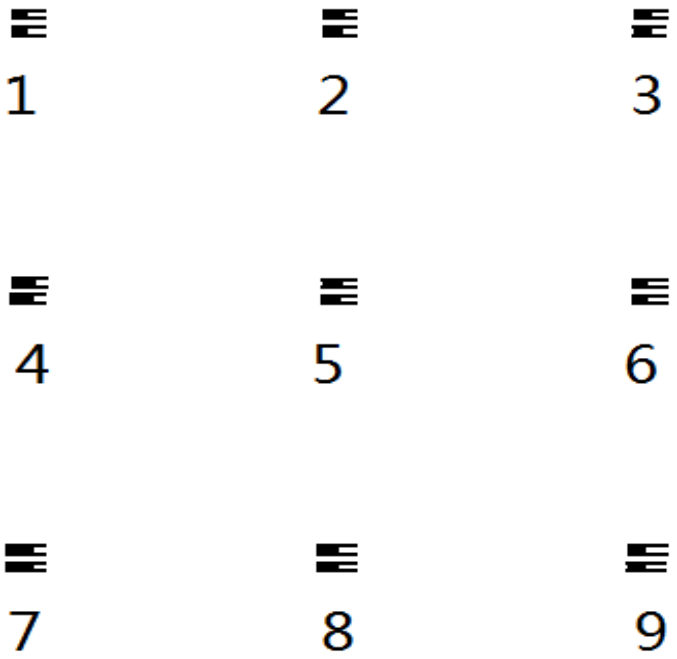

Figure 3-9 Mask for the definition of the cantilevers on the wafer front side.

Figure 3-10 A single pair of cantilevers.

In Figure 3-9 there are 9 different pairs of cantilevers. Chapter 2 lists a table of different lengths versus different thicknesses. Here we select 9 of them to be included in the mask for the cantilever definition at the wafer front side. The geometrical parameters for corresponding configurations are listed below.

Configuration	1	2	3	4	5	6	7	8	9
Length(μm)	802.5	546.4	694.3	472.3	668.1	818.2	534	755.2	924.9
Thickness(μm)	10	10	10	15	15	15	20	20	20
Width(μm)	289.95	289.95	289.95	289.95	289.95	289.95	289.95	289.95	289.95

Table 3-2 Detail parameters of 9 different cantilevers on the mask.

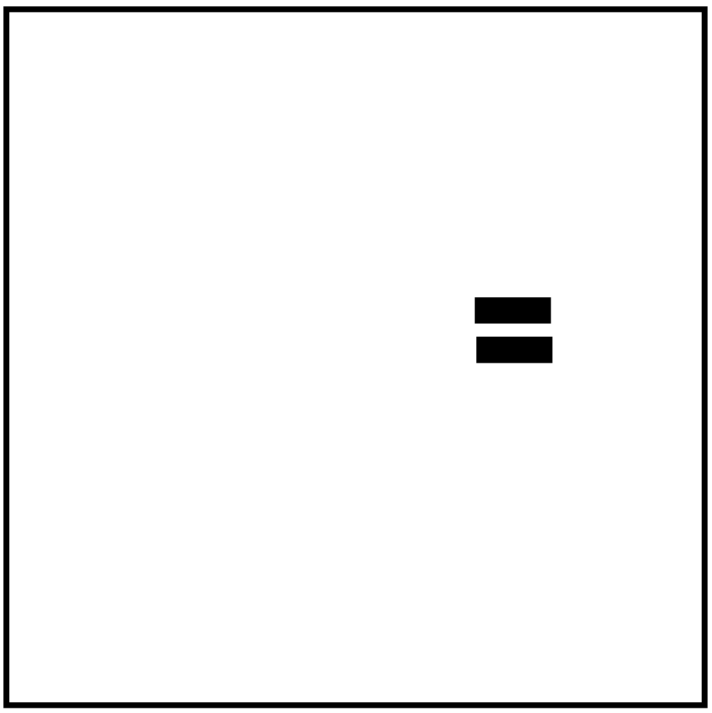

Figure 3-11 Mask for back side.

While for the back side, as the maximum length of the cantilever is 886.4 μm (see chapter 2.3) so the length of the back side mask should longer. We defined it to be 972 μm, and this can fit all cantilevers. For the width, not only guarantees the width of the pattern for backside is bigger than that of front side, but also makes sure two patterns will not contact each other. So we make it 519.65 μm.

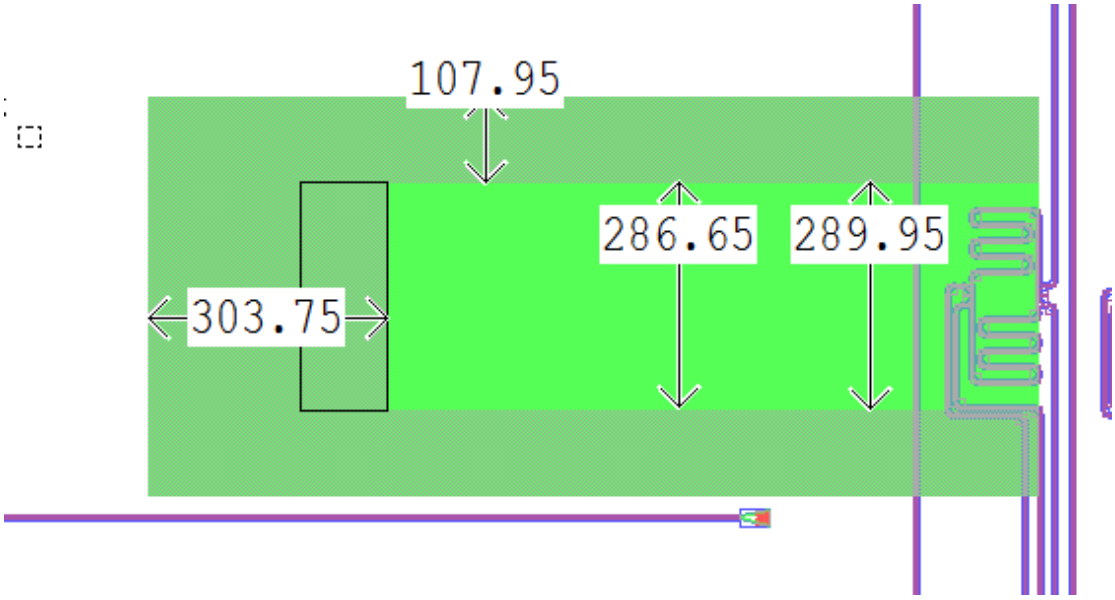

Figure 3-12 Layout of the 5th(see Figure3-9) cantilever.

The width of the cantilever is not as relevant as the length, displacement sensitivity, and maximum strain. Thus, for the width we just take a safe margin to accommodate variation during the etching process or small misalignment, so I make it 290 μm which is a little bigger than the width of the MRR. As illustrated in Figure 3-12, the light green area denotes the cantilever and the dark green areas denotes the mask pattern used for the front side.

Now that the mechanical design of the device and the corresponding mask design have been finished, we need to assess which materials can be used for the fabrication of the envisioned structure. The following section will discuss this aspect.

3.2 Material of the MRR

The original chip from TNO is based on a SOI (Silicon-On-Insulator) wafer. There are 3 layers: a device layer, a buried oxide layer and a substrate layer. Figure 3-11 shows a cross section of this structure. The grey color represents silicon and the yellow part is the buried oxide layer. The MRR and waveguides are made of silicon in the so called device layer. The buried silicon dioxide layer separates the device layer from the silicon substrate. The thickness of each layer, important information for the

development of the fabrication flow, is provided by TNO and it is summarized in Table 3-3.

Layer	Device layer	Buried oxide layer	Substrate
Thickness	200 nm	2μm	700 μm

Table 3-3 Detail thickness for each layer.

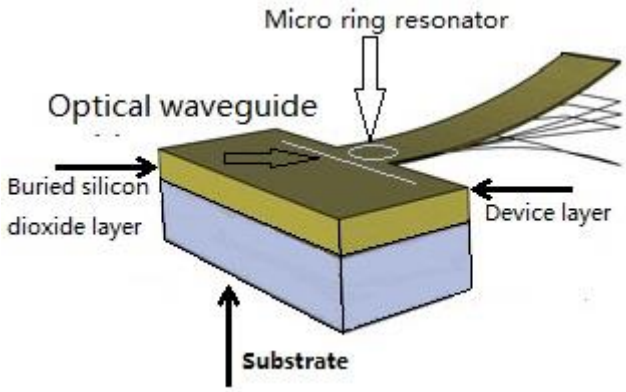

Figure 3-11 Structure of the chip.

3.3 Conclusion

From the analysis of the layout of the MRR and the material used for the realization of MRR provided by TNO, the geometrical parameters of the cantilever have been defined and all information for the development of a suitable post process flow for the chips so to realize the cantilevers now available. This process will be discussed in chapter 4.

Chapter 4 Fabrication

4.1 The basic process modules

In this section, I will discuss what processes are required in this project and why we choose them. Starting from the chips containing the MRR I get from TNO my goal is to design and fabricate the cantilever beam around the MRR. To get a free standing cantilever the main modules needed are lithography and etching as we need to etch the silicon dioxide used as masking layer to define the silicon cantilever, and the bulk silicon (device layer and substrate) to release the cantilever.

4.1.1 Etching Techniques

There two etching methods: wet chemical etching and dry etching plasma systems. Wet chemical etching is commonly used to etch windows in silicon dioxide layer when dimensions are not critical and it is a low cost and easy to implement method. This kind of etching cost not too much and is easy to manipulate. Moreover, this kind of etching tends to be an isotropic process which means etching equally in all directions, so it is less suitable to define high aspect ratio structures.

BHF is a wet chemical etchant, for the removal of silicon dioxide, selectively to silicon or photoresist. This means it etches silicon dioxide more rapidly than it etches silicon or photoresist at room temperature [1]. For this project as the chip has a buried silicon dioxide layer and PECVD oxide layer is used as masking layer (this will be discussed later), BHF is possible choice to define the mask pattern into the oxide layer. The etching rate of BHF 1:7 is $1.2\ \mathrm{nm/s}$.

Dry plasma etching process, being an anisotropic, directional etching, can avoid the undercutting problem which happens in wet etching process. Deep reactive ion etching of silicon (DRIE) is an advanced kind of dry etching of silicon, specially

developed to define high aspect ratio strutures. This etching techinique allows to realize very deep and accurate microstructures, independently of crystal and pattern orientation[1]. So this etching method is used to etch both the silicon device layer and the bulk. To see clearly the different of these two etching techniques, table 4-1 is a detail comparision between these two etching techniques.

WET	DRY
● Etch rate dependent on crystal plane orientation	● Etch rate mostly independent on crystal plane orientation
● Well defined structures	● Well defined structures
● Control of vertical dimension through etch-stop techniques	● Control of lateral dimension through strong anisotropy and crystal orientation independence
● Low cost process	● Medium/fast etch rates (2-10µm/min)
● Accurate control of lateral dimensions, but large spacing between structures	● Vertical dimensions depend on layout/process
● Slow etch rates (0.5-1.5 µm/min)	● Expensive equipment
● Etch solution @ T=60°-115°C	

Note: red lines represent advantages and green lines denote disadvantages.

Table 4-1 Advantage and disadvantage of wet and dry etching.

4.1.2 Lithography

Masks contains the patterns of windows that are transferred to the surface of the silicon wafer using a process called lithography [2].To fabricate a free standing cantilever, lithography is a necessary process, as it transfers the pattern from the mask onto the chip to define where to etch the silicon so to form the beam. Since the chips I get from TNO are very small, so they cannot be handled by the wafer stepper

and contact lithography is used. Figure 4-1 is a picture of the contact aligner equipment used. The first step is coating of the chip with photoresist, followed by a soft bake at 95℃ for 1 minute, and then the chip is fixed on the wafer for patterning.

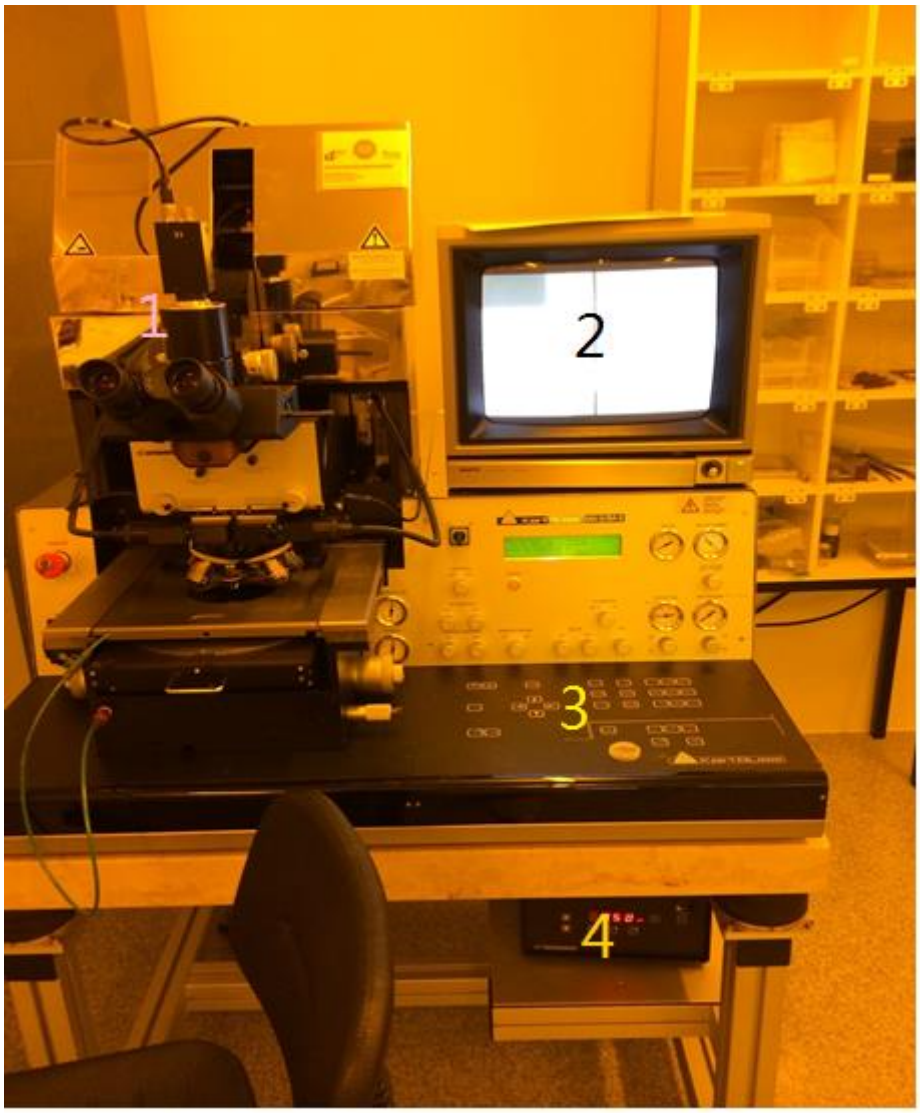

Figure 4-1 A picture of the contact lithography machine: 1) is the microscope, 2) is the monitor, 3) is the parameter panel, 4) is the switch of the light source.

4.2 Main process flow chart

At beginning, we choose photoresist as the masking layer, while after some trails we find that photoresist does not adhere well, so I replaced the photoresist with PECVD silicon dioxide as masking layer, and this issue is shown in next section. This oxide is about 500 nm thick and it can protect the device layer better than photoresist when

etching silicon layer. What's more SiO_2 can integrate on silicon layer so cohesively and it is easy to deposit via PECVD. But after this first depositing PECVD silicon dioxide two more PECVD silicon dioxide layers on both sides are deposited. Figure4-4 is a cross section of the starting with PECVD silicon dioxide deposited on it to protect the rings and waveguides. Table 4-1 lists the different thicknesses of each layer.

Figure 4-2 Cross section of the cantilever after PECVD SiO_2.

Layer	PECVD(SiO_2)	Device layer(Si)	Buried SiO_2	Silicon substrate	PECVD(SiO_2)
Thickness	500nm	200nm	2μm	650μm	500nm

Table 4-2 Detail thickness for each layer.

A first important issue is how to control the thickness of the cantilever. Since this device is very small and a large part of the bulk substrate needs to be removed, i.e. it is a high aspect ratio structure, it is better to use Deep Reactive Ion Etching of Silicon (DRIE). The DRIE plasma etching machine in Dimes is Adixen AMS100 whose etching rate for silicon at $20C°$ is about $5\mu m/min$. Thus if I firstly etch down from front side to a certain thickness-which is the thickness we aim at- then release the beam by etching down from backside. By using the data in Table 4-1 and considering the etching rate, it is easy to calculate the time needed for etching can be calculated. For a thickness of$15\ \mu m$, so the time needed to form a certain thickness is 3 minutes. More detail process flow chart will be introduced as follows:

1. Start with patterned silicon of MRR and waveguides on a chip.

2. Deposit 500 nm of silicon dioxide by PECVD as a protection layer for the device layer. And on the back side as masking layer for the DRIE step.

3. Define an open “window” in the oxide on the back side: coating with photoresist SR-3017, then baking the chip 1 minute at $95\,C°$ after that exposure by contact lithography (see Figure 4-5), followed by baking at $115\,C°$ 1 minute. Finally, develop the exposed photoresist by immersing the chip in MF-322 solution for 1 minute.

4. Coating front side with photoresist, then etch PECVD silicon dioxide by BHF1:7. As the etching rate of BHF1:7 is 1.2 nm/s, it takes at least 7 minutes. Then use DI water to wash it for 10 minutes.

5. Because the substrate silicon is about $650\mu m$ thick, two etching steps are done, one using photoresist as mask and the second using silicon oxide. After 5 minutes DRIE, the photoresist is removed by acetone.

6. Patterning the Mask 2 on the front side, and doing contact lithography as step 3.

7. Open a window in front side by subsequent removal of oxide, silicon device layer and buried oxide. This is done by first an etch step in BHF1:7 solution for 7 minutes, followed by DRIE for 4 minutes and then again in BHF1:7 for at least 30 minutes followed by rinsing the chip 10 minutes with DI water.

8. Since the etching rate for DRIE is $5\mu m/min$, and the total thickness of the beam totally is $17\mu m$ ($15\mu m$ silicon substrate adds $2\mu m$ buried oxide), with about 3 and half minutes should be sufficient.

9. Continue with DRIE to etch from the backside step by step carefully, until the cantilever has been released. Then clean the photoresists remained on the chip front side.

The following parts are some pictures related to the issues encountered that happened during the fabrication.

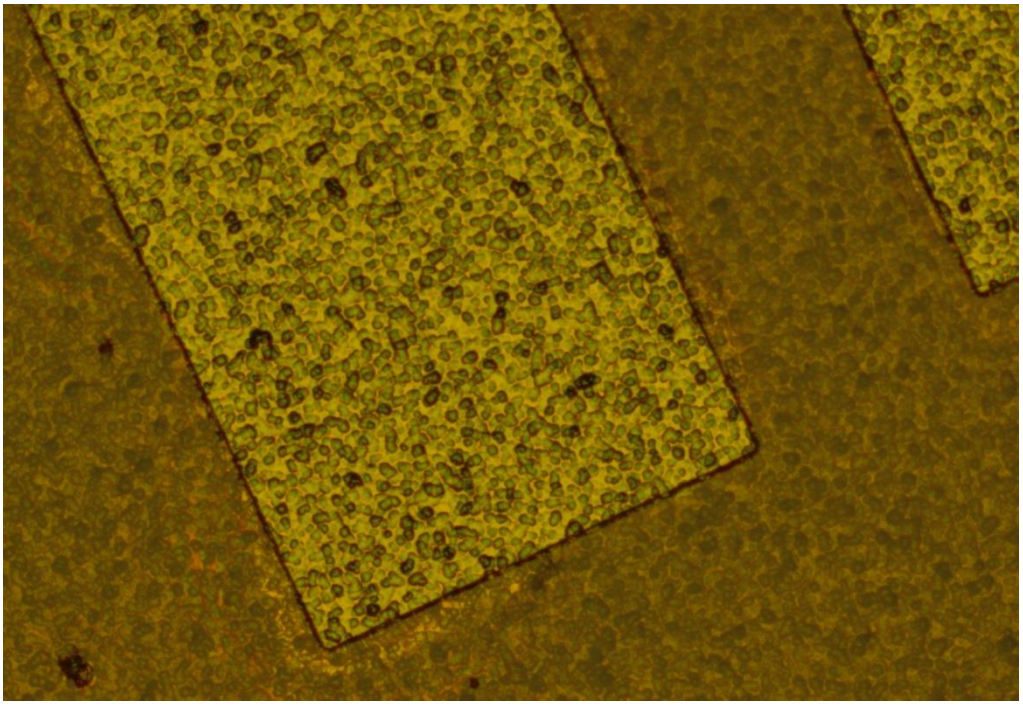

Figure 4-3 A picture taken after developing as step 3. The dark parts are photoresist and the bright parts are where the cantilever exists.

The above picture is taken after developing (see step 3), here we can see the edges of the cantilever is apparently defined, while in Figure 4-6 the edge of the cantilever on front side is not so well defined. This problem is due to the property of wet etching: isotropic process, which etched the edge of device layer. That is why I changed photoresist to PECVD silicon oxide.

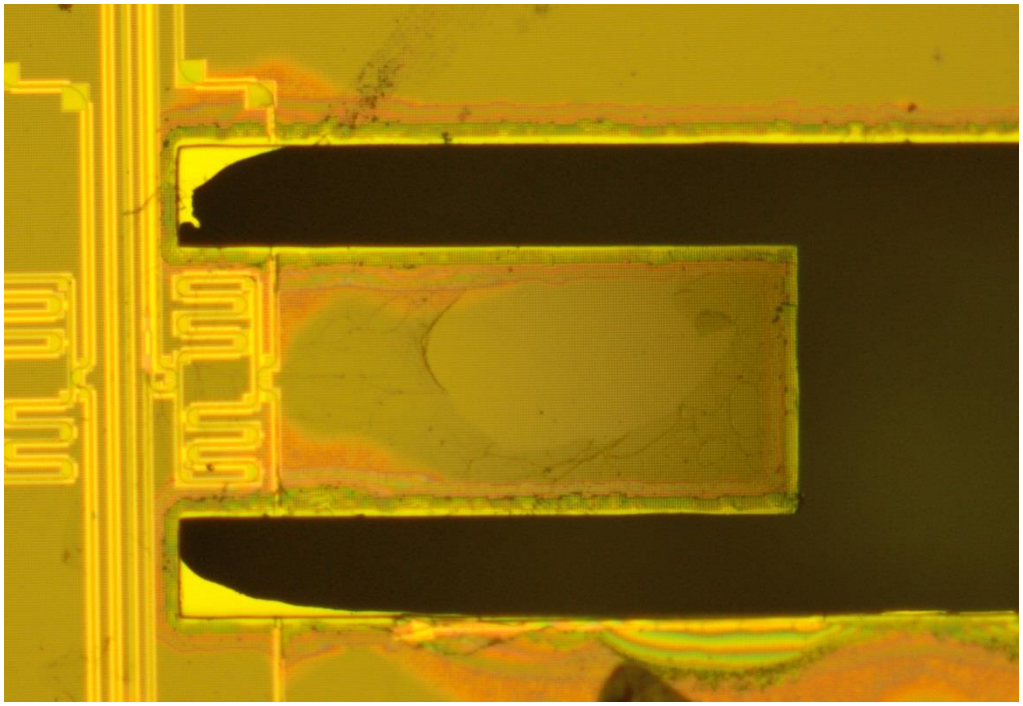

Figure 4-4 A picture of cantilever on front side.

While it is still not easy to keep ring resonator and waveguides undamaged, after 3 failed chips I place the cantilever a little far away from the straight waveguide near the base. After releasing the free standing cantilever, inspection via microscope takes place. Figure 4-8 and Figure 4-9 are pictures of these two different cantilevers, it is apparent that one micro ring resonator is damaged (see Figure 4-8).

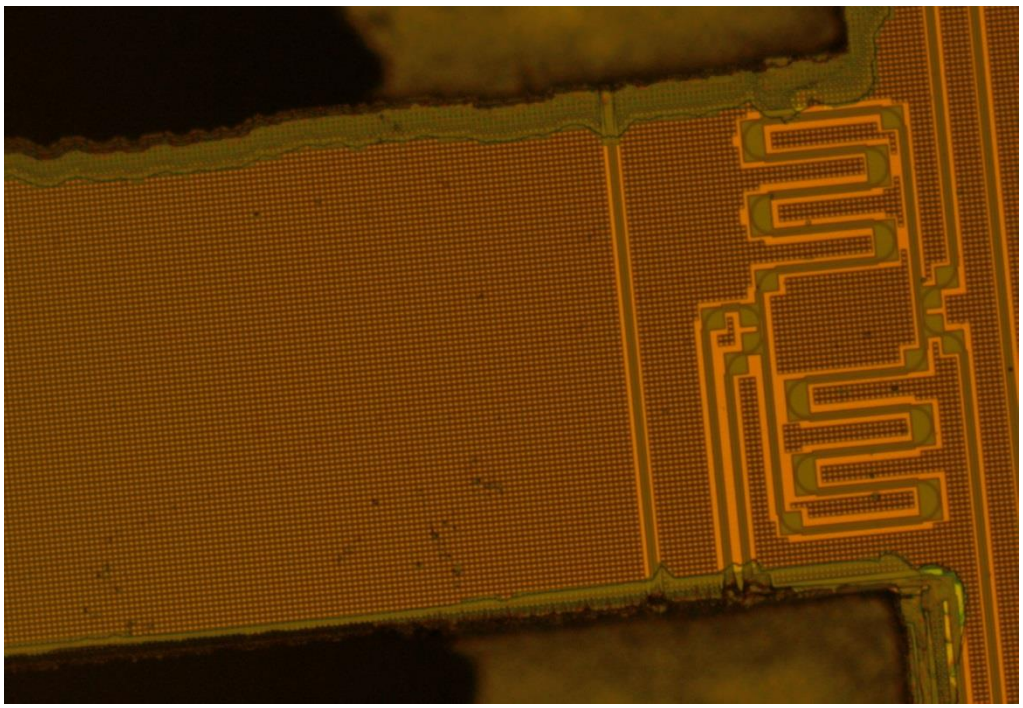

Figure 4-5 A picture of the “dameged” cantilever uses sensing MRR of C1 (see Figure 3-7).

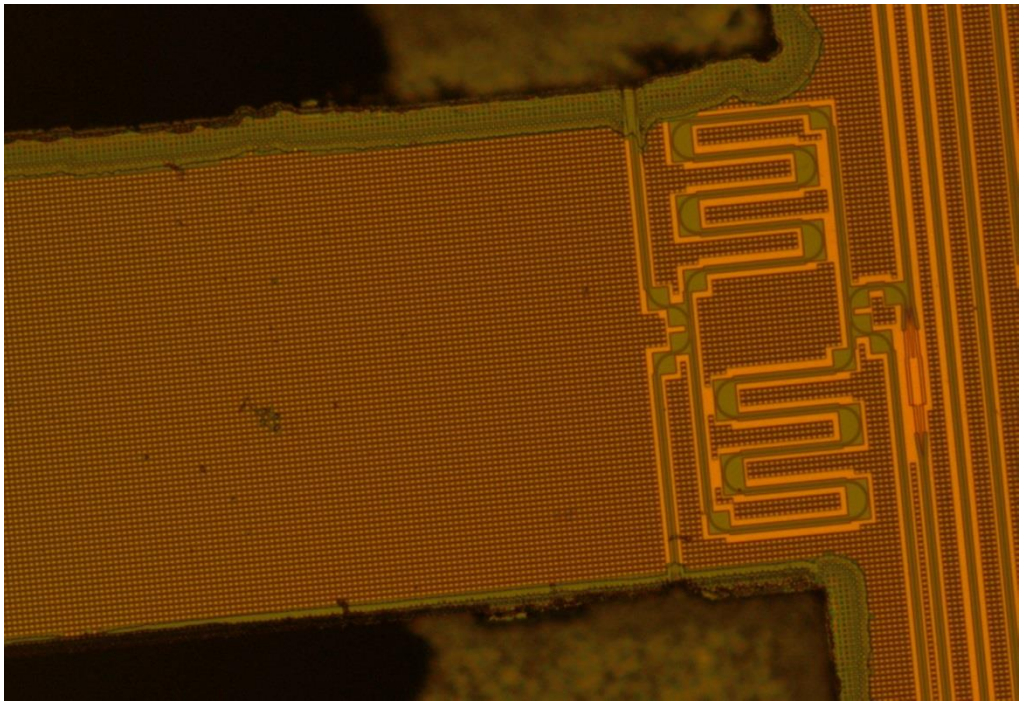

Figure 4-6 A picture of the "undamaged" cantilever uses the reference MRR of C1(see Figure 3-7).

The successfully etched cantilevers are now ready for measurements, as described in next chapter

4.3 Some issues involved in fabrication

As mentioned in chapter 3, the original chip has 3 main layers: device layer which is silicon, buried dioxide layer and silicon substrate layer. To form the cantilever as designed, we need to transfer the pattern onto the chip. The first step is to define the opening at the wafer back side. For this we need a protective layer (or hard mask layer) deposited onto the chip back side in which through lithography the regions to be etched are cleared of both photoresist and masking oxide then etching down from backside to release this beam. At beginning, photoresist is picked as a protection layer on the surface layer, while after developing under the microscope it is obvious that there are some parts of the device layer also been etched during the etching down process, Figure 4-2 and Figure4-3 are pictures I took after developing and etching down. It is obvious that some waveguides are damaged.

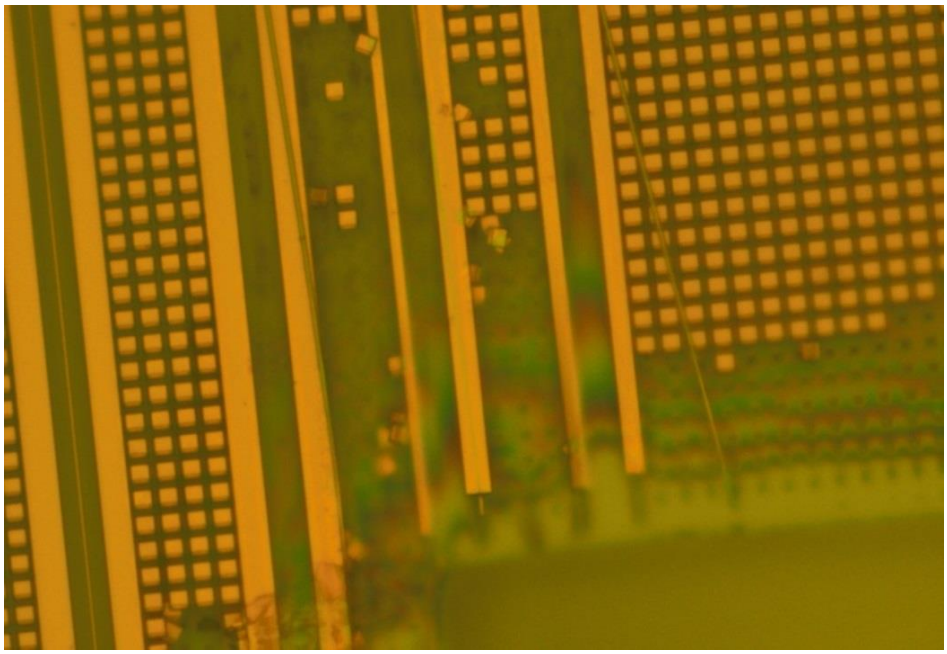

Figure 4-7 Straight waveguide has been damaged.

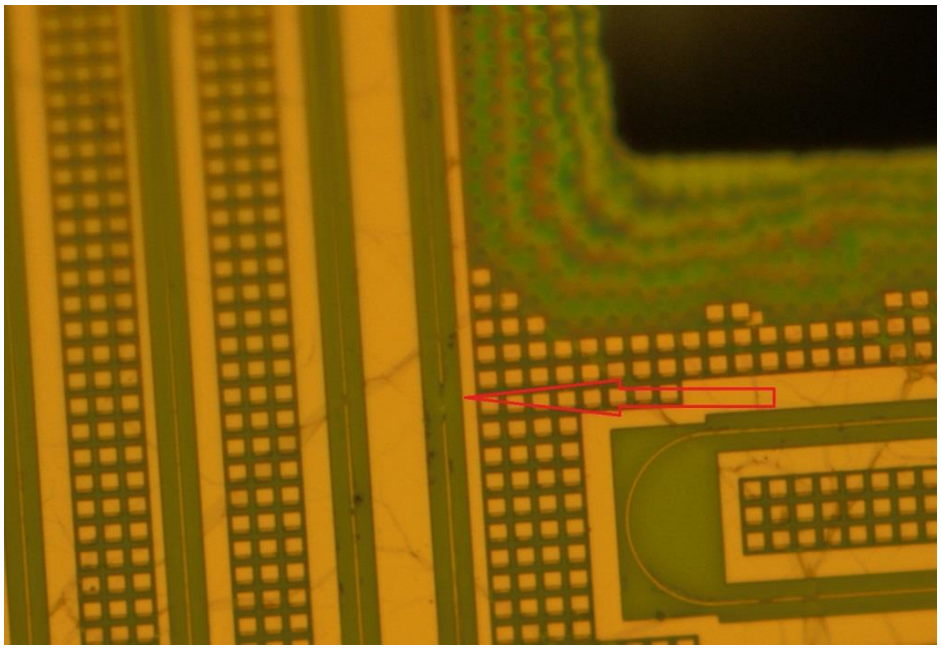

Figure 4-8 An interruption after etching down the cantilever.

Therefore, how to protect the waveguides becomes a key issue. The adhesion between photoresist and device layer is not so strong and this may be the main reason why photoresist cannot cover the device layer so well. Therefore, I changed photoresist to PECVD silicon oxide.

4.4 Conclusion

This chapter describes the main process flow developed to fabricate a cantilever with MRR and also discusses some issues encountered during the fabrication. The whole processes look not so complex, but as processing at chip lever introduces additional complexity as not all machines can handle small pieces, several problems needed to be solved and more time was spent on fabrication then initially planned. The biggest issue is the wet etching of oxide that always damages the ring resonator and waveguides. To solve this problem, I changed the protection layer and this resulted in a better approach.

Reference

[1] Neudeck G W, Pierret R F. Introduction to Microelectronic Fabrication[J]. Modular Series on Solid State Devices, 2002, 5.

Chapter 5 Measurement of the MRR with cantilever

5.1 Introduction

In order to characterize the performance of the MRR cantilever device, a series of measurements for the displacement sensor were performed. Because this device is based on a MRR, the first thing to do is to make sure whether the MRR in this device is still functional after fabrication process to release the cantilever. Then to test its operation as a sensor, it is important to know its mechanical properties such as resonance frequency, stiffness and the optical sensitivity. Note that all experiments were carried out at room temperature and at atmospheric pressure.

5.2 The measurement set up

To investigate the detectable limit of the MRR, an interrogator is required. Many interrogator concepts have been presented in literature, such as the use of scanning lasers [1], Vernier concepts [2], etc.. We use a commercial solid-state DFB laser (Thorlabs PRO800 WDM modules) which its wavelength can be tuned over a few nanometers to select one of the resonator resonances [3]. The setup of this interrogation is illustrated in Figure 5-1. Due to the coupling of the ring resonator and the waveguides the intensity of the laser that is passing through the waveguide extremely dependents on its wavelength (as shown in Fig. 5-3). Because a small shift in resonance wavelength ($\Delta\lambda$) will cause a substantial change in transmission power ΔP (see Figure 5-1, left) in order to get maximum sensitivity, we set the wavelength of the laser at the slope of the transmission diagram.. Figure 5-2 depicts the setup of the vibration-isolated ring resonator which is called “FRESCO”. This setup is used for operation or testing of the MRR chip.

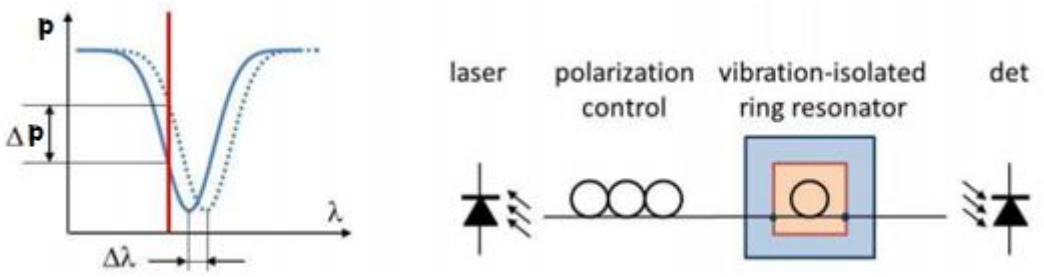

Figure 5-1 interrogation principle (left) and schematic measurement setup (right) [3]

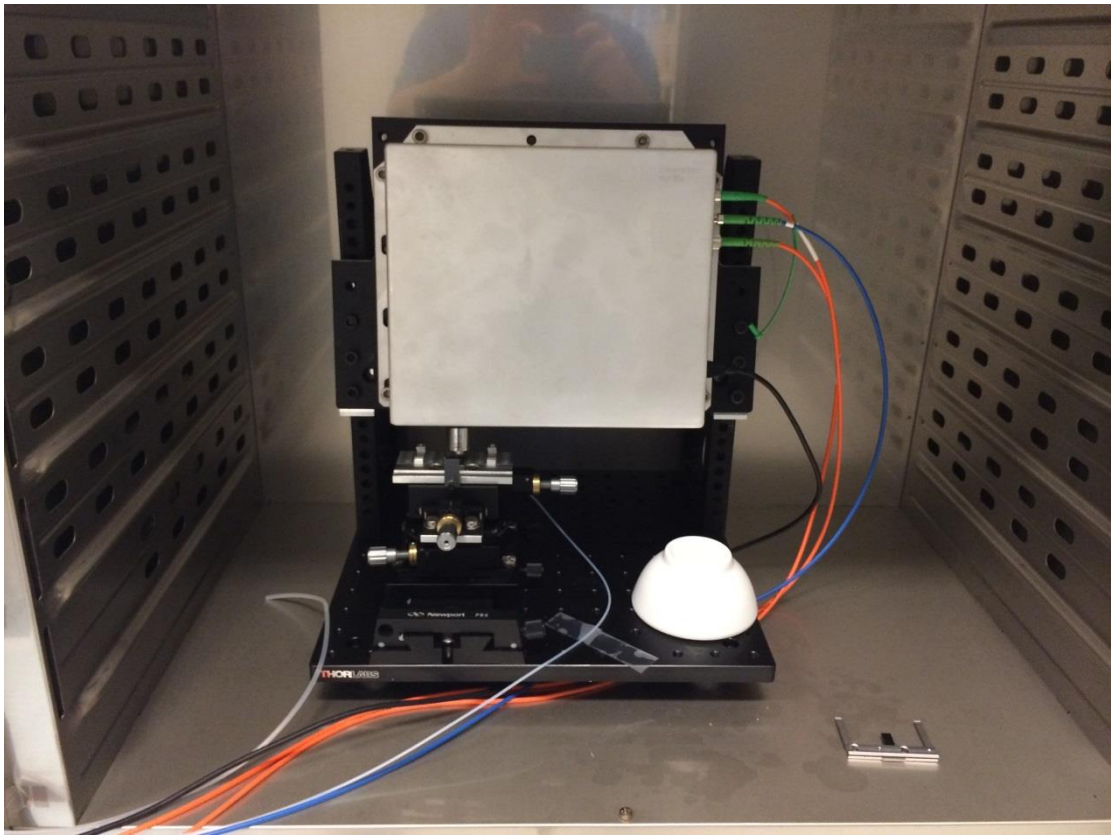

Figure 5-2 A picture of the "FRESCO" setup used for MRR testing.

5.3 Measurement procedure

We use this setup to measure the performance of the chip. From Figure 5-1, a laser with an optical polarization device is connected to the input port of the MRR, followed by a detector at the output port. Through this setup we can measure a number of wavelengths versus output power with time. From this we obtain the ring resonance shape as a function of wavelength. Figure 5-3 is the result of the transmission spectrum of this chip. The red line denotes the "undamaged" MRR by the post processing while the purple line represents the "damaged" one. It is obvious

from the diagram that the “undamaged” MRR is in good condition.

Then next measurement is to find the mechanical resonance frequency through changing the time domain data into frequency domain by Fast Fourier Transform Algorithm (FFT). This is shown in next section. Finally, we need to measure its deflection sensitivity. For this set up the easiest way of measuring the deflection sensitivity of the beam is to measure the bending of the beam due to bimorph effect. Since the beam is made up of silicon and silicon oxide that have different expansion coefficients, the cantilever will bend when the temperature is increased. We use a heater to rise the temperature and a temperature sensor to monitor the temperature change. We position the heater close to the chip and slowly heat the chip to make the cantilever bend. Then the heater is moved away from the beam for a while so the beam cools down and returns to its original position. From the analysis of the output power changes, we estimate whether this chip can achieve the sensitivity as MRR did, as illustrated in Figure 5-4 and Figure 5-5. From these two figures, it is obvious that the chip has the opposite change trend than the temperature sensor.

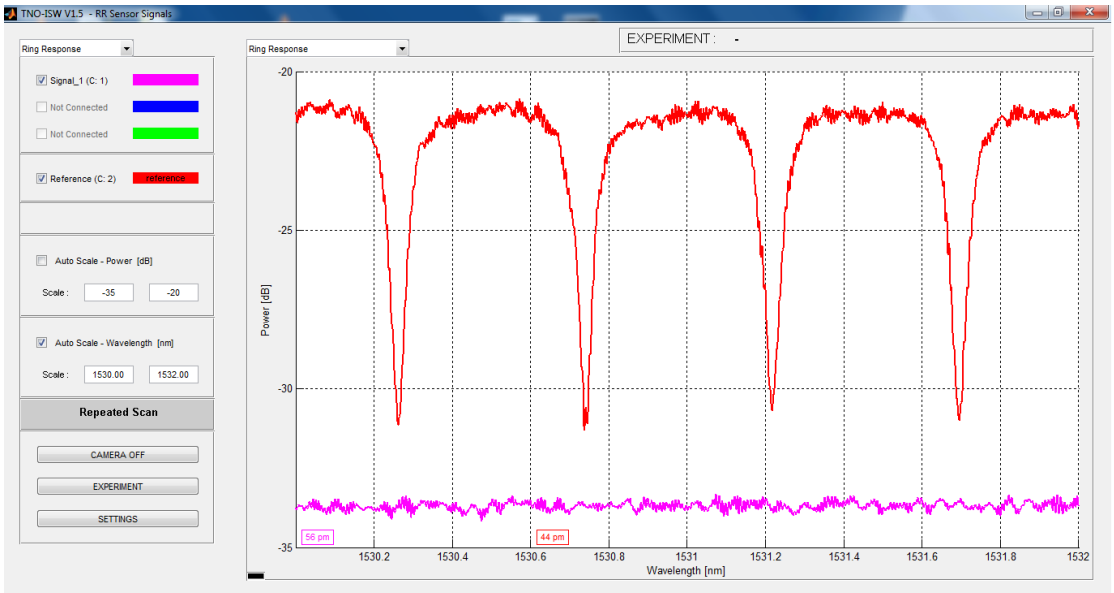

Figure 5-3 Measurement of the transmission spectrum of the chip.

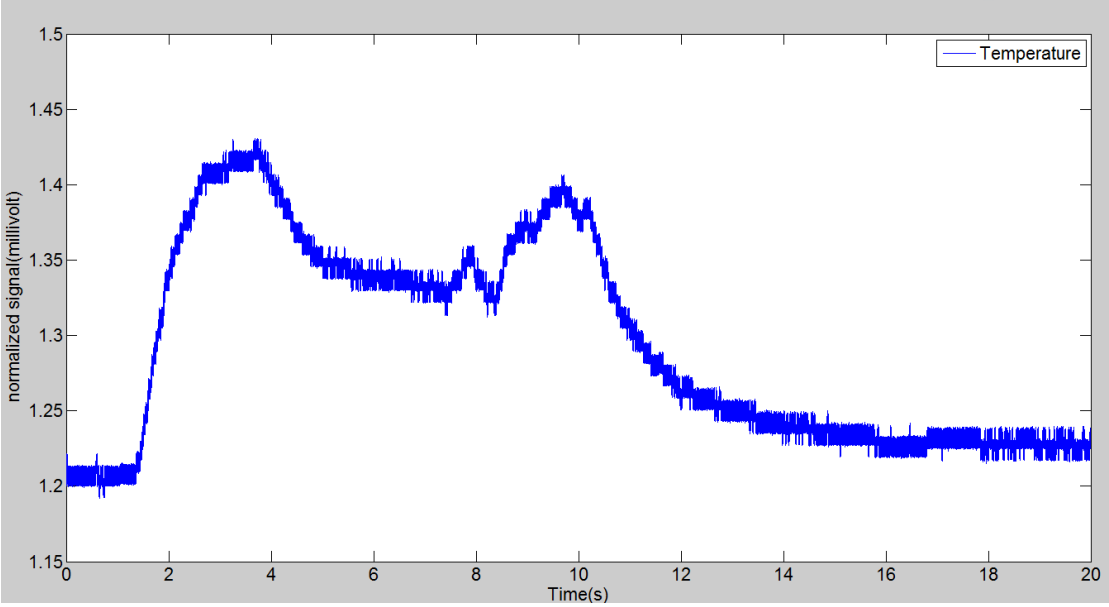

Figure 5-4 The temperature gradient versus time.

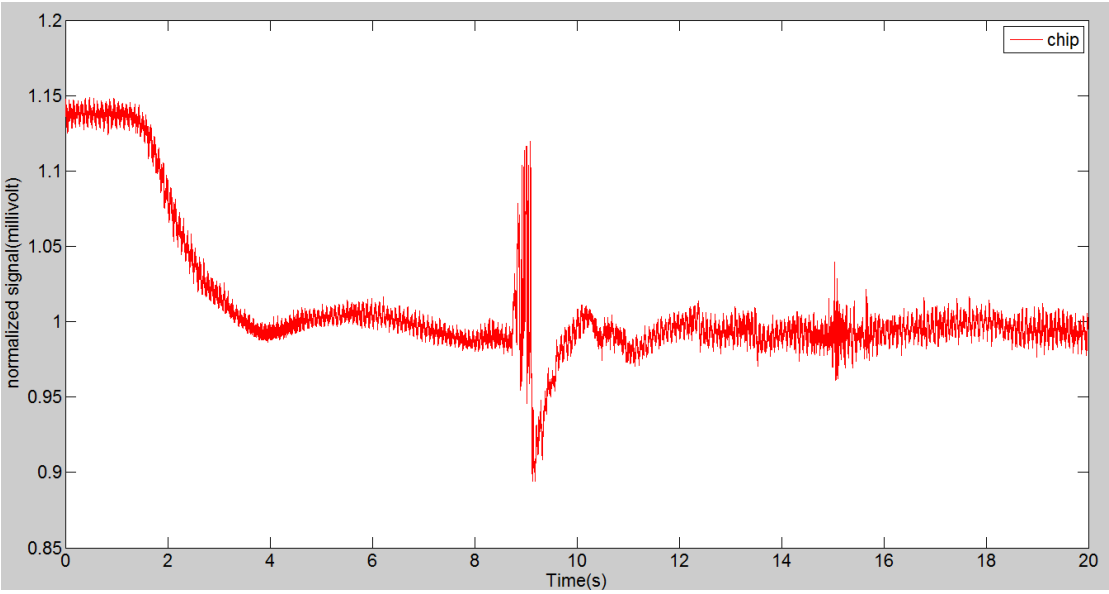

Figure 5-5 Chip output power versus time measured for temperature changes.

Figure 5-6 and Figure 5-7 are measurements after several temperature cycles. We can see that when the temperature is increasing the device output power is decreasing. This is due to the wavelength shift as Figure 5-1 describes. When we take away the heater, the temperature is decreasing, while the change of the output power for the chip is not so straightforward. This can be explained considering that the heat dissipation requires some time, and causes a delay in power change. Thus, we know this chip is sensitive enough to measure the small deflection of the cantilever due to thermal expansion. However we could not quantify the absolute

amount of power reduction due to deflection because of the practical challenges, such as the setup for measuring this is not suitable for such small chip.

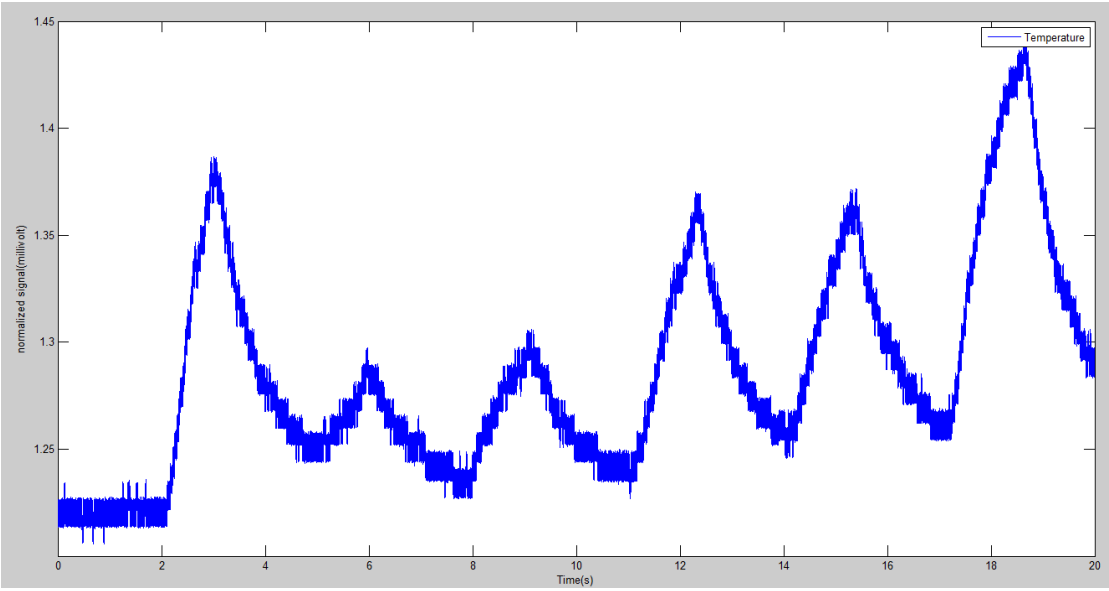

Figure 5-6 The temperature gradient versus time after several temperature cycles.

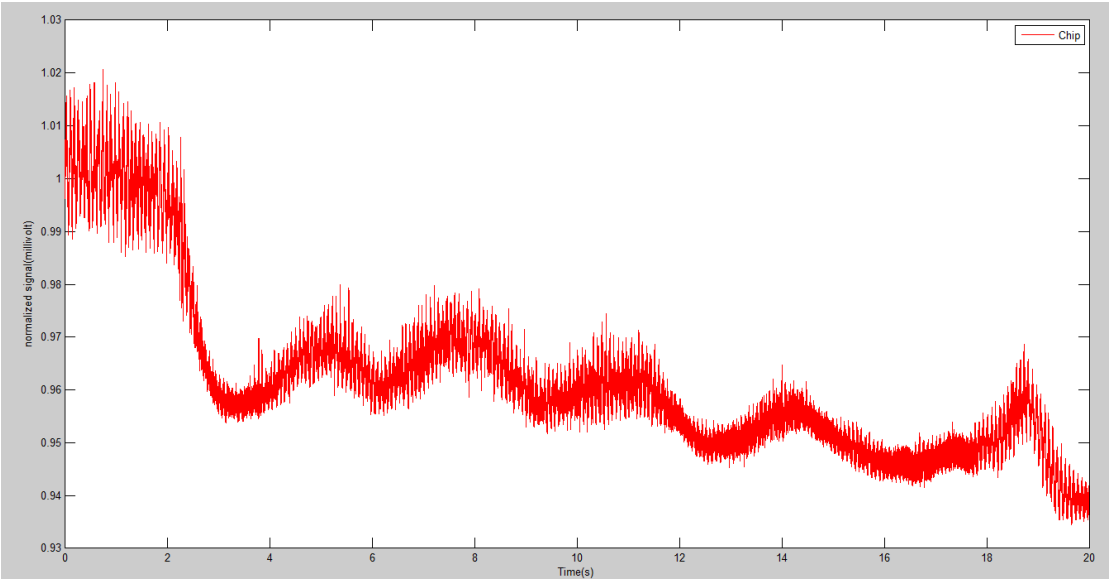

Figure 5-7 Chip output power versus time measured after several temperature cycles

5.4 Discussion

In order to have an estimate of the resonance frequency of the cantilever before measurements we first calculate the resonance frequency using Euler Bernoulli beam theory. Figure 5-8 shows a cross section of the beam where $h1$ is the distance between the neutral axis and the center line of the bulk, and $h2$ denotes the

distance between neutral axis and the center line of the silicon oxide. The mechanical resonance frequency can be expressed as:

$$f_r = \frac{1}{2\pi}\sqrt{\frac{\rho A_{eq}\cdot L^4}{3.01\cdot \mathrm{E}I_{eq}}} \tag{5-3}$$

where the $\mathrm{E}I_{eq}$ can be described as:

$$\mathrm{E}I_{eq} = E_{Si}\left(I_1 + A_1 h_1^2\right) + E_o\left(I_2 + A_2 h_2^2\right) \tag{5-4}$$

considering that $A_1 = t_s * w$ and $A_2 = t_0 * w$, ρA_{eq} is:

$$\rho A_{eq} = w*\left(\rho_{Si}\cdot t_s + \rho_{SiO_2}\cdot t_0\right) \tag{5-5}$$

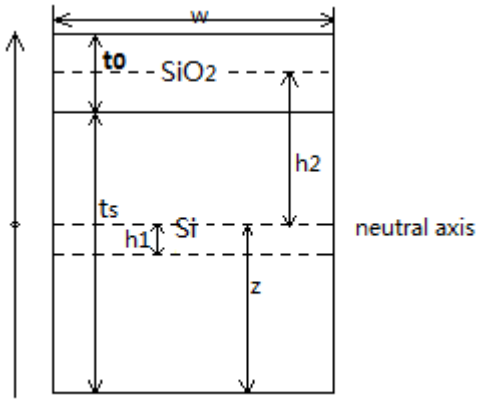

Figure 5-8 Cross section of the cantilever.

The calculated resonance frequency considering the average measured geometry is found as $f_r = 134kHz$. Note that this value is an estimated result for the mechanical resonance frequency, because the cantilever is not a cuboid and the thickness is changing along the beam. The real value can be different than this value but in the same order of magnitude.

Next we need to measure the mechanical resonance frequency around the estimated value using the thermo-noise method [4]. Since the frequency of the laser is much bigger than the resonance frequency of the cantilever, thermal noise of the cantilever can be measured in the spectrum of the output power. To measure the mechanical resonance frequency we did some measurements as previously mentioned. Figure 5-9 is one of these measurements result. It depicts the output

power versus time at λ=1552.64 nm measured with a 100k sample/sec data acquisition card.

Figure 5-10 is the result of Figure 5-9 in the frequency domain, obtained by fast Fourier transform. We can see that not only in the time domain, but also in the frequency domain, the noise level is high. This is somewhat expected because the cantilever is rather stiff and short so its thermo-noise can be easily buried under the electrical or optical noise

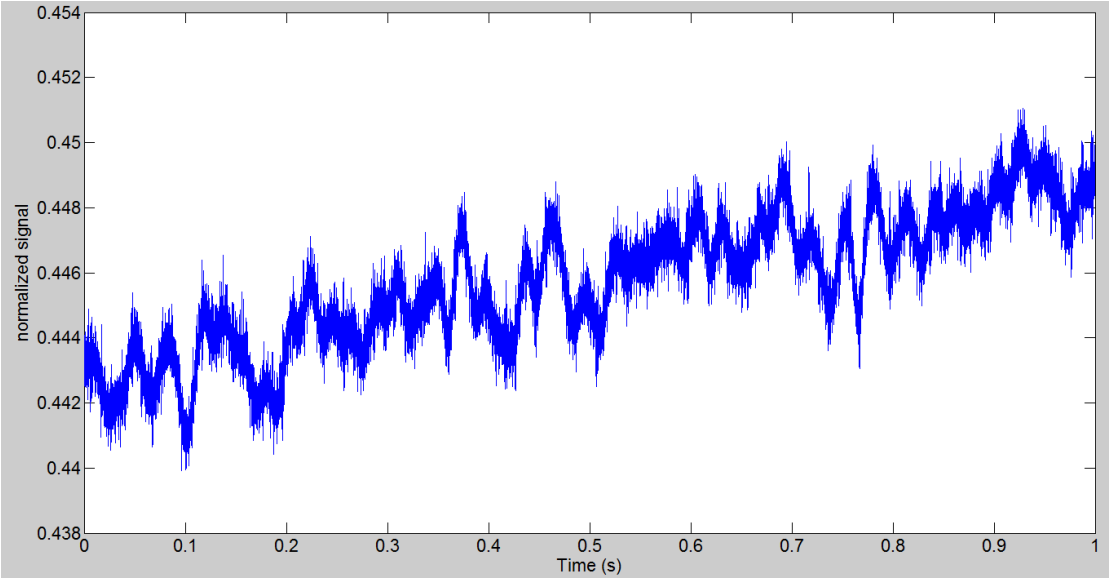

Figure 5-9 Output signal in time domain of the chip.

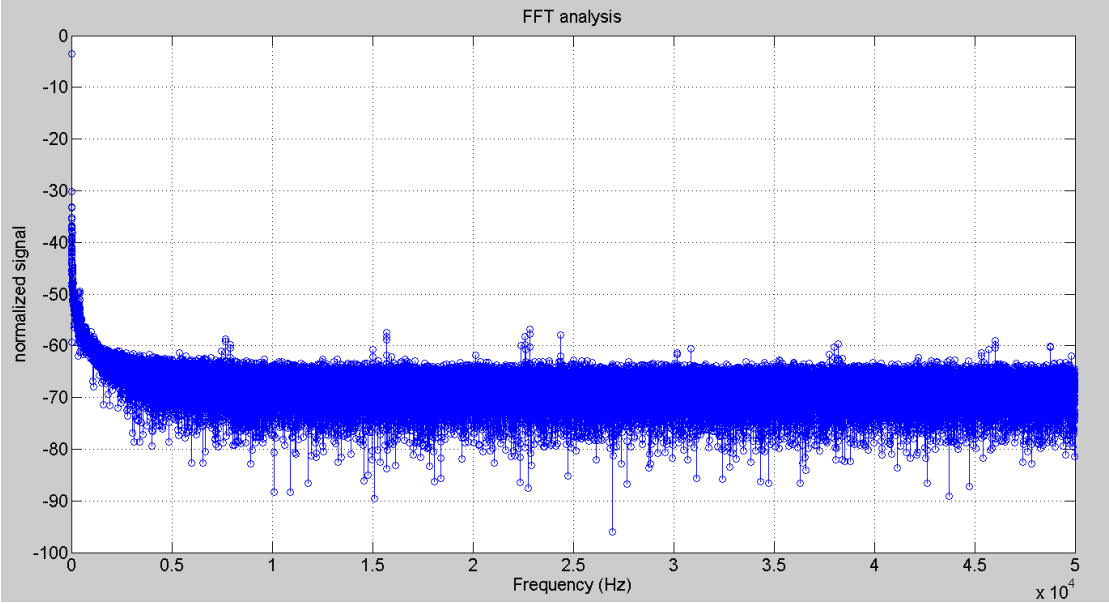

Figure 5-10 Output signal in frequency domain of the chip.

However it is known that the Brownian motion of the cantilever (thermo-noise)

linearly scales with temperature. So by decomposing the temperature dependent part of the noise from its temperature independent part, we can improve the resonance frequency measurements. The total noise can be expressed as:

$$n_{total} = n_{mechanical} + n_{measurement} \tag{5-6}$$

Where $n_{mechanical}$ is the mechanical noise due to the cantilever and $n_{measurement}$ is the noise due to the instruments of the setup and other electrical noises. While $n_{mechanical} \propto k_B T$ (T denotes the temperature and k_B is Boltzmann's constant), $n_{electrical}$ can be considered as independent from the temperature. So we first low pass filtered the temperature signal and we multiplied the total noise in average of temperature minus a minimum of the temperature to enhance the temperature dependent part of the noise and suppress the temperature independent part (see Appendix). Figure 5-11 shows the spectrum of the signal that shows a temperature dependent part enhanced over the temperature independent part.

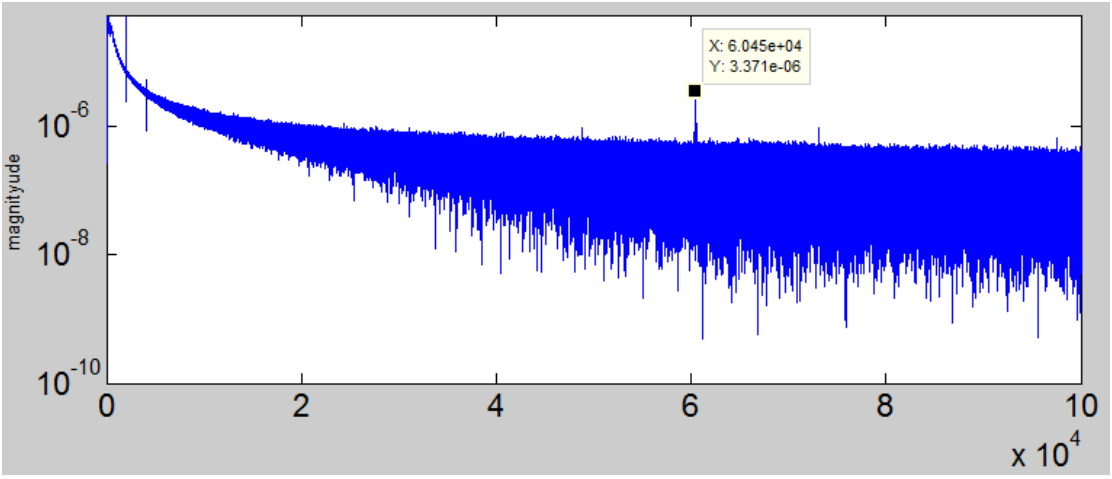

Figure 5-11 Output signal of the chip improved by averaging.

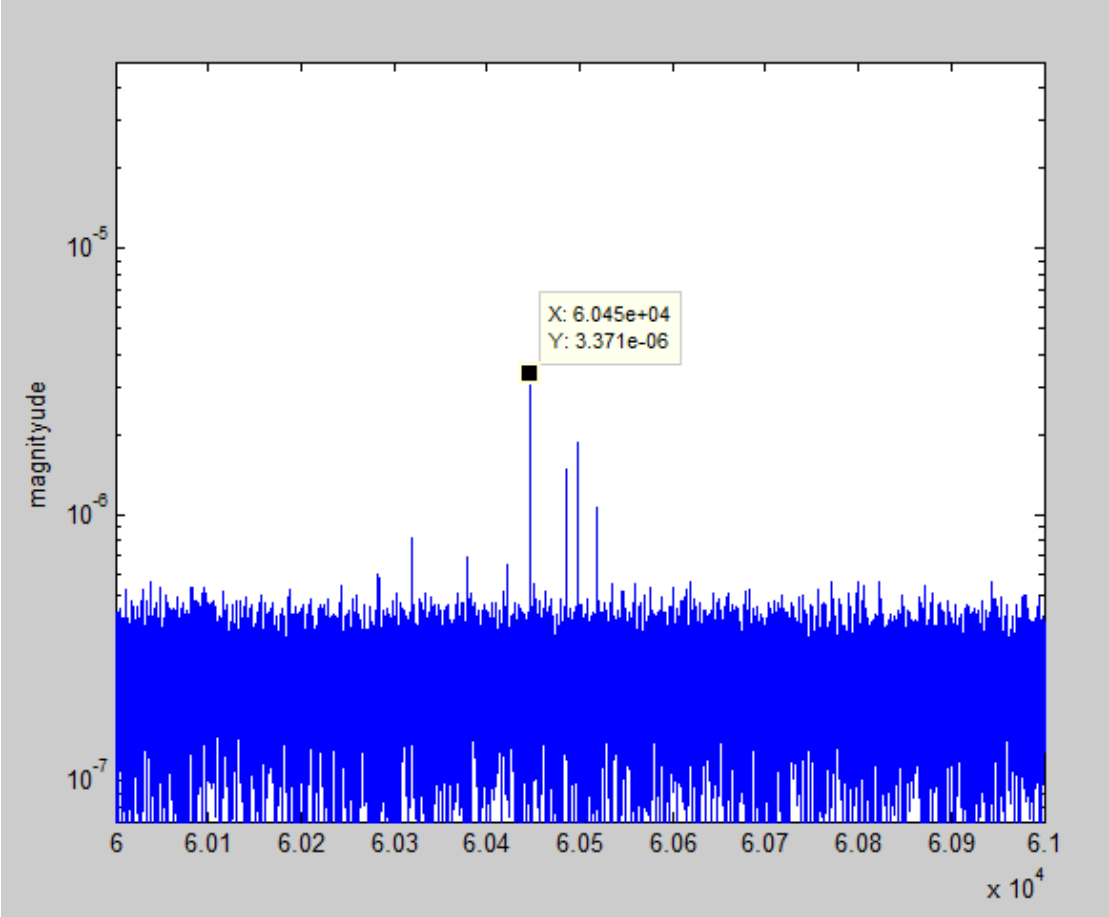

Figure 5-12 A zoom in picture on the peak.

As it can be seen in the Figure 5-11 (to see clearly Figure 5-12 is a zoom in picture) one significant peak around 60 kHz has appeared and we also measured this in the lab which is around 69 kHz, as previous mentioned just make sure the value of the resonance frequency is the same order as estimated then it is reasonable. The peak value is about 60.4 KHz, which is the same order of magnitude as the calculated one. The discrepancy can be fully attributed to the fabrication induced imperfections.

5.5 Conclusion

We measured the performance of the MRR device as a sensor, and we managed to measure its resonance frequency, which was about 60kHz . We measured the changes in output power with respect to changes in temperature via bimorph deflection mechanism. However, the sensitivity measurements where rather qualitatively as the measurement setup is not suitable for this small chip. In future

work we can change the layout of the MRR thus we can measure the performance of this novel sensor so precisely.

Reference

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Chapter 6 Conclusion

6.1 Conclusion

This thesis describes a novel displacement sensor which uses a micro ring resonator (MRR) on a micro cantilever. The key point of this thesis is how to implement the post-processing module to define the cantilever containing the MRR. The proposed device uses the working principle of MRR and by analyzing the output data, the displacement can be measured.

From Euler-Bernoulli beam theory, we defined the length and the thickness of the cantilever. Given the layout of the MRR we determined the width of the beam.

A successful fabrication processes for the integration of micro cantilever with phonic structures used for displacement sensing has been developed. The process uses contact lithography with two masks to define the cantilever. During fabrication, we found out that the photoresist is not an effective protection layer, so we changed it to PECVD silicon dioxide. This works better, however problems still remain such as a not fully etched cantilever base. This problem can be solved by changing the protection layer to another material like silicon nitride or widening the width of the mask. But as only a limited number of chips were available, no additional optimization of the process was done.

The preliminary measurements carried out prove that the idea of this novel displacement sensor is feasible. Since this sensor is made of silicon and silicon dioxide and there is no electrical circuit integrated in the chip, it can be used in harsh environments like electromagnetically active environments. Moreover, the process flow for this sensor is not complex, the cost of this sensor is expected to be low, so it can be widely used in displacement measurements.

6.2 Future work

To make the process more robust and increase the yield, an alternative protection layer like Si_3N_4, should be considered. Moreover, dry etching should be used to etch the silicon oxide, so to better control the cantilever size definition. These proposed improvements not only will better protect the MRR and waveguides during the post processing, but also save costly chip area because a smaller width can be considered. Finally, if the whole wafer is available for post-processing, additional improvement of the process and thus of the final sensor can be obtained, further benefitting of the potential this concept presents.

Appendix

Since $n_{mechanical} \propto k_B T$, we set:

$$n_1 = n_{mechanical}(T_{high}) + n_{measurement}^{high} \tag{5-8}$$

$$n_2 = n_{mechanical}(T_{low}) + n_{measurement}^{low} \tag{5-9}$$

$$T_{average} = \frac{T_{high} + T_{low}}{2} \tag{5-10}$$

Then we can get:

$$T_{average} \cdot (n_1 - n_2) = T_{average} \cdot Ck_B(T_{high} - T_{low}) - T_{average} \cdot (n_{measurement}^{high} - n_{measurement}^{low}) \tag{5-11}$$

From equation 5-11, since $n_{measurement}$ is independent of temperature and there is a small difference between $n_{measurement}^{high}$ and $n_{measurement}^{low}$, so equation 5-11 can be also written as:

$$T_{average} \cdot (n_1 - n_2) \approx T_{average} \cdot Ck_B(T_{high} - T_{low}) \tag{5-12}$$

This method enhances the temperature dependent part of the noise and suppresses the temperature independent part.