Slot Synchronization by Reducing the PPM Pulsewidth in Wireless Optical Systems

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Abstract—Digital pulse position modulation is an attractive modulation scheme in indoor wireless optical transmission systems because of its power efficiency. In this brief, slot synchronization by means of a reduced pulsewidth is discussed, the scheme is compared to on–off keying, and design rules for slot synchronizers are presented. The sensitivity deterioration of the prototype due to slot clock jitter is only 0.2 dB (optical power level).

I. INTRODUCTION

Optical infrared transmission became very popular in mobile indoor communication systems after the appropriate components, such as infrared LED’s and Si-detectors, became available in the late 1970’s [1].

In this brief, we concentrate on digital systems based on intensity modulation and direct detection. In low-power equipment, pulse position modulation (PPM) is an attractive scheme because of its power efficiency and low complexity [2]–[4]. Because the information is represented by the position of the optical pulses, the receiver has to operate synchronously, i.e., it has to know the PPM slot and frame positions. Unfortunately, many authors do not pay attention to PPM synchronization, although it is much more difficult than demodulation. As discussed in Section II, slot synchronization cannot be performed straightforwardly, since the PPM spectrum is a continuous spectrum. Reducing the width of the PPM pulses facilitates for slot clock recovery by means of a bandpass filter or a PLL [4]. This x-pulse PPM scheme is compared to on–off keying (OOK). In Section III, filter and PLL design rules are presented. To prove the feasibility and to verify the jitter calculations, the slot synchronizer was realized in a prototype receiver. We present the sensitivity measurements of this receiver in Section IV. Finally, we summarize the conclusions in Section V.

II. THE x, L-PPM MODULATION SCHEME, COMPARISON TO OOK

In a PPM modulator, an input word consisting of several bits is converted to a pulse position within a frame. The frame, with duration $T_{frame}$, is divided into $L$ slots with duration $T_{slot}$, and only one of these slots contains a rectangular optical pulse. Since $L$ possible pulse positions code for $\log_2 L$ bits of information, the bit rate follows as $R_0 = \frac{\log_2 L}{T_{frame}}$. The duration of the pulse is $T_{pulse} = x T_{slot}$ with $0 < x < 1$. The height of the pulses is $i_{avg}$, such that the average signal level is $i_{avg}$. This is an important quantity, as it determines the average power consumption, and thus the battery lifetime.

The PPM power density spectrum was calculated in [4]. If the pulse duration equals the slot duration, ($x = 1$), the resulting modulation scheme can be expressed as “full-pulse PPM.” In this case, the signal spectrum does not show any discrete frequency components at nonzero frequencies. Consequently, a slot synchronization signal cannot be derived by simply locking a PLL to the signal. If the pulse duration is smaller than the slot duration ($x < 1$), pauses appear periodically in the signal. In the spectrum this deterministic component appears as a series of $\delta$ impulses at the harmonics of the slot frequency, thereby allowing for synchronization by means of a PLL [5].

Comparing $x$, L-PPM to other transmission schemes, such as OOK, requires calculation of the bit error rate (BER) and the minimally required transmission bandwidth $B$. A reasonable estimate is $B = 1/T_{pulse} = 1/x T_{slot}$, corresponding to the first zero in the signal spectrum [6].

For adequately designed receivers, usually the main source of noise is the photodetector shot noise current caused by ambient radiation. It has a spectral density of $N_0 = q I A^2/Hz$ (double-sided), where $q$ is the electron charge and $I$ is the photodiode quiescent current due to ambient radiation. Now suppose that the demodulator is a matched filter (integrate and dump) maximum-likelihood demodulator with ideal synchronization. Then, for Gaussian noise, the BER can be calculated by extending the result that was found for full-pulse PPM in [2]. The result yields

$$\text{BER} = \frac{L}{2} Q\left(\sqrt{\frac{1}{2} L \log_2 L \frac{i_{avg}}{\sqrt{N_0 B_{slot}}}}\right)$$

in which $Q(k) = (1/\sqrt{2\pi}) \int_k^\infty \exp(-1/2 x^2) dx$.

It appears that transmitter power can be saved at the expense of additional bandwidth by reducing $x$ or, more effectively, by increasing $L$. In Fig. 1, the bandwidth and power requirements of full-pulse PPM and half-pulse PPM ($x = 1/2$) are compared to on–off keying. Halving the pulsewidth results in a 1.5-dB optical power saving, at the expense of a doubled transmission bandwidth.

III. SLOT SYNCHRONIZATION

A. Slot Synchronization by Means of a Bandpass Filter

The slot clock signal can be recovered by means of a bandpass filter, centered at the slot frequency, followed by a comparator. Essentially, both signal and noise components within the filter bandwidth $B_f$ might cause clock jitter. However, for all noise levels that are of practical interest, the former can be neglected since the signal spectrum drops to zero at frequencies close to the slot frequency and its harmonics [6].

These noise levels follow from the worst theoretical BER [see (1)] for which accurate synchronization has to be maintained. Generally,
worst-case k-values are chosen in the range 2.3–3.7, corresponding to BER’s in the order of 1E-2–1E-4. These values allow for robust systems for indoor application. The mean square jitter of the recovered clock can be calculated as
\[ \sigma_j^2 = \frac{2B_n N_0}{\left( g'(t)_{\text{max}} \right)^2} \]  
(2)
in which \( g(t) = 2i_{\text{avg}} \left( \sin(\pi x) / \pi x \right) \cos(2\pi t/T_{\text{slot}} + \phi_0) \) is the discrete frequency component at the slot frequency in the time domain and \( g'(t)_{\text{max}} \) is its maximum slope.

A detailed discussion about the maximum allowable timing error in PPM systems is beyond the scope of this brief, but from measurements and calculations it was shown that the BER hardly increases as long as the rms timing error is smaller than 10% of the pulse duration. If the noise bandwidth of the filter is denoted as \( B_n \), the required filter quality factor follows as
\[ Q = \frac{1}{B_n T_{\text{slot}}} > \frac{6.25 L^2}{k^2 \sin^2(\pi x)} \]  
(3)
An optimum occurs for \( x \approx 0.585 \), because, on the one hand, for small pulse widths the synchronization has to be very accurate, while, on the other hand, the \( \delta \) impulse at the slot frequency vanishes as the pulse duration approaches the slot duration.

In practice, \( x = 1/2 \) is a practical and close to optimum choice. For small BER’s and \( L = 4 \), it appears from (3) that reliable slot synchronization can be simply achieved by using a second-order LC filter. For \( L = 4, x = 1/2 \) and \( k = 4.74 \), corresponding to a BER of 2E-6, the feasibility was illustrated by performing jitter measurements while using an LC filter having a quality factor of \( Q = 13.9 \). The transmitter was modulated randomly. The results, measured at a bit rate of 5 kbit/s, are shown in Fig. 2. Equation (2) appears to hold well.

B. Slot Synchronization by Means of a PLL

When \( L > 4 \), synchronization by means of a PLL is more practical, since bandpass filters having large \( Q \)-factors are unpractical to build and difficult to tune. To calculate the jitter in the recovered clock, a simplified PLL model was used. First, the PPM signal at the input was replaced by a square wave with amplitude \( i_{\text{avg}} \). Provided that the PLL bandwidth is much smaller than the slot frequency, the continuous part of the spectrum can be neglected, as discussed before. Further, the noise source is shifted to inside the loop. This approximation is allowed, since the noise signal is white and uncorrelated to the input signal, so that the mixing operation does not significantly influence the noise level [7]. The mean square edge timing error of the recovered clock can be expressed as a function of either \( N_0 \) or \( k \) as
\[ \sigma_j^2 = \frac{2B_n N_0}{T_{\text{slot}} i_{\text{avg}}} B_n = \frac{L^2 T_{\text{slot}}}{8k^2} B_n, \]  
(4)
Here \( B_n \) is the noise bandwidth of the PLL.

By again requiring that the rms edge timing error is smaller than 10% of the pulse duration and by introducing an equivalent PLL quality factor, a design rule follows as
\[ Q_{\text{PLL}} = \frac{1}{B_n T_{\text{slot}}} > \frac{50 L^2}{k^2} \]  
(5)
This requirement looks much like the requirement that was found for bandpass filters.

To verify the theory, a half-pulse 4-PPM PLL synchronization circuit was built and measured using the transmitter described before. The PLL was designed for \( k = 2.83 \), corresponding to a BER of about 3E-3. Then, the equivalent PLL quality factor follows from (5). In our case, the PLL was realized with \( Q_{\text{PLL}} = 100 \), which corresponds to \( B_n = 100 \) Hz. The measurement results are shown in Fig. 3. The measured and predicted results correspond very well. No cycle slips were observed.

IV. RECEIVER SENSITIVITY MEASUREMENTS

When calculating the BER in Section II, we assumed a matched-filter maximum likelihood demodulator. A demodulator that operates according to this principle is shown in Fig. 4. The complexity is minimized by storing only the largest integration result found up to a particular moment, together with the number of the slot in which it was found. Such a system requires a feedback mechanism to control the circuit that stores the integration results [8].

Each frame starts with copying the first integration result into the track and hold (T&H) circuit, so that it can be compared to the next integration result. When the value in the I&D filter exceeds the value in the T&H circuit, it is copied into the T&H circuit, while simultaneously the slot number corresponding to that integration result is stored. Otherwise nothing happens. When the last slot of the frame has passed, the T&H circuit contains the largest integration result.
result found in the frame, and the corresponding slot number is available in the output block. This slot number is converted to a number of output bits. Meanwhile, a new frame is being received.

The circuit was realized with discrete components. The BER was measured at a bit rate of 5 kb/s. The transmitter was modulated with random bits. The results are shown in Fig. 5. For BER’s in the order of 1E-3, the measured demodulator sensitivity approaches the calculated sensitivity quite closely, while for smaller BER’s, in the order of 1E-5, a deterioration of about 0.2 dB (optical power level) occurs, due to some offset in the T&H circuit. The sensitivity deterioration due to slot clock jitter is another 0.2 dB, so that the prototype receiver approaches an ideal demodulator within about 0.4 dB.

Although the prototype operates at a speed of 5 kb/s, essentially, the bit rate can be increased. In our application, an indoor telemetry prototype receiver approaches an ideal demodulator within about 0.4 dB.

REFERENCES


High-Speed and Low-Cost Reverse Converters for the \( (2n - 1, 2n, 2n + 1) \) Moduli Set

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Abstract—In this brief, new architectures are presented for the conversion of residues to binary equivalents in the \( (2n - 1, 2n, 2n + 1) \) moduli set. Both of the architectures presented are based on a new algorithm, which eliminates a multiplication. In the design of the architectures, speed and cost are considered as the principal factors. The proposed architectures use fewer multipliers and adders of smaller size. A comparison in terms of hardware requirements, delay estimates, and complexity is made to establish the advantages of the proposed design.

Index Terms—Modular arithmetic, residue numbers, reverse converters.

I. INTRODUCTION

The moduli set \( (2^n - 1, 2^n, 2^n + 1) \) is of interest in signal-processing applications since the forward and reverse conversions can be implemented without multipliers. However, this choice is poor due to its limited applicability. To overcome this limitation, a more general moduli set of the form \( (2n - 1, 2n, 2n + 1) \) was proposed in [1]. This moduli set enables intermediate ranges to be used which would otherwise require a higher index if the \( 2^n \) moduli set were used. The reverse conversion technique proposed in [1] for the \( (2n - 1, 2n, 2n + 1) \) moduli set shows reduced internal structure due to lower internal dynamic range. Although the final modulo \( M \) operation has been simplified, \( M \) is still large and requires large adders.

II. SIMPLIFIED ARCHITECTURES FOR REVERSE CONVERSION IN THE \( 2n \) MODULI SET

Generally, conversion from residue to binary in the moduli set \( 2^n \) is based on the properties of the moduli set and, hence, the hardware proposed is simple and uses only adders [2]–[7]. Although the reverse conversion for the \( 2^n \) set proposed in [1] is not based on the Chinese remainder theorem, it is complex and uses three multipliers, simply because this moduli set does not possess properties that are amenable to easy hardware implementation. In this brief, alternative architectures are proposed which use fewer multipliers of smaller size compared to those used in [1]. Cost-effective and high-speed versions of the converter are presented here. The cost-effective version is a low-complexity design which uses less area and power when implemented in VLSI. The high-speed version achieves a speed improvement of 50% compared to the low-cost version, and 33% compared to the suggested architecture in [1].

The formula for reverse conversion proposed in [1] is as follows for the sake of completeness:

\[
X = \left( \frac{(m_1 + 1)m_2m_3}{2} x_1 + m_1(m_2 - 1)m_3 x_2 + \frac{m_1m_2(m_3 + 1)}{2} x_3 \right)_{M}^{10} \quad (1)
\]

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