SPICE Modeling of Single-Grain Si TFTs using BSIMSOI

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Single Grain Thin-film transistors (SG-TFTs) fabricated inside a location-controlled grain by µ-Czochralski process have as high as SOI performance. To model them, BSIMSOI with a proper modification of the mobility is proposed. The model has been verified for n- and p-channel DC and low frequency AC conditions by comparison with measurement results. Furthermore, preliminary circuit simulations are executed.

Introduction

Single Grain Thin-Film Transistors (SG-TFTs) fabricated inside a location-controlled grain by µ-Czochralski technology using an excimer laser have reached Silicon-on-Insulator (SOI) performance despite low temperature fabrication (< 350 °C) process (1)-(3). Digital circuits as well as analog and RF circuits could be integrated with display or into vertical direction for applications of Flexible-Electronics or 3D ICs, respectively. Challenges now are to design and to fabricate those circuits by using this technology. To achieve these goals a proper model for circuit simulations is of a crucial importance. Polysilicon TFT models (4)-(7) cannot be employed because they are based on classical long-channel formulation and cannot capture the characteristics of near-submicron TFTs necessary to realize analog and RF circuits; above all, these models use a mobility model that only takes into account the thermionic emission effect across random grain boundary. The SG-TFT channel, on the other hand, consists of one of few silicon crystals and few Coincident Site Lattice Grain Boundaries (CSL-GBs) in between, which have much lower electronic activity than random grain boundary (8). As a consequence, a model that explicitly takes into account of silicon crystals and CSL-GBs has to be developed. A model of large grain polysilicon has been performed (9) but it is based on the classical long-channel formulation.

In this work, on the other hand, a modeling based on BSIMSOI developed by University of California Berkeley (10) is proposed. BSIMSOI is a physically based on SOI model and has been used by many industries for circuit simulation of advanced SOI process. Due to the similarity between SG-TFTs and SOI MOSFETs, lots of the physical effects such as self-heating effect, floating body effect are common to both. BSIMSOI also includes good short channel effects and fully-depletion model important for scaling viewpoint. Furthermore, the model extensively uses smoothing functions, which guarantees continuous and smooth behavior of the model description across all regions of device operation. That ensures the model is robust and efficient when implemented in a SPICE simulator. However, modification of BSIMSOI mobility model is indispensable in order to be adapted to SG-TFTs describing the effect of CSL-GBs present in the channel. This modification is introduced by smoothing function still guaranteeing continuous and smooth behavior of equations across of regions.
Model Formulation

It has been known that in the SG-TFTs fabricated inside a location-controlled grain by \( \mu \)-Czochralski process the channel possesses the CSL-GBs. It was suggested that some of these boundaries are electrically active, although the degree is much lower than that of the random grain boundaries in the polysilicon (8). The motion of carriers across GBs is well known to be described by thermionic emission effect (6)-(7). The thermionic emission effect has to be taken into account in the BSIMSOI mobility model and that is carried out by a semi-empirical model, which introduces some fitting parameters in the physically based model.

Considering a number of CSL-GBs and silicon crystals within the channel, according to the standard MOSFET theory corresponding to the on-current condition, and following the same procedure of (9), the channel resistance \( R_{ch} \) will be:

\[
R_{ch} = nR_G + nR_{GB} = \frac{L}{W \mu_{eff} Q_{invG}} = \frac{nL_G}{W \mu_G Q_{invG}} + \frac{nL_{GB}}{W \mu_{GB} Q_{invGB}}
\]  

where \( L \) and \( W \) is channel length and width, respectively, \( L_G \) average intra-grain length, \( L_{GB} \) average CSL-GB length, \( \mu_{eff} \) effective carrier mobility in the SG-TFT channel, \( \mu_G \) is the mobility in the silicon crystal and \( \mu_{GB} \) is the mobility in the CSL-GB, \( Q_{invG} \) is charge in the inversion layer referred to the silicon crystal, and \( Q_{invGB} \) is the one referred to the CSL-GB. It is related to the one in the grain by thermionic emission effect (7):

\[
Q_{invGB} = \exp(-qV_b/kT)Q_{invG}
\]

Therefore, we can obtain the following relation:

\[
\frac{L}{\mu_{eff}} = \frac{L - nL_{GB}}{\mu_G} + \frac{nL_{GB}}{\mu_{GB} \exp(-qV_b(V_{Gate}/kT))}
\]

That can be rewrite as following:

\[
\frac{1}{\mu_{eff}} = \frac{1 - \alpha}{\mu_G} + \frac{\alpha}{\mu_B}
\]

with \( \alpha = nL_{GB}/L \). \( \mu_G \) is the mobility expressed in the BSIMSOI and it comes down from universal mobility model and depends on gate voltage as following (10):

\[
\mu_G = \frac{\mu_0}{1 + U_a \left( \frac{V_{gs eff} + 2V_{th}}{T_{ox}} \right) + U_b \left( \frac{V_{gs eff} + 2V_{th}}{T_{ox}} \right)^2}
\]

where \( \mu_0 \) is the zero-field carrier mobility in silicon (equal to 670 cm\(^2\)/Vs for NMOS and 250 cm\(^2\)/Vs for PMOS), \( U_a \) and \( U_b \) the fitting parameters used to model the amount of
degradation due to the average normal electric field, \( V_{th} \) the threshold voltage, \( V_{g_{\text{eff}}} \) the smoothing functions that approaches to \( V_{gr} - V_{th} \) and \( T_{ox} \) the gate oxide thickness. \( \mu_B \) is the typical thermionic emission relation:

\[
\mu_B = \frac{\mu_{GB}}{\exp\left(\frac{q V_b}{kT}\right)}
\]  

\( V_b \) is the potential barrier height, which depends on the gate voltage (7). For simplicity, the potential barrier height is described by an empirical equation that utilizes the \( V_{g_{\text{eff}}} \) smooth function as following:

\[
V_b = \frac{V_{\max}}{1 + \vartheta V_{g_{\text{eff}}}}
\]  

where \( V_{\max} \) is the maximum potential barrier height. \( \vartheta \) is a fitting parameter that describes grain boundary potential lowering when gate potential increases. The \( \alpha \) describes the quantity of CSL-GBs in the channel and unifies polysilicon and SOI models. It becomes zero when no CSL-GBs are in the channel and the model approaches to the basic BSIMSOI. It can only be used as fitting parameter because the number of CSL-GBs cannot be known.

**Simulation Results**

After including the changes described above to the existing BSIMSOI model by using Verilog-A implemented in ADS simulator (following the approach of (11)), DC and low frequency Capacitance-Voltage (CV) characteristics are simulated and compared to measurement results. In order to extract the parameters, optimization algorithm is used. Figures 1 and 2 show measurement and simulation results of transfer characteristics and output characteristics, respectively, of n- and p-channel SG-TFTs with 5 \( \mu \)m channel length and width. As shown in figures, a good agreement between measurements and model is obtained.

![Figure 1. Transfer characteristics of n- (left) and p-channel (right) SG-TFTs with W = 5 \( \mu \)m and L = 5 \( \mu \)m for drain voltages from 0.05 V to 5 V and -0.05 V to -5 V, respectively.](image)
Figure 2. Output characteristics of n- (left) and p-channel (right) SG-TFTs with $W = 5 \mu m$ and $L = 5 \mu m$ for gate voltages from 0 V to 6 V and -2 V to -8 V, respectively.

Figures 3 show an agreement between measurement and simulation results of transconductance characteristics of n- and p-channel SG-TFTs. Furthermore, left-side of fig. 3 shows measurements by using different energy densities of excimer laser (LE) during the silicon crystallization. These measurement results show transconductance increase when laser energy is higher due to reduction of CSL-GBs in the channel. This effect is well modeled by only reducing $\alpha$ parameter from 0.8 down to 0.25, whereas the rest of parameters are fixed.

Figure 3. Transconductance characteristics of n-channel with different laser energy (left) and p-channel (right) SG-TFTs with $W = 5 \mu m$ and $L = 5 \mu m$ for drain voltages of 0.05 and -0.05 V, respectively.

Fig. 4 shows agreement between measurement and simulation results of low frequency (1MHz) capacitance-voltage (CV) characteristics between gate and drain-source connected together of 300 SG-TFTs with 5.5 $\mu m$ channel length and width connected in parallel.
Figure 4. CV simulation and measurement of 300 SG-TFTs with \( W = 5.5 \, \mu m \) and \( L = 5.5 \, \mu m \) connected in parallel.

**Circuit Simulations**

Preliminary analog circuit simulations are carried out using BSIMSOI with aforementioned modification. In the simulation, threshold voltages of \( V_{thn} = 0.5 \, V \) for n-channel, \( V_{thp} = -2.5 \, V \) for p-channel and \( \alpha = 0.25 \) for both, with statistical variations of \( \pm 20\% \) are considered. Figure 5 shows simulation results of a NMOS voltage reference circuit with a resistive feedback. As results, 0.7V reference voltage with 15% of statistical variation is predicted. Figures 6, on the other hand, show a two-stage operational amplifier. The simulation results illustrate that the gain is around 25 dB and it is not much statistically varying (< 4%), while the bandwidth has a more statistical variation (~ 23%).

Figure 5. NMOS voltage reference with a resistive feedback (left) and simulation results (right).

Figure 6. Two-stage operational amplifier (left) and simulation results (right).
Conclusion

SPICE modeling of SG-TFTs fabricated inside a location-controlled grain by μ-Czochralski process has been developed. The model employs most of the essential MOS physics from BSIMSOI with an essential modification in order to take the CSL-GBs in the channel into account. The validity of the proposed model has been demonstrated by a good agreement with DC and AC measurement results. Furthermore, preliminary analog circuit simulations are shown.

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References

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