Variable output voltage DC-DC converter with adjustable inductor current for neurostimulators

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November 13, 2012
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by

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A thesis submitted to the Department of Microelectronics, Faculty of Electrical Engineering, Mathematics and Computer Science Delft University of Technology, in partial fulfillment of the requirements for the Degree of

MASTER OF SCIENCE

in Microelectronics

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November 2012
For neural cell stimulation there is a need of a high supply voltage up to 18V. However because the stimulation is not every time the same, sometimes there is only a need for lower supply voltage. The supply voltage should be variable so that loss of energy due to the wasted supply voltage headroom is minimized.

In order to be able to cover this stimulation voltage range the converter needs to convert the 3.3V battery voltage up to a variable output voltage with a maximum voltage of 18V. This needs to be done with a power efficiency of at least 80%. Also the converter must not be sensitive to input/output variations and temperature changes.

In this work the boost converter topology is selected and is designed with a new current sensing technique. Also the controller circuit is designed so that the converter works always in the discontinuous current mode. For this controller circuit an efficient capacitor based voltage measurement circuit is designed. Everything is designed at transistor level to be implemented in the 0.35μm High Voltage I3T25 technology of On Semiconductor. The working principle is illustrated with circuit simulations.
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1 Introduction

In [24] a neural stimulator is designed in the i3t25 technology[24]. This stimulator needs a voltage up to 18V DC for the stimulation of the neural cells. A typical battery for biomedical applications has a voltage of 3-4V DC. The higher voltage can be generated by placing battery cells in series but this takes a lot of area. Thus a better solution is to use a DC-DC converter. A DC-DC converter converts one DC voltage into another DC voltage. DC-DC converters are most of the time part of the power management units that are usually integrated on-chip. In case of the stimulator, there are different sections that require different voltages: a higher voltage to stimulate the tissue and a low voltage is used for the other electronics to reduce the power consumption. The high voltage used for the stimulation must be variable to keep the energy consumption low when the stimulator stimulates at a lower voltage. This can be done by converting to a high voltage first. Then the voltage can lowered again (for example with a low dropout regulator), but this is highly inefficient. That is the reason that this conversion can be better done using a switched DC-DC converter with a high efficiency. This will be explained more in detail in Chapter 2.

The stimulator power supply will be a single battery. Voltage of the battery is likely to vary because: this battery can be used to power many modules and they can turn on-off independently, which leads to changes in the battery voltage seen by the other modules. The voltage of the battery can also vary over time due to the discharge of the battery, and the ageing of the battery. Therefore, apart from the efficiency, the converter must be able to convert a great range of input voltages to a stable output supply voltage.

Furthermore the response of the converter to the variations in the load current or the changes in the battery voltage, generally referred to as load and line transient responses respectively, should be fast enough to avoid fluctuations in the output voltage. This requires some form of feedback from the output voltage and therefore leads to stability considerations as well. The circuit techniques employed for stability should not add excessive area and power overhead.

With very small transistor sizes in CMOS technologies device stress should also be taken into consideration. The circuit techniques and topologies used should ensure a reliable operation over a long life-time of the device. Apart from protecting the internal circuits of the IC, these converters should also be able to tolerate the voltage stresses themselves. Hence the critical requirements on the DC-DC converters can be outlined as:

- A variable constant output voltage from 3.3V to 18V DC: to stimulate at different voltages in an efficient way.
- Convert different input voltages (from 1.8 to 3.3V DC) to a stable output voltage.
variations in the input voltage must not lead to variations in the output voltage.

- A power efficiency above the 80%: When the system uses less power the energy source can be smaller. This means that the system can work with a smaller battery. In this way the system size decreases. A high efficiency of the system results also in a longer life time of the stimulator on a particular battery.

- Less power consumption results also in less heat generation due to power dissipation in the system. This is important since temperature changes of a few degrees are destructive for neural cells.

- Not more than two off-chip components. Reliability is a very important condition because it is implanted in the head of the human body. Off chip connections are not as reliable as silicon connections.

- Fast response to changes in the input voltage and the output load current. (This is because by stimulation the current is switching suddenly on and off). This is required to ensure the stable output voltage.

- Minimum area: the whole stimulator must implanted in the head of a human body.

For the loading current we will consider to the stimulation cycle of the stimulator as shown in Fig 2.1, since the DC-DC converter will be the power source of this cycle. A stimulation cycle is as follows: during 100 μs a current pulse is sent to the electrodes with an amplitude between 1mA and 20mA. After this 100 μs pulse the same pulse is repeated for 100 μs, on the electrode but now inverted.

Then the stimulator is switched off for 1ms and then the cycle is repeated. Thus the converter needs to handle a load current of 1mA up to 20mA for 200 μs.

![Figure 1.1: Current stimulation cycle.](image)

The difference between various types of converters will be covered in detail in Chapter 2. After the explanation of the different converters one type of conversion is chosen for the converter. In Chapter 3 the chosen converter is designed at system level. Also the feedback circuit is designed in this chapter. In Chapter 4 the system blocks are implemented at transistor level and the challenges that are encountered by implementing at transistor level are solved. In Chapter 5 the circuit is simulated to prove the correct functionality and the performance of the circuit is analyzed. In the last chapter the conclusions and recommendations for further research are presented.
2 DC-DC converters

Several methods exist to achieve DC-DC voltage conversion. Each of these methods has its specific benefits and disadvantages, depending on a number of operating conditions and specifications. Examples of such specifications are the voltage conversion ratio range, the maximal output power, power conversion efficiency, number of components, dimensions of the converter, etc. When designing fully-integrated DC-DC converters these specifications generally remain relevant, nevertheless some of them will gain weight, as more restrictions emerge. For instance the used IC technology limiting the availability and quality factor of the passive components and the available chip area will be dominant for the production cost. These limitations will in turn have a significant impact on the choice of the conversion method. The simplest method of performing DC-DC voltage conversion is by means of linear voltage converters, which are explained in Sect. 2.1. The second and third method are switched mode converters, either using capacitor charge-pumps, or inductive type DC-DC converters. We will first look to the fundamental difference between the inductor and capacitor based converters in Section 2.2. After that we will look into practical converters in Section 2.3 and 2.4. And at the end we will choice between the different converters in section 2.5.

2.1 Linear regulators

A simplified block diagram of a linear regulator is shown in Fig 2.1. The regulator uses an error amplifier to compare the output voltage to a reference voltage. The amplifier then generates a control signal proportional to the error between the desired and actual output voltages. This control signal drives a pass transistor at some point between saturation and cutoff so that the correct amount of supply current is supplied to the load to keep the output voltage at the correct value.

![Block diagram of a linear series voltage regulator.](image)

Figure 2.1: Block diagram of a linear series voltage regulator.

One advantage of using linear regulators is that they are simpler to design than the
switching mode converters and they don’t have switching effects due to the continuous regulation of the output. However these regulators suffer from a high energy loss at high load currents and when the difference between the regulated and the unregulated voltage is high the efficiency is low. This can be explained by the fact that the current in the circuit is the same though the variable resistance and the load and thus the efficiency $\eta$ for the linear regulators is estimated as

$$\eta = \frac{V_o}{V_i} \quad (2.1)$$

Here $V_o$ is the output voltage and $V_i$ is the input voltage. Now, consider converting 18 V to 6 V using a linear regulator and from equation (2.1), we can estimate the efficiency as 33 %. This is when all the components are still ideal. Another drawback of the linear regulator is that they can only down convert the voltage. That’s the reason that generally the linear regulators not chosen for a DC-DC converter. Most of time the designer will chose a switching regulator. We will discuss the switching regulator in the next section.

### 2.2 Switching regulators

An energy source delivers energy with a constant voltage (voltage source) or a constant current (current source). When a higher voltage is needed the energy must first be stored in a energy storage element from the energy source. Then when the energy storage element is switched in series with the energy source the voltage over the two elements will be higher. When we now store the energy with the higher voltage in a other energy storage element we can deliver energy to a load with a higher voltage. We can make the schematic like in fig.2.2a) for storing the energy in the energy storage element. In fig. 2.2b) we see the schematic for getting the energy out of the storage element into another storage element with a different voltage.

![Figure 2.2: Energy conversion Block diagram](image)

For the energy source we use two different energy sources types: a current source and a voltage source. For the energy storage elements we have two elements: an inductor and a capacitor. We can make four different combinations for the schematic in figure 2.2(a) with the two sources and the two energy storage elements. In the next paragraph there will be more explanation about the different combinations.

The battery that is used for the stimulator behaves already as a voltage source and we don’t have to let it behaves like a voltage source. But because the battery doesn’t behaves
like a current source we must manipulate the voltage source so that it behaves like a current source.

This leads that the voltage compliance of the current source is limit by the voltage of the voltage source. The extra energy loss by the manipulated voltage source is when the voltage that is needed to let the current flow is lower than the voltage source because we always lose the voltage that we not use times the current.

The difference between the inductor and the capacitor is that the inductor stores the energy in the magnetic field. The capacitor store the energy in the electrostatic field. The other difference is that the current through the inductor can’t change instantaneously and by the capacitor is it the voltage that can’t change instantaneously. Thus for the last energy storage element in figure 2.2(b) we use a capacitor because we want to store a voltage at the output. In the next sections we look to the fundamental losses of the different circuits.

### 2.2.1 Capacitive Energy storage element

#### 2.2.1.1 Charge Capacitor with voltage source

The principle of a gradual change of energy in an electrical circuit, means that the energy stored in electric or magnetic fields cannot change instantaneously [10, 9, 16]. For simple analysis, the assumption is made in transient analysis that the switching occurs quite instantaneously [20, 11]. Let \( t = 0 \) be the instant of time when switching starts, and two additional instants: just prior and just after switching be \( t = 0^- \) and \( t = 0^+ \) respectively. In mathematical language, the value of the function \( f(0^-) \) is the "limit from the left", as \( t \) approaches zero from the left, while \( f(0^+) \) is the "limit from the right", as \( t \) approaches zero from the right. According to the above principle, the voltage \((V)\) (charge \((q)\)) of a capacitor just after switching is equal to the voltage (charge) just prior to switching:

\[
V_{C1}(0^+) = V_{C1}(0^-)
\]  \hspace{1cm} (2.2)

\[
q(0^+) = q(0^-)
\]  \hspace{1cm} (2.3)

We implement the ideal switch as a device that switched on and off in zero time and with zero-resistance, we consider the charging circuit shown in Fig. 2.3(a), where the voltage source \( V_s \), the switch \( S_1 \) and the capacitor \( C_1 \) are ideal. When \( S_1 \) is turned-on, the voltage \( V_{C1} \) over the capacitor changes abruptly from zero to \( V_s \). In other words, the charging of \( C_1 \) is done by an infinitely high current pulse during an infinitely Small time. Using the above assumptions, we can write \( V_{C1}(0^-) = 0 \), \( V_{C1}(0^+) = V_s \) and \( V_{C1}(0^-) \neq V_{C1}(0^+) \) which contradicts equation 2.2. This contradiction can be overcome since any circuit with a real capacitor with switch and voltage source has in practice some resistance connected in series. The infinite current spike is now prevented in the switched circuits shown in Fig. 2.4, so that the initial conditions are correct. Note that such circuits may be composed by taking into consideration just the resistances of the switch. The charging circuit with the resistor is shown in Fig. 2.4(a). It is described by a first order differential equation because it comprises only one capacitor \( C_1 \). So, the aim
Figure 2.3: Ideal capacitor charge circuit (a) with a fixed voltage. (b) with another capacitor.

Figure 2.4: Capacitor charge circuit included a series resistance (a) with a fixed voltage. (b) with another capacitor.

is to calculate the response of the first order circuit to the voltage step $V_i$. According to Kirchhoff’s Current Law $i_s(t) = IC_1(t)$, this is:

$$\frac{V_i - V_{C1}(t)}{R} = C_1 \frac{dV_{C1}(t)}{dt} \quad (2.4)$$

Rearranging the above equation:

$$\frac{dV_{C1}(t)}{V_{C1}(t) - V_i} = -\frac{1}{RC_1} dt \quad (2.5)$$

Now it can be simply integrated:

$$\int \frac{dV_{C1}(t)}{V_{C1}(t) - V_i} = -\frac{1}{RC_1} \int dt \quad (2.6)$$

Integration of both sides yields with the integration constant $D$:

$$ln[V_{C1}(t) - V_i] = -\frac{t}{RC_1} + D \quad (2.7)$$

Since the time constant $\tau = RC_1$,

$$V_{C1}(t) = V_i = e^{\frac{t}{\tau}} + D \quad (2.8)$$

An initial ($t=0$) voltage across $C1$ will be

$$V_{C1}(0) = V_i = e^D + V_i \quad (2.9)$$
So, the complete response is:

\[ V_{C1}(t) = V_0 e^{-\frac{t}{\tau}} + V_i \left( 1 - e^{-\frac{t}{\tau}} \right) \]  \hspace{1cm} (2.10)

The complete response was calculated in Maple and is presented in Fig. 2.5 together with the voltage across the resistance \( V_R = V_i - V_{C1} \). The current in the circuit is limited by \( I_0 = \frac{(V_i - V_0)}{R} \) and at the end of one \( \tau \) interval, the voltage over the capacitor is \( 1 - e^{-1} \approx 0.632 \) of its initial value, while at the end of \( 5\tau \) the voltage ratio is less than 0.01. Because of this fact, it is common to assume that the duration of the transient response is about \( 5\tau \); but note that, strictly speaking, the transient response declines to zero in infinite time, since \( e^{-t} \rightarrow 0 \), when \( t \rightarrow \infty \). When we look to the efficiency of the

![Graph](image)

Figure 2.5: Complete response of the charging circuit and its components with \( V_s = 1V \).

energy transfer to the capacitor with the initial voltage \( V_0 = 0V \). As known, the energy stored in the capacitor is:

\[ E = \frac{CV^2}{2} \]  \hspace{1cm} (2.11)

So substitute eqn.(2.10) into eqn.(2.11) for this case leads to:

\[ E_o = \frac{C_1V_{C1}(t)^2}{2} = \frac{C_1 \left( \frac{V_i \left( 1 - e^{-\frac{t}{\tau}} \right)}{2} \right)^2}{2} = \frac{C_1V_i^2 \left( 1 - e^{-\frac{t}{\tau}} \right)^2}{2} \]  \hspace{1cm} (2.12)

The loss in the resistor is:

\[ E_{Loss} = \int_0^{t_1} i(t)^2Rdt = \frac{C_1V_i^2 \left( 1 - e^{-\frac{2t_1}{\tau}} \right)}{2} \]  \hspace{1cm} (2.13)
So the efficiency is the transferred energy divided by the total energy:

$$\eta = \frac{E_\alpha}{E_\alpha + E_{\text{Loss}}} = \frac{(1 - e^{-\frac{t}{\tau}})^2}{(1 - e^{-\frac{t}{\tau}})^2 + (1 - e^{-\frac{2t}{\tau}})} = \frac{1}{2} \left(1 - e^{-\frac{t}{\tau}}\right) \quad (2.14)$$

this is plotted in Fig. 2.6. We can see that the highest efficiency of charging the capacitor is 50% and independent of the resistance and capacitance of the circuit. This fact is investigated in more detail.

![Efficiency plot C charge with voltage source](image)

Figure 2.6: Efficiency plot C charge with voltage source

When \( t \gg 5\tau \), the voltage \( V_{C1}(t) \) is considered to be equal to the source voltage \( V_{C1}(0+) = V_i \). The amount of charge transferred by an exponentially decreasing current is equal to the product of its initial value and the time constant.

$$q = \int_0^\infty i(t)dt = I_0 \int_0^\infty e^{-\frac{t}{\tau}}dt = -\tau I_0 (-t)e^{-\frac{t}{\tau}} \bigg|_0^\infty = I_0 \tau \quad (2.15)$$

And when substitute the \( I_0 \) and \( \tau \) in eqn.(2.15) the charge is:

$$q = I_0 \tau = \left(\frac{V_i - V_0}{R}\right)RC_1 = (V_i - V_0)C_1 \quad (2.16)$$

The very large magnitude of the current pulse is represent by the impulse function \( \delta \) applied for a very short (approaching zero) time interval, but as seen in formula 2.16 their product stays finite, as shown in Fig. 2.7. The charge in the circuit is only dependent of the voltage difference and the capacitance \( C \) in the circuit. But the time that it takes to fully charge the capacitor depends on the resistance \( R \).
Figure 2.7: Response of $i(t)$ by charging a capacitor over a resistance and an equivalent impulse.

For analyze the efficiency for the case when the capacitor is precharged consider again the charging circuit in Fig. 2.4 (b), but where the ideal capacitor $C_1$ is now pre-charged to the voltage $V_0$ and holds an initial energy $E_0 = \frac{C_1(V_0)^2}{2}$. After $C_1$ is charged instantaneously to $V_f$ the final energy in the capacitor $E_1 = \frac{C_1V_f^2}{2}$. The transferred energy to the capacitor is then:

$$E_{trans} = E_1 - E_0 = \frac{C_1(V_f)^2}{2} - \frac{C_1(V_0)^2}{2} = \frac{C_1(V_f^2 - V_0^2)}{2} \quad (2.17)$$

The energy is dissipated as heat when the capacitor $C_1$ is charging through the resistor $R$ as shown in Fig. 2.4(a). The power is $P = I^2R$ and its integrated value is the energy dissipated:

$$E_{Loss} = E_h = I_0^\infty t \int_0^\infty (e^{-\frac{t}{\tau}})^2 dt = \frac{(\Delta V)^2}{2R} \tau = \frac{C_1(\Delta V)^2}{2} \quad (2.18)$$

This leads to the following efficiency:

$$\eta = \frac{E_{trans}}{E_{trans} + E_{Loss}} = \frac{V_f^2 - V_0^2}{V_f^2 - V_0^2 + (V_f - V_0)^2} = 1 - \frac{V_0 + V_f}{V_f} \quad (2.19)$$

We can see that when the capacitor is not pre-charged there is always a loss of 50% of the energy no matter what the resistance or capacitor are. But the charging time to fully charge the capacitor is changing with different values for the resistance and capacitance. We can also see that when we pre-charge the capacitor we can get a high efficiency. In the next section we are looking what the losses are when we charge the capacitor with a current source.

2.2.1.2 Charge Capacitor with current source

In the previous section we have charged the capacitor with a voltage source and we saw that we always lose fifty percent of the energy. Thus in this section we investigate if that is also the case when we charge the capacitor with a current source. The charging circuit with a current source and the nonideal switch is shown in Fig. 2.8. It is described by a
Figure 2.8: Capacitor charge circuit included a parallel resistance with a fixed current.

A first order differential equation because it comprises only one capacitor C1. The aim is to calculate the complete response of the first order circuit to the current step $I_s$ thus by opening the switch. According to Kirchhoff’s Current Law $I_s(t) - I_R(t) = I_{C1}(t)$ and Kirchhoff’s voltage Law $V_R = V_{C1}$ this is:

\[ I_s - \frac{V_{C1}}{R} = C_1 \frac{dV_{C1}(t)}{dt} \]  

(2.20)

Rearranging the above equation:

\[ \frac{dV_{C1}(t)}{V_{C1}(t) - I_s R} = -\frac{1}{RC_1} dt \]  

(2.21)

Now it can be simply integrated:

\[ \int \frac{dV_{C1}(t)}{V_{C1}(t) - I_s R} = -\frac{1}{RC_1} \int dt \]  

(2.22)

The integration of both sides yields with the integration constant $D$:

\[ \ln [V_{C1}(t) - I_s R] = -\frac{1}{RC_1} t + D \]  

(2.23)

Rearranging the above equation with $\tau = \frac{1}{RC_1}$:

\[ V_{C1}(t) - I_s R = e^{-(D + \frac{t}{\tau})} \]  

(2.24)

The initial voltage over C1 will be

\[ V_{C1}(0) = V_0 = I_s R + e^{-D} \]  

(2.25)

So, the complete response is:

\[ V_{C1}(t) = V_0 e^{-\frac{t}{\tau}} + I_s R \left(1 - e^{-\frac{t}{\tau}}\right) \]  

(2.26)

The current through the resistance $I_R = \frac{V_{C1}}{R}$ was calculated in Maple and is presented in Fig. 2.13 together with the current into the capacitor $I_{C1} = I_s - I_R$. We can see in this plot that at the beginning the whole supply current flows to the capacitor. And at the end of the response the whole supply current is flowing to the resistance. This is exactly the opposite of the capacitor being charged with the voltage source.
Figure 2.9: $V_C$ with constant current source $I_S=1A$.

Now we look into the energy transfer to the capacitor and energy loss in the resistor. The total energy in the capacitor while charging is:

$$E_C = \frac{CV_1^2(t)}{2}$$  \hspace{1cm} (2.27)

And the transferred energy to the capacitor is the total energy minus the initial energy:

$$E_C - E_0 = E_{\text{trans}} = \frac{C_1V_1^2(t)}{2} - \frac{CV_0^2}{2}$$  \hspace{1cm} (2.28)

The energy delivered by the source can be calculated by taking the integral of the delivered power:

$$E_d = I_s \int_0^t V_C dt$$  \hspace{1cm} (2.29)

And the efficiency is then:

$$\eta = \frac{E_{\text{trans}}}{E_d}$$  \hspace{1cm} (2.30)

This is calculated with Maple and plotted in Fig.2.10. We see in this figure that the efficiency is decreasing over time. We can see in the plot that the efficiency of the transferred energy begins by 100% and when we store more energy in the capacitor the efficiency drops. When we compare this to the voltage source then is this the opposite because the transferred energy starts with a efficiency of 0%. And when the capacitor is fully charged the efficiency is 50%. This can be explained by the fact that at beginning of switching there are fast changes in the transient signal and thus there are high frequencies.
in the signal at the moment of switching. For high frequencies the impedance of the capacitor is zero. By the charging capacitor with a voltage source the resistor is in series with the capacitor and thus the whole voltage standing over the resistor. By charging with the current source the resistor is in parallel with the capacitor and thus the whole source current flow to the capacitor.

This looks good but as earlier explained we don’t have a ideal current source and thus we lose energy by the conversion from a voltage source to a current source. This is due to the fact that for an ideal current source the voltage over the source is variable but by the conversion of a voltage source to the current source the voltage is constant thus the power delivered by the source is the current times the constant supply voltage. And the energy delivered by the source can be calculated by taking the integral of the delivered power:

$$ E_d = \int_0^t V_i I_a(t) dt $$

(2.31)

So the efficiency of the energy transfer is

$$ \eta = \frac{E_{trans}}{E_d} $$

(2.32)

So in the case when we not pre-charge the capacitance the efficiency is:

$$ \eta = \frac{E_{trans}}{E_d} = \frac{I_a R^2}{V_i t} \left(1 - e^{-\frac{t}{\tau}}\right) $$

(2.33)

This is calculated with maple and plotted in Fig.2.11 We can see in the plot that the efficiency of the transferred energy grows not higher than 20% When we compare this
to the capacitor charged with the voltage source we see that this is lower. Thus we see when we will charge a capacitor that is not precharged we always lose minimal 50% of the energy. In the next section will find that is the same when we look to charging the inductor.

2.2.2 Inductive Energy Storage element

2.2.2.1 Charge Inductor with a voltage source

![Inductor charge circuit](image)

Figure 2.12: Inductor charge circuit included a serie resistance with a fixed voltage.

The charging circuit for the inductor with the non ideal switch is shown in Fig. 2.12. It is described by a first order differential equation because it comprises only one inductor \( L_1 \). So, the aim is to calculate the complete response of the first order circuit to the voltage step \( V_i \). According to Kirchhoff’s voltage Law \( V_i - V_R = V_{L1}(t) \), this is:

\[
V_i - i_L(t)R = L_1 \frac{di_{L1}(t)}{dt}
\]

(2.34)
Rearranging the above equation:

\[
\frac{di_L(t)}{i_L(t) - \frac{V_i}{R}} = -\frac{R}{L_1} dt
\]  
(2.35)

Now it can be simply integrated:

\[
\int \frac{di_L(t)}{i_L(t) - \frac{V_i}{R}} = -\frac{R}{L_1} \int dt
\]  
(2.36)

The integration of both sides yields with the integration constant \(D\):

\[
\ln \left[ i_L(t) - \frac{V_i}{R} \right] = -\frac{R}{L_1} t + D
\]  
(2.37)

Rearranging the above equation with \(\tau = \frac{L_1}{R}\):

\[
i_L(t) - \frac{V_i}{R} = e^{-(D + \frac{t}{\tau})}
\]  
(2.38)

An initial current through \(L_1\) will be

\[
i_L(0) = I_0 = \frac{V_i}{R} + e^{-D}
\]  
(2.39)

So, the complete response is:

\[
i_L(t) = I_0 e^{-\frac{t}{\tau}} + \frac{V_i}{R} \left(1 - e^{-\frac{t}{\tau}}\right)
\]  
(2.40)

The voltage over the resistance \(V_R = I_{L_1} R\) was calculated in Maple and is presented in Fig. 2.13 together with the voltage over the inductor \(V_{L_1} = V_s - V_R\). We can see in this plot that at the beginning the whole supply voltage is standing over the inductor. And at the end of the response the whole supply voltage is standing over the resistance. This is exact the opposite of the capacitor charged with the voltage source.

Now we will look to the efficiency of the energy transfer. As known, the energy stored in the inductor is:

\[
E = \frac{L_1 I^2}{2}
\]  
(2.41)

Consider again the charging circuit in Fig. 2.12, where the ideal inductor is pre-charged to the current \(I_0\) and holds an initial energy \(E_0 = \frac{L_1 I_0^2}{2}\). After \(L_1\) is charged instantaneously with \(V_i\) for time interval \(t_1\), the final energy \(E_{11} = \frac{L_1 I_{11}^2}{2}\). There is energy dissipating as heat when the inductor \(L_1\) is charging through the resistor \(R\) as shown in Fig. 2.12. According to the Joule-Lenz law, the power is \(P = I^2 R\) and its integrated value is the heating loss:

\[
E_h = \int_0^\infty i_{L_1}^2(t) R dt
\]  
(2.42)
The energy transfers too the inductor is the final energy minus the initial energy:

\[ F_{t1} - F_0 = F_{\text{trans}} = \frac{L_1(I_{t1})^2}{2} - \frac{L_1(I_0)^2}{2} \]  \hspace{1cm} (9.43)

And the energy delivered by the source can be calculated by taking the integral of the delivered power:

\[ E_d = V_s \int_0^{t1} i_{L1}(t) dt \]  \hspace{1cm} (2.44)

So the efficiency of the energy transfer is

\[ \eta = \frac{F_{\text{trans}}}{E_d} \]  \hspace{1cm} (2.45)

We have calculate this with Maple and plotted in Fig.2.14 We can see in the plot that the efficiency of the transferred energy begins by 100% and when we store more energy in the coil the efficiency drops. When we compare this to the capacitance then is this the opposite because the transferred energy starts with an efficiency of 0% and then when the capacitor is fully charged the efficiency is 50%. This difference can be explained by the fact that at beginning of switching there are fast changes in the transient signal and thus there are high frequencies in the signal at the moment of switching. For high frequencies the impedance of the capacitor is zero and the impedance of the inductor is very high. By charging with a voltage source the resistor is in series with the inductor and thus the whole voltage standing over the inductor and that was the opposite with the capacitor. With the inductor we can get a high efficiency from beginning of charging.
and drops when the voltage over the resistor is growing. There is only a problem with storing energy in an inductor because we can only store a current in a inductor and not a voltage thus we must also transfer the energy into a capacitor to store a voltage.

### 2.2.2.2 Charge Inductor with a current source

With this circuit we have the same problem as when we charge a capacitor with a voltage source but now the current can’t change instantaneously through the inductor. Let \( t = 0 \) be the instant of time when switching starts, and two additional instants: just prior and just after switching be \( t = 0^- \) and \( t = 0^+ \) respectively. In mathematical language, the value of the function \( f(0^-) \) is the "limit from the left”, as \( t \) approaches zero from the left, while \( f(0^+) \) is the "limit from the right”, as \( t \) approaches zero from the right. According to the above principle, the current (charge) of a inductor just after switching equals the current (charge) just prior to switching:

\[
i_{L1}(0^+) = i_{L1}(0^-) \tag{2.46}
\]

\[
q(0^+) = q(0^-) \tag{2.47}
\]

Defining an ideal switch as a zero-resistance device that gets opened or closed in zero time, we consider the charging circuit shown in Fig. 2.15(a), where the current source \( I_s \), the switch \( S_1 \) and the capacitor \( C \) are ideal. When \( S_1 \) is turned off, the inductor current \( I_{L1} \) changes abruptly from zero to \( I_s \). In other words, the charging of \( L_1 \) is accompanied by an infinitely high voltage pulse during an infinitely Small time. Using the above designations, we can write \( i_{L1}(0^-) = 0, \ i_{L1}(0^+) = i_s \) and \( i_{L1}(0^-) \neq i_{L1}(0^+) \) which
contradicts equation 2.46. In transient analysis, the last expression is called an incorrect initial condition for the chosen mathematical model of an ideal switched circuit. This contradiction can be ignored since any current source with a real switch has in practice some resistance connected in parallel. The infinite voltage spike is prevented in the switched circuits shown in Fig. 2.16, so that the initial conditions are correct. Note that such circuits may be composed by taking into consideration just the resistances of the switch. Thus now we look to the case with a ideal current source. It is described

Figure 2.16: Inductor charge circuit including a parallel resistance with a fixed current.

by a first order differential equation because it comprises only one inductor $L_1$. So, the aim is to calculate the complete response of the first order circuit to the current step $I_s$. According to Kirchhoff’s voltage Law $V_R = V_{L1}(t)$

$$ (I_s - I_{L1})R = L_1 \frac{di_{L1}(t)}{dt} $$  \hspace{1cm} (2.48)

Rearranging the above equation:

$$ \frac{di_{L1}(t)}{I_{L1} - I_s} = \frac{R}{L_1} \frac{dt}{dt} $$  \hspace{1cm} (2.49)

Now it can be simply integrated:

$$ \int \frac{di_{L1}(t)}{I_{L1} - I_s} = \frac{R}{L_1} \int dt $$  \hspace{1cm} (2.50)

The integration of both sides yields with the integration constant $D$:

$$ ln [I_{L1} - I_s] = \frac{R}{L_1} t + D $$  \hspace{1cm} (2.51)
Rearranging the above equation with $\tau = \frac{L}{R}$:

$$I_{L1} - I_s = e^{-(D + \frac{t}{\tau})}$$  \hspace{1cm} (2.52)

An initial current through $L_1$ will be

$$I_{L1}(0) = I_0 = I_s + e^{-D}$$ \hspace{1cm} (2.53)

So, the complete response is:

$$I_{L1}(t) = I_0 e^{-\frac{t}{\tau}} + I_s \left( 1 - e^{-\frac{t}{\tau}} \right)$$ \hspace{1cm} (2.54)

The complete response was calculated in Maple and is presented in Fig. 2.13 together with the current through the resistance $I_R = I_s - I_{L1}$. We can see in Fig.2.13 that the current through the inductor is growing over time while the current through the resistance is decreasing over time.

![Figure 2.17: $I_{L1}$ and $I_R$ by charge a inductor with current source](image)

Figure 2.17: $I_{L1}$ and $I_R$ by charge a inductor with current source

For the efficiency of the energy transfer we look to the energy transferred in the inductor and the dissipated energy in the resistor. Consider again the charging circuit in Fig. 2.16, where the ideal inductor is pre-charged to the current $I_0$ and holds an initial energy $E_0 = \frac{L_1 I_0^2}{2}$. After L1 is charged instantaneously with $I_s$ for time interval $t_1$, the final energy $E_{t1} = \frac{L_1 I_s^2}{2}$. There is energy dissipating as heat when the inductor $L_1$ is charging through the resistor $R_2$ and the current trough $R_1$ is dissipating heat as shown in Fig. 2.12. According to the Joule-Lenz law, the power is $P = I^2 R$ and its integrated value is the dissipated energy:

$$E_h = \int_0^\infty (I_s - I_{L1})^2(t)Rdt$$ \hspace{1cm} (2.55)
The energy transferred to the inductor is the final energy minus the initial energy:

$$ E_{t1} - E_0 = E_{trans} = \frac{L_1(I_{t1})^2}{2} - \frac{L_1(I_0)^2}{2} $$  \hspace{1cm} (2.56)

So the efficiency of the energy transfer is

$$ \eta = \frac{E_{trans}}{E_h + E_{trans}} $$  \hspace{1cm} (2.57)

We have calculate this with maple and plotted in Fig.2.18 We can see in the plot that

![Figure 2.18: energy efficiency charge inductor with voltage source](image)

the efficiency curve is the same as for the charge a capacitor with the voltage source case. And thus we always lose 50% of the energy when we not preflux the inductor.

### 2.2.3 Output capacitor

For the output storage element we take a capacitor because we want a voltage at the output and in the capacitor the voltage can’t change instantaneously.

#### 2.2.3.1 Charge Capacitor with another Capacitor

Now we look for the case when we charge capacitor with a other capacitor. The circuit with the two capacitors and the switch with a resistance R is shown in Fig. 2.4(b). When the switch is closed the capacitor $C_1$ (pre-charged to a voltage $V_i$) is discharged and simultaneously the empty capacitor $C_2$ is charged. To find the voltages across these capacitors, consider a bi directional current flow and compose two first order differential
equations:
\[
\begin{align*}
V_{C1}(t) &= V_{C2}(t) - RC_1 \frac{dV_{C1}(t)}{dt} \quad \text{or} \quad V_{C2}(t) = V_{C1}(t) + RC_1 \frac{dV_{C1}(t)}{dt} \\
V_{C1}(t) &= V_{C2}(t) + RC_2 \frac{dV_{C2}(t)}{dt}
\end{align*}
\] (2.58)

Take the Laplace Transform of both systems:
\[
\begin{align*}
V_{C1}(s) &= V_{C2}(s) - RC_1 [sV_{C1}(s) - V_{C1}(0)] \quad \text{or} \quad V_{C2}(s) = V_{C1}(s) + RC_1 [sV_{C1}(s) - V_{C1}(0)] \\
V_{C1}(s) &= V_{C2}(s) [1 + sRC_2 - V_{C2}(0)] \quad \text{or} \quad V_{C2}(s) = V_{C1}(s) - [sRC_2 V_{C2}(s) - V_{C2}(0)]
\end{align*}
\] (2.59)

By filling in $V_{C1}(0) = V_s$ and $V_{C2}(0) = 0V$ the solutions in the Laplace domain are:
\[
\begin{align*}
V_{C1}(s) &= \frac{C_1 V_s (1 + sRC_2)}{s^2 RC_1 C_2 + s(C_1 + C_2)} \quad V_{C2}(s) = \frac{C_1 V_s}{s^2 RC_1 C_2 + s(C_1 + C_2)}
\end{align*}
\] (2.60)

Taking the Inverse Laplace Transform of both equations (2.60), we obtain the voltages in the time domain. To simplify the expressions we introduce the time constant $\tau = RC_1 C_2 / (C_1 + C_2)$ since the current flows through serially connected capacitors.
\[
\begin{align*}
V_{C1}(t) &= \frac{C_1 V_s}{C_1 + C_2} + \frac{C_2 V_s}{C_1 + C_2} e^{-\frac{t}{\tau}} \quad V_{C2}(t) = \frac{C_1 V_s}{C_1 + C_2} \left[1 - e^{-\frac{t}{\tau}}\right]
\end{align*}
\] (2.61)

With the current
\[
I(t) = \frac{V_{C1}(t) - V_{C2}(t)}{R} = \frac{V_i}{R} e^{-\frac{t}{\tau}}
\] (2.62)

The boundary values are:
\[
I(0) = I_0 = \frac{V_i}{R} \quad V_{C1} = \lim_{t \to \infty} V_{C1}(t) = \frac{C_1 V_s}{C_1 + C_2} \quad V_{C2} = \lim_{t \to \infty} V_{C2}(t) = \frac{C_1 V_s}{C_1 + C_2}
\] (2.63)

At the begin time of switching, the current is limited by the resistance $I(0) = \frac{V_i}{R}$ and reaches 0.01 of this value at 5$\tau$. As follows from equation (2.60), the transient slopes for $C_1$ and $C_2$ are different and defined by the time constants $RC_1$ and $RC_2$ respectively. Since in this particular case, $C_1$ is pre-charged to $V_i$, its discharging can be considered as the natural response, while the charging of empty $C_2$ matches the definition of a forced response. Both the voltages of equation (2.61) and the current through $R$ given by equation (2.62) were calculated in Maple and depicted in Fig. 2.19.

The efficiency analysis of this case is done in the same way as the voltage source charging a capacitor. With energy in the output capacitor $E_o = \frac{C_2 V_{C2}(t)^2}{2}$, energy in the input capacitor $E_i = \frac{C_1 V_{C1}(t)^2}{2}$ and the energy loss in the resistance $E_{Loss} = \int_0^1 I(t)^2 R dt$ becomes the efficiency:
\[
\eta = \frac{E_o}{E_o + E_{Loss} + E_i} = \frac{C_2 C_1 \left(1 - e^{-\frac{t}{\tau}}\right)^2}{(C_1 + C_2)^2}
\] (2.64)

This is calculated with Maple and plotted in Fig.2.20. We see in this figure that the efficiency is increasing over time until the point where the voltage of both capacitors is
the same. We can see in this plot that the efficiency at this point is 25%. For analyzing where the other 75% is lost the different energies are calculated with maple and plotted in Fig.2.21. It is seen that we lose half of the energy in the resistance, independent of the size of the resistance. We explain this by the same fact as explained by the case of charging a capacitor with a voltage source. The other quarter of the energy we don’t lose but is still in the capacitor $C_1$. When we look to the efficiency Equation (2.64) we can see that we get the highest efficiency when we chose the value for $C_2$ the same as $C_1$. Thus when we look to the efficiency in this case we see that when the capacitor isn’t pre-charged the efficiency of the energy transfer is always lower than 25%. But when we look to the case when we pre-charge the capacitor $C_2$ the efficiency can be a lot higher because the same reason as by the case of charge the capacitor with a voltage source.

In the next section we will look to the case when we charge the output capacitor with a inductor.

### 2.2.3.2 Charge Capacitor with inductor

The charging circuit with the voltage source, inductor, capacitor and non ideal switch is shown in Fig. 2.22. It is described by a second order differential equation because it comprises one inductor $L_1$ and one capacitor $C_1$. So, the aim is to calculate the complete response of the second order circuit to the voltage step $V_i$. According to Kirchhoff’s voltage Law $V_i - V_R - V_{L1}(t) = V_{C1}(t)$, this is:

$$V_i = L_1 \frac{di_L(t)}{dt} + I_L(t)R = \frac{1}{C_1} \int I_{L1}(t)dt$$

(2.65)
Figure 2.20: Efficiency over time when charge a capacitor with other capacitor C1=C2=10.6 R=1

Rearranging and differentiating the above equation:

\[ 0 = L_1 \frac{d^2 i_{L1}(t)}{dt^2} + R \frac{di_{L1}(t)}{dt} + \frac{1}{C_1} I_{L1}(t) \]  

(2.66)

Take the Laplace Transform of the equation:

\[ 0 = s^2 + \frac{R}{L_1}s + \frac{1}{L_1C_1} \]  

(2.67)

so s1 and s2 can be calculated

\[ s1 = \frac{-R}{2L_1} + \sqrt{\left(\frac{R}{2L_1}\right)^2 - \frac{1}{L_1C_1}} \]  

(2.68)

\[ s2 = \frac{-R}{2L_1} - \sqrt{\left(\frac{R}{2L_1}\right)^2 - \frac{1}{L_1C_1}} \]  

(2.69)

So, the complete response is:

\[ i_L(t) = A_1 e^{s1t} + A_2 e^{s2t} \]  

(2.70)

To solve A1 and A2 fill in the initial conditions \( I_0 \) the initial current in the inductor and \( V_0 \) the initial voltage over the capacitor for \( t=0 \)

\[ I_0 = A_1 + A_2 \]
Figure 2.21: Energy in the capacitors and energy lose in the resistor plotting over time when charging a capacitor with other capacitor $C_1 = C_0 = 1 \mu F$ and $R = 1 \Omega$

Figure 2.22: Capacitor charge circuit included a series resistance with a fixed voltage and pre-charged inductor.

$$V_0 = V_i - I_0 R - L_1 \frac{di(t)}{dt} = V_i - I_0 R - L_1 (s1A_1 + s2A_2)$$

Now $A_1$ and $A_2$ can be solved

$$A_1 = \frac{I_0 s1 - V_0 C_1 s1 s2}{s1 - s2}$$

$$A_2 = \frac{I_0 s2 - V_0 C_1 s1 s2}{s2 - s1}$$

So, the voltage across the capacitor is:

$$V_C(t) = \int_0^t A_1 e^{s1t} + A_1 e^{s2t} dt$$

(2.71)
And after integrating:

\[
V_C(t) = V_0 + \frac{A_1 s^2(e^{s1t} - 1) + A_1 s1(e^{s2t} - 1)}{C_1 s1s2}
\]  

(2.72)

When we look to s1 and s2 there are three responses possible. A square root of a real number, a negative number or zero. We define the damping factor

\[
\zeta = \sqrt{\left(\frac{R}{2L_1}\right)^2 \frac{1}{L_1C_1}} = \frac{R}{2L_1} \sqrt{\frac{C_1}{L_1}}
\]

We have plotted the different response voltage over the capacitor for the different ζ in Fig.2.23. We can see when the square root is real ζ>1 the response is overdamped and

![VC for different responses](image)

Figure 2.23: VC for different responses Vs=1 V0=0 and 10=0

when the square root is complex ζ < 1 the response is underdamped and when the square root is zero ζ = 1 the response is critically damped.

When we look to efficiency we look to the quality factor Q that is defined as

\[
Q = \frac{2\pi E_{stored}}{E_{discharge}} = \frac{1}{2\zeta} = \frac{1}{R \sqrt{\frac{L_1}{C_1}}}
\]

From this we can see that when we want high efficiency we want a high Q. Q is high when ζ is small. Because we want efficient charge of the capacitor we look further more to the case when ζ < 1. We have now plotted the voltage over the resistor, capacitor, inductor and the current in the circuit in Fig.2.24.

We see that there is energy exchange between the capacitor and the inductor. The voltage will grow over the capacitor until the point that all the energy is out of the
Figure 2.24: $V_{L1}$ and $V_R$ and $V_{C1}$ and the current by discharge a inductor with voltage source in a capacitor with $C_1 = 1 \mu F$, $L_1 = 1 \mu H$, $R = 0.1 \Omega$, $V_i = 1V$, $V_0 = 0V$ and $I_0 = 0A$

inductor this is when the current is zero. After that point the energy is flowing back in to the inductor and thus the voltage is decreasing over the capacitor. Now when we want too see the efficiency of the energy transfer in this case.We look to the energy in the capacitor before charging.

$$E_0 = \frac{C_1 V_0^2}{2}$$  \hspace{1cm} (2.73)

And to the energy in the capacitor while charging

$$E_C = \frac{C_1 V_{C1}^2(t)}{2}$$  \hspace{1cm} (2.74)

The energy transferred to the capacitor is

$$E_C - E_0 = E_{trans} = \frac{C_1 V_{C1}^2(t)}{2} - \frac{C_1 V_0^2}{2}$$  \hspace{1cm} (2.75)

and the delivered power of the source is

$$E_d = V_i \int_{0}^{1} I_{L1}(t) \, dt$$  \hspace{1cm} (2.76)

There is energy dissipating as heat because the fact that the inductor $L_1$ is charging the capacitor $C_1$ through the resistor $R$ as shown in Fig. 2.22. According to the Joule-Lenz
law, the power is $P = I^2R$ and its integrated value is the heating loss:

$$E_h = \int_0^{t_1} I_{L1}^2(t) \cdot R \, dt$$  \hspace{1cm} (2.77)

Total used power is the delivered power of the source and the initial energy in the inductor:

$$E_d + E_{I1} = V_i \int_0^{t_1} I_{L1}(t) \, dt + \frac{L_1 I_0^2}{2}$$  \hspace{1cm} (2.78)

so efficiency can be calculated with

$$\eta = \frac{E_c}{E_d + E_{I1}}$$  \hspace{1cm} (2.79)

![Graph showing efficiency by discharge of an inductor with voltage source in a capacitor.](image)

**Figure 2.25:** efficiency by discharge of an inductor with voltage source in a capacitor.

This is calculated with Maple and plotted in Fig. 2.25. In the plot we can see that the efficiency of the transferred energy starts at 0% and when we store more energy in the capacitor the efficiency grows till the point that all the energy from the inductor is stored in the capacitor. The highest efficiency is at the moment that the inductor is fully discharged in the capacitor and the current is zero. Thus we can get a high efficiency when we open the switch when the inductor is fully discharged in the capacitor.

### 2.3 Practical capacitor converters

There are different types of the capacitive converter. The most known type of capacitive DC-DC converter is called a charge pump like as in Fig. 2.26. Where switches $S_1, S_3$
and $S_5$ are switched with $CLK$ and the switches $S_2$ and $S_4$ are switched with $CLKn$.
At the moment that the $CLK$ signal is high $S_1$ is closed and $C_1$ is charged to $V_i$ because $CLKn$ is low. At the moment that $CLKn$ is high switch $S_1$ is opened and $S_2$ is closed and the potential of the node between switch $S_1$ and $S_2$ is $2V_i$ and thus $C_2$ is charged to $2V_i$. At the next moment $CLK$ is high and $S_2$ is opened and $S_3$ is closed and the potential of the node between $S_2$ and $S_3$ is $3V_i$ and thus $C_3$ is charged to $3V_i$ and so on. For historical reasons it is often considered to be a step-up converter built from capacitors and diodes, which are used as switches. Nowadays, when charge pumps are built around transistor switches, their circuitry does not differ in principle from the step-down switched capacitor DC-DC converters. The cornerstone of both circuits is a reconfigurable array of switches and capacitors generally called “flying capacitors” this are the capacitors $C_1,C_2,C_3$ and $C_4$ in fig. 2.26 because neither of the capacitors have fixed voltage nodes. These capacitors are charged from the input voltage and then discharged to the load thus providing charge transfer and a constant output voltage. The capacitive converters based on switched capacitors are widespread in applications requiring small power and no isolation between input and output. They feature minimal radiated EMI, relatively low noise and in most cases are fabricated as integrated circuits which have made capacitive converters popular for use in power management for mobile devices. An additional goal of such converters is the option for unloaded operation with no need for dummy loads or complex control because when the capacitors fully charged the converter is in steady state and there is no energy transfer from input to output.

![Schematic of a chargepump](image)

Figure 2.26: schematic of a chargepump

However, as we have previously demonstrated capacitive converters suffer from inherent power loss during charging and discharging of a capacitor in parallel with the voltage source or another capacitor. Theory predicts that this power loss is proportional to the squared voltage difference taking place before the corresponding circuit has been configured see equation 2.18. As a result, capacitive converters exhibit a rather high efficiency if the capacitors pre-charged to certain voltages are paralleled with components maintaining similar voltages. When the same capacitive converter operates between or outside the target voltage ratios, the efficiency drops dramatically[15, 23].

The disadvantage of capacitive converters for high conversion ratios is the larger number of switches and respective drivers complicating the converter circuitry. Another
problem of capacitive converters is a high inrush current during start-up that must be limited by soft-start circuitry. Another fundamental problem of capacitor converter is the fact that the capacitors nodes both are flying. Because of this fact every cycle the parasitic capacitance is now charging and discharging which leads to a loss of energy with on chip capacitors[18]. In this work there is analysis when everything is ideal what the highest efficiency can be because the fact of the parasitic capacitance. The following relation is found [18]:

\[
\eta_{max} = \frac{k}{1 + \left(\frac{1 + \sqrt{1 + a^2}}{1 - \sqrt{1 + a^2}}\right)(k - 1)}
\]

Where \(k\) is the multiplication factor of the output voltage divided by the input voltage and \(a\) is the ratio between the parasitic capacitance and the capacitance itself. We have calculated the maximum efficiency versus the ratio \(a\) with maple with \(k = 6\) and this is plotted in fig.2.27. We see in this plot that when the parasitic capacitance is 5% of the capacitance value the maximum efficiency already drops below the 70%.

When we consider off chip capacitors there no longer the problem of the parasitic capacitance but there is another problem with the fact that the capacitors are flying because now we must have two bondpads for every capacitor. This leads to a lot of connections when we want a high conversion.

Another capacitor converter is based on the Micro-electromechanical systems (MEMS) technology[14]. The working principle of this converter is based on the fact that when we change the capacitance value of the capacitor the voltages also change over the capacitor. Thus the capacitor is charged from the input source to the input voltage and before it's
discharging to the load the capacitor is mechanical modified what leads to a different voltage by the discharge of the capacitor.

2.3.0.3 Variable output voltage with capacitor converter

When we make the switched capacitor converter (SCC) with a set of discrete target voltages we can make a variable output voltage. This set of target voltages is closely related to the SCC efficiency over the full range of output voltages. The target voltage is the no-load output voltage and is equal to some multiple \( n \) of the input voltage. In general, \( n \) is a function of the number of flying capacitors and the way that they are connected to the input and output and among themselves. So the target voltage is independent of the values of the flying capacitors and determined only by the SCC topology, while \( n \) can be a positive or negative rational number [27, 11]. At each target voltage, the SCC efficiency reaches a maximum value and drops when the desired output voltage drops below the target voltages. For example, a commercial SCC operates at the fixed input voltage \( V_i = 3V \) and has three peaks of efficiency shown in Fig. 2.28. This SCC can be switched between three conversion ratios \( n = \frac{3}{2}, 2 \) and 3. When the output voltage must be lower than about 4.5 V, the conversion ratio is set to \( n = \frac{3}{2} \) and for output voltage above 4.5V and lower than 6V it is switched to \( n = 2 \) and above 6V it is switched to \( n = 3 \). Consequently, high efficiency is observed when the output voltage must be about \( 4.5V(3 \cdot \frac{3}{2}), 6V(3 \cdot 2) \) and at \( 9V(3 \cdot 3) \). When the SCC operates between and outside these three target voltages, the efficiency drops.

Any SCC can be modeled by an equivalent circuit that includes a voltage source \( V_{\text{trg}} \) and an internal resistance \( R_{\text{eq}} \) as depicted schematically in Fig. 2.29 [11]. In the model presentation of Fig. 2.29, the power losses are conveniently described as a function of the load current which simplifies the input to output voltage ratio as well as the efficiency:
\[
\frac{V_o}{V_{trg}} = \frac{R_o}{R_o + R_{eq}} \quad (2.80)
\]
\[
V_{trg} = nV_i \quad (2.81)
\]
\[
\eta = \frac{V_o}{V_{trg}} = \frac{1}{n} \left( \frac{R_o}{R_o + R_{eq}} \right) \frac{V_o}{V_i} \quad (2.82)
\]

It is clear, that the highest efficiency will be achieved if \( n \) is such that \( V_{trg} \) is made close to the desired \( V_o \), leaving a small voltage drop on \( R_{eq} \). It is also clear that the best efficiency can be obtained if the resolution of \( n \) is high and when its values are evenly spaced. Previous attempts to improve the efficiency by changing \( n \) on-the-fly gave SCC configurations with a limited number of target voltages, namely with a coarse resolution of \( n \). As a result, the efficiency drops significantly when the required \( n \) is in between the sparsely spread values of \( n \).

SCC can be operated in open loop or closed loop configurations. In the open loop case, \( n \) and \( R_{eq} \) are fixed. In this case, the output voltage will not be regulated and will depend on \( V_i \) and the load resistance \( R_o \). In this situation, it is advantageous to reduce \( R_{eq} \) as much as possible to keep the efficiency high. Regulation can be achieved by either changing \( n \) or \( R_{eq} \) (or both) \([27, 30]\). The no-load voltage can be changed by changing on-the-fly the SCC topology and hence altering \( n \), while \( R_{eq} \) can be changed by adding a linear regulator in the charging/discharging paths. Other possibilities to vary \( R_{eq} \) are frequency dithering, frequency change, and duty cycle control \([4, 29, 13, 11]\).

### 2.4 Practical Inductive converters

The inductive converters have been a power supply solution in all kinds of applications for many years due to the wide variety of possibilities in current and voltage requirements. There are three basic inductive converters the up converter call the boost, the down converter call the buck, and the up-down converter call the buck-boost converter\([7]\). These converters can made with only one inductor and one output capacitor. Generally, the advantage for these inductive converters are that they are efficient over a wide range of output currents and wide range of output voltage, it is easy to make the output voltage variable and only one inductor is required for a high conversion ratio.

But there are also disadvantages for this converter. The inductor in such a converter is bulky, hard to realize on-chip \([21, 10, 6]\) and electromagnetic interference (EMI) is an issue because of the pulsating current through the inductor. There are also more advanced converters\([2, 25, 22]\) like the flyback converter and the forward converter with the advantage that the input and output circuit’s are isolated from each other, but the price we pay for this is that they use a transformer that is more bulky than only one inductor.

An other advanced converter is the resonant converter. In this converter a capacitor resonates with an inductor like as in section 2.2.3 the case charge capacitor with the inductor. With this converter the switching losses are low because now we can switch
with zero voltage or zero current. The advantage of this converter is that they work with a high efficiency, but the disadvantage is that the converter only works in a small range because otherwise the converter is out of resonance and we need extra components as an extra capacitor and a transformer what make the converter more bulky. And there are also combinations of the inductor based and capacitor based converters like as [1]. We will only look further to the basic converters because we want a converter as small as possible.

When we look to the implementation of the inductor, on chip is hard to design because we need a low series resistance when we want a high efficiency and a high conversion factor. When we choose for off chip inductor we only have one more connection to the chip because by the buck converter one side of the inductor is connected to ground and with the boost converter one side of the inductor is connected to the input source. Thus we only need one extra bondpad when we choose for an off chip inductor.

2.5 Conclusion

In this chapter we have seen that the energy transfer of a voltage source to the inductor is an efficient way for energy transfer if the charging time is low and/or the initial current trough the inductor is low. By charging the capacitor there is always a lose of fifty percent of the energy when we not pre charge the capacitor. But the efficiency can be high when the initial voltage over the capacitor is closer to the charging voltage.

When we look to the variable output voltage the capacitor based converter is only efficient when the converter works on the optimal voltage conversion ratio and when the voltage ripple at the output is made low. The inductor based converter works efficient over the whole range of voltage conversion ratio and output power. An other disadvantage of the capacitor converter is when we want to make a charge pump that delivers high energy, we need big capacitors and that leads to a lot of area on the chip. And when we want a high conversion factor we need more capacitors. With a seven times voltage converter we need seven big capacitors. For on chip capacitors we have than also a high loss because of the parasitic capacitance. When we will make it with off chip capacitors we need two bond pads for every capacitor what lead to 14 bondpads.

When we look to the inductor the on chip inductor is also not a good option because we need a good inductor with a low resistance for a high voltage conversion and that cannot be made with on chip inductors. With an off chip inductor we only need one bondpad because one site of the inductor is connected to ground with a buck-boost converter and connected to the voltage source with the boost converter. This is summarized in Table 2.1.

Because we want a high voltage conversion we cannot make the complete converter on chip. For the capacitor based converter we need 14 bondpad’s when we choose for off chip and that’s too much because we want as few connections as possible. Thus we choose a inductor based converter.
<table>
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<th>on chip capacitor based</th>
<th>off chip capacitor based</th>
<th>on chip inductor based</th>
<th>off chip inductor based</th>
</tr>
</thead>
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<td>small</td>
<td>big</td>
<td>small</td>
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<td>2 for every conversion ratio</td>
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<td>1</td>
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<td>1</td>
</tr>
<tr>
<td>variable voltage</td>
<td>medium</td>
<td>medium</td>
<td>easy</td>
<td>easy</td>
</tr>
</tbody>
</table>

Table 2.1: Overview of converter selection
3 System level design of the Inductive converter

3.1 System Topologies

In Chapter 2 we have motivated the choice for the inductor converter. Now there are different topologies for this type of circuit and in this section we will choose the topology. We have the freedom to choose 3 of the components, because at the input we have a voltage source and we want a capacitor at the output as stated in the chapter before. Then we have to choose where we want to place the switches to charge and discharge the inductor and the place of the inductor. We can make 3 different schematics as is shown in Fig 3.1. In the schematic we can see that there are three positions for the

![Diagram of different topologies](image)

Figure 3.1: (a) Boost converter (b) Buck converter (c) Buck-Boost converter

inductor. The name of the different converters are boost, buck and buck-boost. In the next sections we analyze the different options.

3.1.1 Boost converter

The name given to the converter with the inductor connected to the input is the boost converter. A simple schematic of the boost converter is shown in Fig 3.1 (a).

Switches $S_1$ and $S_2$ are switched on and off alternately but the duration of $S_1$ being ‘on’ decides the duty cycle $D$. Due to the switching, the voltages and the currents have ripples. These ripples are filtered out by the inductor and the capacitor. As shown in Fig. 3.2(a) switch $S_2$ can be replaced by a diode $D_1$ which conducts when switch $S_1$ is
Figure 3.2: (a) Boost converter schematic using diode (b) when the switch S1 is on (c) when the diode D1 is on

off. When switch $S_1$ is on as in Fig. 3.2(c) a current flows from $V_i$ through the inductor to ground. In this state the inductor $L$ stores energy in the magnetic field. The energy stored in the capacitor is now used as a energy supply for the load. When switch $S_1$ is off as in Fig. 3.2(b) the inductor tries to maintain the current that was flowing through it and hence supplies the current towards the load. This leads to a growing voltage over the inductor. Until the point that the diode becomes forward biased. The diode $D_1$ turns on and completes the connection to the output. The current is now flowing to the load and also to the capacitor which leads to an increase in the voltage over it. The capacitor at the output filters the voltage ripple across the load resistor $R_{Load}$.

The forward voltage at the diode can be considerable compared to the supply voltage when operating in low voltage technologies. Therefore this diode is replaced by a switch. The switch must always switch off before the moment that the current through the switch goes negative so that the inductor and output capacitor can’t oscillate. When the diode is replaced by a switch the boost converter is called a synchronous boost converter. When the energy stored in the inductor is enough to keep a certain non-zero amount of current flowing through the load before it needs to recharge the energy it is called ‘continuous conduction mode (CCM)’. If the inductor current falls to zero before the next instant of the switch $S_1$ to become on, it is called ‘discontinuous conduction mode (DCM)’. We will talk more about DCM and CCM in the next part of this chapter. The inductor current profiles for the continuous conduction mode and the discontinuous conduction mode are shown in Fig. 3.3. From [7] we get the simplified transfer.

$$\frac{V_o}{V_i} - M_{Boost} - \frac{1}{1 - D} \quad (3.1)$$

Where $M_{Boost}$ is the multiple factor and $D$ is the duty cycle. We can see in this equation that the output voltage can only be higher than the input voltage $V_o \geq V_i$. 

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Figure 3.3: Inductor current in (a) continuous conduction mode (b) discontinuous conduction mode

3.1.2 Buck converter

Buck converter is the name given to the converter with the inductor connected to the output. The circuit of a buck converter can be implemented as shown in Fig 3.1 (b). Switches $S_1$ and $S_2$ are switched on and off alternatively, but the fraction of time that the switch $S_1$ being ‘on’ from the cycle time decides the duty cycle $D$. As shown in Fig. 

![Buck Converter Diagram](image)

Figure 3.4: (a) Boost converter schematic using diode (b) when the switch $S_1$ is on (c) when the diode $D_1$ is on

3.4(a), switch $S_2$ can be replaced by a diode $D_1$ which conducts when switch $S_1$ is off. When switch $S_1$ is on, as in Fig. 3.4(b) a current flows from $V_i$ through the inductor to the output $V_o$. In this mode the inductor $L$ is used to store the energy in the magnetic field. When switch $S_1$ is off as in Fig. 3.4(c), the inductor tries to maintain the current that was flowing through it and hence supplies the current towards the load. This leads to a growing voltage over the inductor till the point that the diode is forward biased. At this point the diode $D_1$ turns on and completes the connection to ground required for the current flow. In this converter the inductor smooth out the ripple in the output
current. The capacitor is used at the output to filter the voltage ripple across the load resistor $R_{\text{Load}}$.

The simplified transfer we get from [7]:

$$\frac{V_o}{V_{in}} = M_{\text{Duck}} - D$$

We can see in this equation that the output voltage can only be lower than the input voltage, i.e. $V_o \leq V_i$.

### 3.1.3 Buck boost converter

Buck boost converter is the name given to the converter where the inductor is connected to the ground. A simple buck boost converter can be implemented as shown in Fig 3.1 (c). Switches $S_1$ and $S_2$ are switched on and off alternately, and also in this converter the duration of $S1$ being ‘on’ decides the duty cycle $D$. Due to the switching, the output voltage and the current have ripples. As shown in Fig. 3.5(a) switch $S_2$ can be replaced by a diode $D_1$ which conducts when switch $S_1$ is off. When switch $S_1$ is on as in Fig. 3.5(b) a current flows from $V_i$ through the inductor to ground. In this state the inductor $L$ is used to store the energy in the magnetic field. The energy to the load is delivered by the capacitor in this state. When switch $S_1$ is off as in Fig. 3.5(c) the inductor tries to maintain the current that was flowing through it and hence supplies the current from its stored energy which leads to an increasing voltage until the point that the diode is forward biased. The diode $D_1$ turns on and completes the connection to the output so that the current can flow through the load. The inductor is neither connected to the output nor the input and thus we have on the input and output a current ripple. A capacitor is used at the output to filter the voltage ripple across the load resistor $R_{\text{Load}}$.

The simplified transfer we get from [7]:

---

Figure 3.5: (a) Boost converter schematic using diode (b) when the switch $S_1$ is on (c) when the diode $D_1$ is on
\[
\frac{V_o}{V_{in}} = M_{Buck-Boost} = \frac{-D}{1 - D}
\]

We can see in this equation that the output voltage is always negative but the amplitude can be lower or higher than the input voltage \(V_o \leq 0\).

### 3.1.4 Choice for converter

The converter needs to convert the input voltage to a voltage several times higher and every voltage in between. For the choice we have plotted the different conversion for each converter type in a figure. In this figure we see the difference between the different converters. The boost converter cannot convert voltages lower than the input voltage while the other two can do this. The buck converter can’t convert into higher voltages than the input voltage. We can see that using the same duty cycle the boost converter always has a higher output voltage than the Buck-boost. The Buck-Boost also has the disadvantage that it converts with a minus sign. Because we always have to convert always the input voltage to a higher voltage we choose a boost converter.

![Conversion Factor of the Boost, the Buck and the Buck-Boost converter](image)

**Figure 3.6.** Conversion Factor of the Boost, the Buck and the Buck-Boost converter

### 3.2 Operation mode

Now for the boost converter we need to look at the operation mode. The converter can work in two modes [7, 3]: the continuous conduction mode (CCM) when the current through the inductor isn’t zero in the switching period. The other mode is the discontinuous conduction mode (DCM), when the current through the inductor will be zero
for some moment in the switching period. There are many differences in the stability, the inductance and frequency. In the next sections we look in to the difference between the different modes.

3.2.1 Continuous Conduction Mode (CCM)

We will analyze the CCM mode in the same way as in [7] but now taking into account of the drain-to-source resistance and the forward diode voltage. When we consider the continuous conduction mode, there are two states per switching cycle for the boost converter. The charge state: $S_1$ is on and $S_2$ is off, and the discharge state: $S_1$ is off and $S_2$ is on. For analyzing the circuit we represent each of the two states in Figure 3.2(b) and 3.2(c) shows the equivalent circuit diagram. The duration of the charge phase is $DT_s - T_{ch}$, where $D$ is the duty cycle set by the control circuit, and $T_s$ is the time of one complete switching cycle. The duration of the discharge phase is $T_{di}$. Since there are only two phases per switching cycle for continuous conduction mode, $T_{di} = (1 - D)T_s$. These times are shown along with the waveforms in Fig. 3.7. During the charge phase, $S_1$, which presents a low drain-to-source resistance ($R_{DS,on}$) to simplify the equations we assume that the resistance is constant and the voltage drop over the switch is $I_LR_{DS,on}$. There is also a small voltage drop across the on resistance of the inductor ($R_L$) equal to $I_LR_L$. Diode $D_1$ is off during this time because it is reverse biased. Thus the input voltage $V_i$ minus the losses ( $I_L(R_L + R_{DS,on})$ ), is applied across inductor $L$. The inductor current, $i_L$, flows from the input source, $V_i$, through $S_1$ to ground. During the charge phase, the voltage across the inductor ($V_L$) is almost constant and equal to $V_i - I_L(R_L + R_{DS,on})$. As a result of the applied voltage the inductor current increases. The inductor-current increase can be calculated by:

$$V_L = L \frac{di_L}{dt} \Rightarrow \Delta I_L = \frac{V_L}{L} \Delta T$$

(3.2)

And when we fill this in we get:

$$\Delta I_{L(+)} = \frac{V_s - I_L(R_L + R_{DS,on})}{L} T_{ch}$$

(3.3)

The quantity $\Delta I_{L(+)}$ is the inductor ripple current see Fig. 3.7. During the charge

![Figure 3.7: Current in CCM with $T_{ch}, T_{di}, \Delta I_L$ and $I_L(AVG)$](image)

period of the inductor all of the output load current is delivered by the output capacitor $C$. Now we look to the discharge period when $S_1$ is off the drain-to-source impedance
is high. Since the current flowing through inductor $L$ cannot change instantaneously
the current shifts from $S_1$ to $D_1$. Due to the decreasing inductor current the voltage
across the inductor reverses polarity until rectifier $D_1$ becomes forward biased and turns
on. The voltage applied to the left node of $L$ remains the same as before, i.e. $V_i - I_L R_L$
. The voltage applied to the right node of $L$ is now the output voltage, $V_o$, plus the
diode forward voltage, $V_d$. The inductor current $I_L$ now flows from the input source
$V_i$ through $D_1$ to the parallel combination of the output capacitor and the load resistor.
During the discharge phase the voltage across the inductor is almost constant and equal
to $(V_o + V_d + I_L R_L) - V_i$. Maintaining the same polarity convention this voltage is negative
(or opposite in polarity from the applied voltage during the charge time). Hence the
inductor current decreases during the discharge time. The inductor current decrease
during the discharge phase is given by:

$$\triangle I_{L(-)} = \frac{(V_o + V_d + I_L R_L) - V_s}{L} T_{di}$$

(3.4)

The quantity $\triangle I_{L(-)}$ is also the inductor ripple current. In steady-state conditions the
current increase $\triangle I_{L(+)}$ during the charge time and the current decrease $\triangle I_{L(-)}$ during
the discharge time are equal. For the steady state analysis $\triangle I_{L(+)} = \triangle I_{L(-)}$ solving for
$V_o$ to obtain the continuous conduction mode boost voltage conversion relationship. The
steady-state equation for $V_o$ is then:

$$V_o = (V_s - I_L R_L) \left( 1 + \frac{T_{ch}}{T_{di}} \right) - V_d - I_L R_{DS, on} \left( \frac{T_{ch}}{T_{di}} \right)$$

(3.5)

And, using $T_s = T_{ch} + T_{di}$, and using $D = \frac{T_{ch}}{T_s}$ and $(1-D) = \frac{T_{di}}{T_s}$, the steady-state equation
for $V_o$ is:

$$V_o = \frac{V_s - I_L R_L}{1 - D} - V_d - I_L R_{DS, on} \left( \frac{D}{1 - D} \right)$$

(3.6)

The discontinuous conduction mode analysis will show that the above equation is true
only for continuous conduction mode.

In the above equations for $\triangle I_{L(+)}$ and $\triangle I_{L(-)}$ the output voltage was implicitly
assumed to be constant with no ac ripple voltage during the charge and discharge phases.
The output capacitor is assumed to be large enough so that its voltage change is negligible.
These assumptions are valid when the ac ripple voltage is designed to be much less
than the dc part of the output voltage. The above voltage conversion relationship for $V_o$
illustrates that $V_o$ can be adjusted by adjusting duty cycle $D$. A common simplification
is to assume $R_{DS, on}$, $V_d$, and $R_L$ are small enough to ignore. Setting $R_{DS, on}$, $V_d$, and
$R_L$ to zero, the above equation simplifies considerably to:

$$V_o = \frac{V_i}{1 - D}$$

(3.7)

Which corresponds to Eq.3.1. To analyze the average current through the inductor, we
consider the discharge phase because only in that phase the inductor delivers current
to the output. The average current in the output capacitor must be equal to zero in
steady state thus the inductor current averaged over a complete switching cycle is equal to the output current \( (I_o) \). The relationship between the average inductor current and the output current for the continuous mode boost power stage is thus given by:

\[
I_{L(\text{AVG})} = \frac{T_{di}}{T_s} I_o (1 - D) - I_o \tag{3.8}
\]

or,

\[
I_{L(\text{AVG})} = \frac{I_o}{(1 - D)} \tag{3.9}
\]

An important observation is that the inductor ripple current \( (\Delta I_L) \) is independent of the output load current and the average inductor current is proportional to the output current. Because of this fact the minimum and the maximum values of the inductor current track the average inductor current exactly. In other words, if the average inductor current decreases by 20 mA due to a load current decrease then the minimum and maximum values of the inductor current decrease also by 20 mA (but only as long as continuous conduction mode is maintained).

### 3.2.2 Discontinuous Conduction Mode (DCM)

Now consider what happens when the circuit parameters change, e.g. due to decreasing the inductance or increasing the load resistance or changing the duty cycle \( (D) \) and the conduction mode changes from continuous to discontinuous. We explain now the DCM mode by decreasing the inductance. As seen in the previous section for a lower inductance the current ripple increases, but the average current is not changed because this is set by the output current. The current ripple increases until the point where it is twice the average current. After this point the current through the inductor is zero for a part of the switching cycle as shown in Fig.3.8. In a boost power stage, when

![Diagram showing current from CCM to DCM](image)

Figure 3.8: Current from CCM to DCM by lowering the inductance value

the inductor current will fall below zero it just stops at zero due to the unidirectional current flow in the diode and remains there until the beginning of the next switching cycle. This operating mode is called the discontinuous current mode. In discontinuous current mode there are three unique phases during each switching cycle. These phases are the same two phases as in the continuous current mode but now there is one extra phase; this is the phase in which \( I_L = 0 \). We call it the off phase. The charge phase is when \( S_1 \) is on and \( D_1 \) is off. The discharge phase is when \( S_1 \) is off and \( D_1 \) is on. The off state is when both \( S_1 \) and \( D_1 \) are off. The first two states are identical to the continuous
current mode case except that in the discontinuous current mode \( T_{di} \neq (1-D)T_s \). This is due to the off state. The duration of the charge state is \( T_{ch} = DT_s \), where \( D \) is the duty cycle set by the control circuit expressed as a ratio of the on time of the switch and the time of one complete switching cycle \( T_s \). The duration of the discharge state is \( T_{di} = D_2 T_s \). The off time is the remainder of the switching cycle and is given as \( T_{off} = T_s - T_{ch} - T_{di} = D_3 T_s \). These times are shown with the corresponding waveforms in Fig. 3.9. The equations for the current are given below. The inductor current increase during the charge state is given by:

\[
\Delta I_{L(+)} = \frac{V_s - I_L(R_L + R_{DS,on})}{L} T_{ch} = I_{pk}
\] (3.10)

The current starts at zero each cycle in discontinuous current mode and thus the ripple current magnitude \( \Delta I_{L(+)} \) is also the peak inductor current \( I_{pk} \). The inductor current decrease during the discharge state is given by:

\[
\Delta I_{L(-)} = \frac{(V_o + V_d + I_L R_L) - V_s}{L} T_{di}
\] (3.11)

As explained already for the continuous conduction mode case in steady state the current increase \( \Delta I_{L(+)} \) during the charge time and the current decrease during the discharge time \( \Delta I_{L(-)} \) are equal. Therefore these two equations can be equated and solved for \( V_o \):

\[
V_o = (V_s - I_L R_L) \left( 1 + \frac{T_{ch}}{T_{di}} \right) - V_d - I_L R_{DS,on} \left( \frac{T_{ch}}{T_{di}} \right) \] (3.12)

Now if we substitute \( T_{ch} = DT_s \) and \( T_{di} = D_2 T_s \) into the above equation we obtain:

\[
V_o = (V_s - I_L R_L) \left( 1 + \frac{D}{D_2} \right) - V_d - I_L R_{DS,on} \left( \frac{D}{D_2} \right)
\] (3.13)

Now we consider the output current. It is the average over the complete switching cycle of the inductor current during the \( D_2 \) interval.

\[
I_o = \frac{1}{T_s} \left[ \frac{1}{2} I_{peak} D_2 T_s \right]
\] (3.14)

Now if we substitute the relationship for \( I_{peak} (\Delta I_{L(+)} ) \) and \( T_{ch} - DT_s \) into the above equation we obtain:
\[ I_o = \frac{1}{T_s} \left[ \frac{1}{2} \left( \frac{V_s - I_L (R_L + R_{DS,on})}{L} DT_s \right) D_2 T_s \right] = \frac{[V_s - I_L (R_L + R_{DS,on})] D D_2 T_s}{2L} \]  

(3.15)

We now have two equations, one for the output current just derived, and one for the output voltage, both in terms of \( V_s \), \( D \), and \( D_2 \). Now we can solve each equation for \( D_2 \) and set the two equations equal to each other to eliminate \( D_2 \). The resulting equation can be used to derive an expression for the output voltage, \( V_o \). The discontinuous conduction mode boost voltage conversion relationship is given by:

\[ V_o = V_s - I_L R_L - V_d + \frac{[V_s - I_L (R_L + R_{DS,on})]^2}{2LI_o} \]  

(3.16)

For simplification of this derivation we assume that the dc resistance of the inductor, the output diode forward voltage drop, and the power MOSFET on state voltage drop are all small enough to neglect. Setting \( R_{DS,on} \), \( V_d \), and \( R_L \) to zero, the above equation simplifies considerably to:

\[ V_o = \left( 1 + \frac{V_s D^2 T_s}{2LI_o} \right) V_s \]  

(3.17)

The above relationship shows one of the differences between the continuous current mode and the discontinuous current mode. For continuous conduction mode, the voltage conversion relationship is a function of the duty cycle, input voltage, the inductance, switching time and output current; for continuous conduction mode, the voltage conversion relationship is only dependent on the duty cycle and the input voltage.

### 3.2.3 CCM vs DCM

The choice for continuous or discontinuous dependsents on the application. One of the differences is that in discontinuous current mode the energy after every cycle is zero in the inductor. Now to get the same average energy transfer the peak current is higher in discontinuous current mode. This is a disadvantage because higher current, e.g., higher losses in the switches and inductor. But there are also advantages. There is no energy after a clock cycle in the inductor, which leads to a more stable system. Also because the energy storage in the inductor is zero after every cycle we can faster react on variations in the output load. In discontinuous mode a smaller inductance is needed because the current slope must be higher for discontinuous conduction mode operation than for continuous conduction mode operation. When we consider the switches there are also some advantages of discontinuous current mode operation: because the current is zero while switching on, we don’t have the switch on losses in the switch. When we look to the conversion ratio for continuous current mode we see that this is only dependent on the duty cycle and ideally we can get as high gain as we want when we make the duty cycle around 1. But that’s not the case when take in account the resistance of the switches and the inductor. This can be shown by substitute Eq. 3.9 and \( I_o = \frac{V_o}{R} \) in Eq.
which leads to:

\[
V_o = \left[ \frac{V_s}{1-D} - V_d \right] \left[ \frac{1}{1 + \frac{R_L + D R_D S_{on}}{R(1-D)^2}} \right]
\]

We see that when \( D \) is high the losses in the inductor and the switch are big and that poses a limitation on the output voltage. When we consider the conversion ratio of discontinuous mode we cannot analyze it in the same way because Eq.3.9 is not valid for discontinuous current mode. But we can explain that the voltage can be very high in discontinuous mode from the fact that when the average energy to the load is lower than the average energy to the output of the converter that then there is an energy surplus that charges the capacitor which leads to an increasing voltage.

Advantages of Discontinuous Operation:

- A small inductor can be used because the average energy storage is low.
- Stability is easier to achieve because there no second pole in the input-to-output transfer function. Also, no right half-plane (RHP) zero appears since energy delivered to the output each cycle is directly proportional to the power transistor on-time (ton) for the discontinuous case[39].
- The output diode is operating at zero current just prior to becoming reverse biased. Therefore, reverse recovery requirements are not critical for this diode.
- The power transistor turns on to a current level which is initially zero, so its turn-on time is not critical and lower switching losses result.

But there also some disadvantages from the use of the discontinuous current mode:

- Transistor and diode peak current requirements are higher than they would be in a continuous mode design. Average current requirements remain unchanged.
- Without feedback the output voltage could be grow to dangerous high voltages that can break down the converter. This is because the converter charge the output capacitor but the capacitor is not discharged enough by the load in the charge phase, resulting in an increasing voltage.
- More losses in the resistors due to higher peak currents.

Because we want high conversion factor and small components we choose for constant operation in the discontinuous current mode.

### 3.3 Controller

In the previous section discontinuous current mode operation was chosen. In this section we will design the control of the boost converter such that it will always work in discontinuous current mode. To do this we define the conditions where the switches must switch on and off so that the converter works in discontinuous current mode. Switch \( S_1 \)
must switch on at the moment that the current is zero in the inductor and must switch off at the moment that the current in the inductor is $I_{peak}$. Switch $S_2$ must switch on at the moment that the voltage over switch $S_1$ is higher than the output voltage and must switch off at the moment that the current in the inductor is zero. The signals for the switches and the current in the inductor are plotted in Fig. 3.10. Now every cycle

![Diagram of signals in the converter]

**Figure 3.10: Signals in the converter**

an energy package is brought to the output and the amount of energy can be regulated by changing $I_{peak}$. But there is a problem when the output is not loaded or lightly loaded because then the boost converter brings more energy to the output than that there is used by the load and that leads to charging the capacitor and thus the voltage is a higher voltage. To overcome this problem we wish to turn off the boost converter when the voltage is growing higher than the voltage that we want. To determine this state the output voltage needs to be measured. To realize this control the current in the inductor must be sensed to define the various phases. And the output voltage need to be sensed for switching on and off the boost converter. There are different ways to measure the current and the voltage in a circuit. First we will consider measuring the current and then measuring the voltage.

### 3.3.1 Measuring the current

#### 3.3.1.1 Sense resistor

The current measurement can be done by inserting a resistance in the current path and then measure the voltage over the resistor [5, 8] as shown in Fig. 3.11. The current can determined using Ohm’s law $I = \frac{V}{R}$. A disadvantage of this method is that we lose energy in the resistor because $P = I^2R$. This energy loss can be reduced by using a low
resistance but small voltage changes are not easily measured, because then the accuracy is low because the voltage swing is then also lower with the same change in the current. Another disadvantage is that we can't place the resistor at the ground side of the source because there is a voltage drop over the resistor, which would make the source voltage of the switch higher and that makes it difficult to drive the switch. Thus the resistor must placed at the input and thus we must measure the voltage differentially because the input voltage can also vary and measuring a differential voltage is harder to design. Another disadvantage is that spread of the absolute resistance in our technology is relatively big and thus hard to measure the current accurately. The advantage of this current sensing method is that it is easy to implement.

### 3.3.1.2 Implement $R_{\text{sense}}$ with MOSFET

The on resistance of the switch can also be used as a sense resistor, by measuring the drain source voltage of the MOSFET as shown in [Fig. Variable output voltage DC DC converter with variable setting inductor current](a)[8]. When the switch is implemented with a nMOS transistor the equivalent resistance of the device is:

$$
R_{ds} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_t)}
$$

Where $\mu$ is the mobility, $C_{ox}$ is the oxide capacitance per unit area, $L$ and $W$ are the MOSFET length and width, and $V_t$ is the threshold voltage [7]. The advantage is that the switch is already in the circuit and does not lead to extra energy loss. The disadvantage is that the on resistance of the switch is changing over temperature and is inherently non linear, and not very accurate. This can be overcome by making the voltage reference also varying over temperature and non linear in the same way. This can be done by controlling a defined current to a second switch which is matched with the switch in the current pad see Fig.3.12(b). Because the on resistance of the second switch also varies...
over temperature and is inherently nonlinear the voltage is also varying but in the same way as the voltage over the switch in the current path. Thus when the voltage over both switches is the same the current through both switches is the same and because the current of the second switch is defined we can compare the voltages over both switches. One disadvantage is that we can only measure the current during the time that the switch is on.

3.3.1.3 Coupled inductor

Another method is to use a coupled inductor as shown in Fig.3.13[8]. Now the current

![Coupled inductor diagram](image)

Figure 3.13: Coupled inductor

is copied to the other inductor by the magnetic field and it can be used to measure the current through the first inductor without influencing the circuit. Disadvantage is that a inductor is bulky and now we must use two bulky inductors. The second disadvantage is that we can’t measure the dc current with this method, because a coupled inductor can only measure the change in magnetic field and thus only the change in current.

3.3.1.4 Current mirror

Another method is to copy the current through the switch $S_1$ as shown in Fig.3.14[26, 28, 12]. This can be done by using two of the same switches and keeping the voltage over

![Current mirror diagram](image)

Figure 3.14: Current mirror

it the same using the feedback topology as shown. Now the current through switch $S_1$ is copied to switch $S_3$ and we can measure the current through switch $S_3$ without loading the boost circuit. Disadvantage is that we can only measure the current during the time that switch $S_1$ is on and thus not the zero current state because in that state switch $S_1$ is open. Another disadvantage is that the switches must be well matched. Furthermore the voltage needs to be made the same and to do this accurately we need a fast op-amp that consumes energy. An advantage is low energy consumption because it is not in the
energy path and $I_{copy}$ can make a factor smaller by making the copy of the switch the same factor smaller.

### 3.3.1.5 Integrate voltage over the inductor

Also we can measure the voltage over the inductor:

$$V_L = L \frac{dI_L(t)}{dt}$$

Integrate this leads to

$$\int V_L = LI_L + C$$

where $C$ is a constant [8, 17]. Here we can see already the disadvantage that we must take into account the initial value otherwise we have an offset. Therefore we can only measure the change in the current and not the absolute value of the current. Also here the advantage is that the circuit is not in the energy path so that the energy loss can be made low.

### 3.3.1.6 Derivative of output voltage

There can also measure the derivative of the output voltage to measure the zero current. Because

$$I_C = C \frac{dV_C(t)}{dt}$$

and thus when $\frac{dV}{dt} = 0$ then the current is also zero. The disadvantage is that we only can measure the zero current state when the circuit is not loaded because then $I_C = I_L$. Advantage is that it is not directly in the energy path and thus the energy loss can be made low. Variable output voltage DC DC converter with variable setting inductor current

### 3.3.2 Zero current measuring

When switch $S2$ in fig. 3.1a) is implemented with a diode the voltage at the node between the inductor, the switch and the diode can be measured and determine the moment that the voltage is going from high to low. When the voltage is going from high to low the current is zero, because this is when the diode is turned off. That is at the moment that the switch node is going lower than the output voltage and that is at the moment that the current is zero in the inductor. Advantage is that it will not load the circuit when we measure with a high input resistance and thus not lose energy.

### 3.3.3 Measuring the output voltage

The output voltage will be measured by measuring the output node with a high input resistance because then it is not loading the circuit and no energy is lost.
3.3.4 Choice of the controller circuit

We want a high efficiency and thus low energy loss in the current sense circuit. Thus the sense resistor option is not a good option for this application. The size of the boost converter we also want to be small and because of this the coupled inductor is also not a good option. The current copier is a good option but this option needs a comparator and an op-amp that is fast enough to copy the current accurately. A fast op-amp needs more current and thus the option $R_{sense}$ with a MOSFET is more efficient because here we will only need a comparator. Thus we will choose for the $R_{sense}$ with a MOSFet option for measuring $I_{peak}$. But as explained before we can use this only during the time that the switch is on thus we need another circuit for the detection of zero current. For this we will choose for the option of comparing the switching node voltage with the output node voltage because this is easier and requires less energy than measuring the derivative of the output voltage. The output voltage we will measure directly because measuring a voltage at a node does not load the circuit when using a high input resistance. The schematic of the system level design is plot in Fig. 3.15.

![Schematic of system level design](image_url)

Figure 3.15: schematic of system level design
4 Circuit design of the inductive converter

In the previous chapter we have designed the DC-DC converter and controller in system blocks. In this chapter we will implement the different system blocks on transistor level. In the first part of this chapter we will talk about the inductor, switch and capacitor selection. In the last part of this chapter we will talk about the controller of the DC-DC converter that is needed for a good working of the converter.

4.1 Boost converter Components

4.1.1 Inductor

The inductor is an important component in the boost converter because that’s the component in which we will store the required energy. To store the energy in an efficient way we have seen in the previous chapter that we need a low resistance. Thus a requirement for the inductor is that it must have a low series resistance and low core losses. Another requirement is that we must to minimize the size of the components. We want a high voltage at the output with a low voltage at the input. This leads to a high current at the input thus we must also take in account that the inductor will not saturate due to the high current and switching frequency. To determine the value of the inductor we analyze the maximum inductor value for which that the converter still works in the discontinuous mode. This analyze will be based on [7].

When the diode conducts, its current equals to the inductor current. As can be seen from Fig. 3.2(b), the minimum value of the inductor current during the diode conduction subinterval $DT_s < t < T_s$ is $I_{L(\text{AVG})} = \frac{\Delta I_L}{2}$ If this minimum current is positive, then the diode is forward-biased for the entire subinterval and the converter operates in the continuous conduction mode. So the condition for operation of the boost converter in the continuous conduction mode is:

$$I_{L(\text{AVG})} > \frac{\Delta I_L}{2} \quad (4.1)$$

And the condition for operation of the boost converter in the discontinuous conduction mode is:

$$I_{L(\text{AVG})} < \frac{\Delta I_L}{2} \quad (4.2)$$

Substitution of the discontinuous conduction mode solution for $I_{L(\text{AVG})}$ Eq. 3.9 and $\Delta I_L$ Eq. 3.10 yields for the discontinuous conduction mode:

$$\frac{I_o}{(1-D)} < \frac{DT_sV_i}{2L} \quad (4.3)$$

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This equation can be rearranged to obtain

\[
\frac{I_o 2L}{T_s V_i} < D(1 - D)
\]  \hspace{1cm} (4.4)

This can also be expressed as

\[
K < K_{\text{crit}}(D)
\]  \hspace{1cm} (4.5)

where

\[
K = \frac{I_o 2L}{T_s V_i} \quad \text{and} \quad K_{\text{crit}}(D) = D(1 - D)
\]  \hspace{1cm} (4.6)

The dimensionless parameter \( K \) is a measure of the tendency of a converter to operate in the discontinuous conduction mode. Large values of \( K \) lead to continuous mode operation, while small values lead to the discontinuous mode for some values of duty cycle \( D \). The dependence of \( K_{\text{crit}}(D) \) on the duty cycle \( D \) is plotted in Fig. 4.1. An arbitrary choice of \( K \) is also illustrated. \( K_{\text{crit}}(D) \) is zero at \( D = 0 \) and at \( D = 1 \), and has a maximum value of \( \frac{1}{4} \) at \( D = \frac{1}{2} \). Hence, if \( K \) is greater than \( \frac{1}{4} \), then the converter operates in continuous conduction mode for all \( D \). Fig. 4.1 illustrates what happens when \( K \) is less than \( \frac{1}{4} \). The converter then operates in the discontinuous conduction mode for some intermediate range of values of \( D \) near \( D = \frac{1}{2} \). But the converter operates in the continuous conduction mode near \( D = 0 \) and \( D = 1 \). It is natural to express the mode boundary in terms of the load current \( I_o \), rather than the dimensionless parameter \( K \).

Equation 4.4 can be rearranged to directly expose the dependence of the mode boundary on the load current:

\[
I_o < I_{\text{crit}}(D)
\]  \hspace{1cm} (4.7)

where

\[
I_{\text{crit}}(D) = \frac{T_s V_i D(D - 1)}{2L}
\]  \hspace{1cm} (4.8)

---

![Figure 4.1: \( K_{\text{crit}} \) and \( K \) vs \( D \)](image_url)

---

50
For the inductor selection we must solve \( L \) such that eq. 4.8 is satisfied so that the converter works in the discontinuous mode. The worst case condition for the boost power stage (given the lowest \( L_{\text{max}} \)) is at the duty cycle where \( D(D - 1) \) is the lowest.

\[
I_{\text{max}} < \frac{T_s V_i D(D - 1)}{2 I_{\text{crit}}}
\]  
(4.9)

Now we calculate \( L_{\text{max}} \) from the specification values from the introduction chapter \( T_s = 2\mu s, V_i = 3.3V, I_{\text{crit}} = 20mA \) and \( D = 0.82 \) by using Eq. 3.7 with \( V_o = 18V \) we get 24\( \mu \)H. By using an inductor value lower than just calculated ensures discontinuous conduction mode operation for output load currents below the critical current level, \( I_{\text{crit}} \).

From Eqn 4.9, it can be inferred that

- the more the output current, the smaller energy storing elements are required to ensure discontinuous mode operation.
- decreasing the switching time (increasing the operation frequency) requires a lower inductor value to ensure discontinuous current mode.

Thus we must take an off-chip inductor with the requirements that the inductor is small and can handle a peak current of \( \frac{2 I_{\text{crit}}}{1-D} = \frac{20mA}{1-0.82} = 222 \text{ mA} \). To keep some margin we chose 300mA, a frequency of 2 MHz and an average current of \( \frac{I_{\text{peak}}}{2} = 150mA \) with a value of 18uH without saturation or overheating.

We have chosen for an inductor from Coilcraft because they have spice models for the inductors so that we can simulate how the coil behaves in the converter. Coilcraft has a lot of inductors thus we need to select an inductor that meets our specifications. Because we want a small inductor we look at the dimensions of the inductor and because we also want a efficient converter we look into the losses of the inductor. For the losses coilcraft has a tool on its website where we can fill in the frequency and the currents of operation and then the tool calculates the losses of the inductor so that we can compare different inductors. We have selected four inductors dimensions: the MSS5131, MSS6122, MSS6132, MSS7341. We then filled in the required information in the tool. From the tool we see that the MSS7341-183 has the lowest losses thus we have chosen this inductor.

For the inductor in the simulation we use the model of the Coilcraft website. See Fig. 4.2. Their values are given in Table 4.1 under \( Z_{in1} \), \( f \) is frequency. Because some values depend on the frequency there was a problem with this model to simulate it in Cadence. Thus we have converted the model to a model without the dependence of frequencies in the components. See \( Z_{in2} \) in Table 4.1. We also added an ideal inductor \( Z_{in3} \) to Table 4.1. The values of the components we have obtained by doing simulations in ADS because this program can handle simulations with components that are dependent on frequency. We have fine-tuned the values by comparing the Bode plots till the moment that they are the same. The magnitude frequency plot is plotted in fig.4.3. The phase plot is plotted in fig. 4.4. This new model we use in Cadence for the simulations of the converter.
4.1.2 The switches

4.1.2.1 Losses in the switch

The power losses in the DC-DC converter can be subdivided roughly into three types: conduction loss, switching loss, and quiescent operating power loss. Conduction loss is caused by the non-zero on-resistance of power switches, which introduces power loss due to current flowing through the switch during on-time. The total conduction loss of a switching converter also includes the loss by the equivalent series resistance (ESR_L) of the inductor, equivalent series resistance (ESR_C) of the output capacitor, and series resistance of wires.

Switching loss comes from the overlap of voltage drop over the switch and the current through the switch at moment that the switch is switching on or off, as depicted in Fig. 4.5. This phenomenon comes from the fact that the switch is not directly high-ohmic (switching off) or low-ohmic (switching on) while switching but it takes time to go from high-ohmic to low-ohmic and vice versa. The power loss is the current times the voltage. Another type of switching loss originals from gatedrivers responsible for charging and discharging the parasitic gate capacitor of the power switches.

Quiescent operating power loss is caused by static power needed to keep the control circuitry working. Contributions of conduction loss and switching loss become dominant at high load operation but quiescent operating power loss and switching loss become
dominant at small loads.

4.1.2.2 Switching losses

Zero-Current Switching (ZCS) and Zero-Voltage Switching (ZVS) are methods to reduce switching loss [7]. With ZCS, a switch should be turned on and off when the current through the switch is zero. And with ZVS, a switch should be turned on and off when the voltage over the switch is zero. ZCS is invented to avoid the problem that at the moment that the switch is turned on the voltage is not directly zero and thus we lose energy in the switch, and while switching off is the problem that the current through the switch is not directly zero. These problems are shown in Fig. 4.5. As we switch on the switch when the current in the inductor is zero we don’t lose energy by switching on the switch but we have still the loss when switching off the switch.
4.1.2.3 Conduction losses

As mentioned above, at large load the conduction loss and switching loss (or gate-drive loss) are the fundamental contributions to power dissipation. In the field of microelectronics, the ability to dimension and freely design the transistor is an advantage. Because now we can get the best compromise between switching and resistive losses. By carefully choosing the size of the transistor an optimum balance between these two kinds of losses can be found. Because the parasitic capacitance is bigger when we make the transistor bigger but the resistance of the switch is lower when we make the switch wider. By sizing a MOSFET the principal objective is to minimize the sum of the dissipation due to these two mechanisms. Since the power transistors conduct in the triode region, with \((V_{DS} \ll V_{GS} - V_t)\), the device channel resistance is given by:

\[
r_{ds} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_t)}
\]  

(4.10)

While the minimum length \(L\) of the power switches is always chosen, the width can not be increased to infinite in an effort to eliminate switch conduction loss, because the increase of the width results in a remarkable increase of conduction gate capacitance,
which, in turn, increases switching loss. Apparently, there exists an optimum width W for a power MOSFET used as a switch.

### 4.1.3 Switch S1

This switch is used for charging the inductor. To charge the inductor with low loss we have seen in the second chapter that we need a low resistance. Switch S1 can be implemented in different ways. The IC technology is B3T25 (a 0.35μm technology) of On Semiconductor.

The next choice is between nMOS and pMOS. The source is connected to the negative supply thus for a pMOS a negative value would be needed and a nMOS is easier to drive because the gate voltage must be vt higher than the source. Thus there will be chosen for nMOS because the reason that a nMOS is easier to drive.

Now there are many nMOS transistors in the technology thus the next choice will be to figure out which one is the best. Because the drain voltage can be as high as 18 volt by switching the switch off the transistor must not break down at this voltage. That’s the reason that the high voltage nMOS transistor will be chosen because the other transistors break down due to the 18 volt.

For the length of the switch a minimum length is chosen because we want a small resistance and a small switch for holding the parasitic capacitance low. The width we can not make too big because of the parasitic capacitance and the area and not too small because we want a low $R_{DS, on}$ as stated before.

Because the frequency and currents are changing by changing $I_{peak}$ it is hard to calculate an optimum for the size of the switch mathematically. Thus we have swept the width of the transistor for different $I_{peak}$, so that we can see where the optimum is for various $I_{peak}$s. The result is plotted in Fig.4.6. The controller is also not ideal and this is the reason that the efficiency is already lower because the static power loss in the controller. We can see that for lower $I_{peak}$ the optimum is for a lower width of the transistor. This can be explained by the fact that the frequency is higher for lower $I_{peak}$ and thus the parasitic capacitance has a bigger influence on the total efficiency and the $I_{peak}$ is lower thus the conduction losses by the $R_{DS, on}$ are lower. And that the efficiency is higher for higher $I_{peak}$ can be explained by the fact that the used energy is higher but
the energy for the controller is almost the same thus the efficiency is higher. We have chosen for 5000\(\mu m\) because this is the optimum for the lower \(I_{\text{peak}}\) and for the higher \(I_{\text{peak}}\) by doubling the size of the transistor we get only a 2\% higher efficiency.

### 4.1.4 Switch S2

This switch will be used for discharging the inductor to the output. This switch can be implemented with a pMOS or nMOS but also with a diode. This switch must turn on when the voltage over switch \(S_1\) is higher than the output voltage and close when the voltage over switch \(S_1\) is lower than the output voltage. This is exactly what a diode does. Thus the control of the diode is easy because it controls itself.

For a nMOS implementation there will be a problem with switching on because the gate must be made higher than the source voltage. That’s a problem because we want to switch the highest voltage in the chip.

A pMOS implementation can be chosen because to switch a pMOS on the gate must be made lower than the source voltage. This can be done, but the high voltage pMOS transistor gate source voltage can only be 3.3V, otherwise the transistor will break down. Thus there must be made a level shifter to control the pMOS switch. Also there must
be made a control signal for the pMOS switch.

Because of the easy implementation and control we will choose a diode implementation. Next we need to decide which diode we want to use. There are many diodes in the technology. The diode must not break down by a reverse bias voltage of 18 volt and must have a low forward bias voltage because then we have lower losses in the diode. Also it must switch on quickly because otherwise there can arise a high voltage over the nMOS switch. Because of these specifications a schottky diode will be selected because this one has low forward bias voltage and can switch very fast and can handle a reverse bias voltage of 18V.

The dimension of the diode is determined by the current. The current that must be handled is 500mA and we want some margin thus it must handle 800mA.

**4.1.5 Capacitor**

The capacitor is used to deliver energy to the output at the moment that the inductor is charging. The value of the capacitor is directly related to the peak-peak voltage ripple (Vpp) of the output voltage. The voltage ripple is the voltage drop during the time that the inductor is charging and can be calculated from:

\[
V_{pp} = \frac{I_o DT_s}{C_{min}} \tag{4.11}
\]

Hence, \( C_{min} \) becomes:

\[
C_{min} = \frac{I_o DT_s}{V_{pp}} \tag{4.12}
\]

From Eqn. 4.12, it can be inferred that

- Increasing the capacitance value decreases the output voltage ripple.

- The minimum capacitance required reduces with increasing switching frequency.

The start-up time is also influenced by the output capacitor value because there is a constant amount of energy bring to the output capacitor by discharging the inductor every cycle. What charge the capacitor and let grow the output voltage. The bigger the capacitor the slower voltage increases and thus a longer start-up time \( t_{\text{start-up}} \).

\[
t_{\text{start-up}} = \frac{V_{out}C_{out}}{I_{AVG}}
\]

The output voltage is plotted for different output capacitors in Fig. 4.7. In this figure we can see that for a smaller output capacitor the converter output voltage is increasing faster. We can also see in the figure that the output voltage ripple is bigger for a smaller output capacitor. We have chosen for an output capacitor of 330mF because the output voltage was fast enough reached and has a small output voltage ripple and this capacitor value is available in a small package.
Figure 4.7: $V_o$ for a sweep over $C_{out}$ (100$nF$ to 500$nF$)

4.2 Controller

The schematic of the controller is shown in Fig. 4.8. For sensing the peak current through the inductor ($I_{peak}$) the $R_{sense}$ has been implemented with a MOSFET and for the reference a matched MOSFET as shown in Fig. 4.8 because it is easy and offers low energy loss as was explained in the previous chapter. Switch $S_3$ is also implemented with the same high voltage nMOS as switch $S_1$ for the matching of the two switches. The source of switch $S_3$ is also connected to ground and the gate to $V_g$ so that the source and gate voltages are also the same as those for switch $S_1$. Because we want low energy loss in the controller circuit we chose a 1000 times smaller width for the reference nMOS transistor because then the current through the nMOS transistor can also be 1000 times smaller. See eq. 4.10 thus yielding a 1000 times smaller energy loss. Now the voltages of both transistors need to be compared. And for this comparison we use a comparator see Fig. 4.8.
4.2.1 The $I_{\text{peak}}$ detector

We choose a 3 stage comparator with a pseudo-differential input stage, a differential pair and an output stage. We want to implement the comparator with low voltage transistors because low voltage transistors are smaller than high voltage transistors. When we do this we have a problem because the node between the switches and the inductor is at a high voltage at the moment that the inductor is discharging thus we must switch this node off from the comparator input when the voltage increases to a voltage that is too high. Because we must do this we can use this time to compensate for the offset in the comparator. We do this by connecting the output of the comparator to the negative input of the comparator and switch a capacitor between the negative output and the reference voltages as shown in Fig. 4.9. Furthermore, we connect a reference voltage to the positive input[20]. During first phase, because the gain of the op amp the voltage on the negative node is made the same as the voltage on the positive node plus the offset of the op-amp, the capacitor is charged with the offset voltage of the op-amp.

During the next phase the negative input of the comparator is connected to the capacitor in series with the switch voltage and the reference voltage is connected to the positive input. Now the voltage at the negative input of the comparator is the voltage over the switch minus the offset voltage of the comparator. In this way the offset is compensated.

Because the voltages over switches $S_1$ and $S_3$ are low the voltages on the input of the
comparator are low thus we want to implement its input stage with pMOS transistors. See Fig. 4.10 the transistors $M_1$ and $M_2$ are the input transistors. And the output must track the input when we switch the comparator as a voltage follower, thus this voltage will also be low. For this reason we want to implement the output transistor $M_7$, also with a pMOS. For the matching of the transistors $M_5, M_6$ and $M_7$ we will also implement transistors $M_5$ and $M_6$ with pMOS. And thus the differential pair will be implemented with nMOS (transistors $M_3$ and $M_4$). The bias currents are chosen such that the transistors are all in saturation and as low as possible so that the comparator does not burn too much power. But the bias current cannot be chosen too small because otherwise the comparator will be too slow to detect the $I_{peak}$ accurately. The dimensions of the transistors are summarized in Table 4.2.

![Comparator topology for the $I_{peak}$ detection](image)

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Width($\mu m$)</th>
<th>Length($\mu m$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_1$</td>
<td>1</td>
<td>0.35</td>
</tr>
<tr>
<td>$M_2$</td>
<td>1</td>
<td>0.35</td>
</tr>
<tr>
<td>$M_3$</td>
<td>6</td>
<td>0.35</td>
</tr>
<tr>
<td>$M_4$</td>
<td>6</td>
<td>0.35</td>
</tr>
<tr>
<td>$M_5$</td>
<td>6</td>
<td>0.35</td>
</tr>
<tr>
<td>$M_6$</td>
<td>6</td>
<td>0.35</td>
</tr>
<tr>
<td>$M_7$</td>
<td>4.7</td>
<td>0.35</td>
</tr>
<tr>
<td>$M_8$</td>
<td>3</td>
<td>0.35</td>
</tr>
<tr>
<td>$M_9$</td>
<td>3</td>
<td>0.35</td>
</tr>
<tr>
<td>$M_{10}$</td>
<td>2</td>
<td>0.35</td>
</tr>
<tr>
<td>$M_{11}$</td>
<td>2</td>
<td>0.35</td>
</tr>
</tbody>
</table>

Table 4.2: Dimensions of the transistors in the $I_{peak}$ detector

Because the comparator could be unstable when we switch it in op-amp mode we analyze the gain margin and the phase margin over the input voltage. This is plotted in...
Fig. 4.11.

![Graph showing phase margin and gain margin as a function of V<sub>ref</sub> (10mV to 400mV)](image)

Figure 4.11: Phase and gain margin as a function of V<sub>ref</sub> (10mV to 400mV)

We can see in the plot that the phase margin over the input range is always greater than 54 degrees and the gain margin over the input range is always greater than 35 dB. And thus we can consider the op-amp with feedback to be a stable system.

4.2.2 The <i>I</i><sub>peak</sub> reference voltage

For the <i>I</i><sub>peak</sub> reference voltage we use the voltage over a matched high voltage nMOS transistor, through which we steer a defined current so that, because of the R<sub>on</sub> of the transistor, we get a voltage over the transistor as explained in the previous chapter. The defined current is from an ideal current source. To make the current source more realistic we copy the current from the current source through the nMOS transistor by using a cascode current mirror. We use a cascode current mirror because the cascode current mirror can copy the current better than a normal current mirror. We want a good copy of the current because every mismatch in the current leads to a direct mismatch in the voltage reference. Thus the sizes of the transistors in the current mirror we choose such that the transistors are also well matched and have low channel length modulation, thus
bigger size and longer length. Hence, the current through the nMOS transistor is almost the same as the current from the current source.

4.2.3 Zero current detector

For the zero current detection we will compare the voltage over switch $S_1$ with the output voltage. See Fig. 4.8. But we can not directly compare the voltage by means of a comparator because the gate source voltage of the transistors cannot handle voltages higher than 3.3V. Thus the voltage of the switching node must be converted to a lower voltage. This can be easily done by resistors with a well defined relationship but the disadvantage is that there is always a current flowing through the resistors. To reduce the energy loss we can make the total resistance larger but we can’t make the resistors too large because we want to implement it on chip and big resistance takes a lot of chip area. Thus this is not a good option for this application.

We might consider implementing the voltage divider by means of capacitors with a defined ratio that can also make a division of the voltage. A disadvantage of using capacitors is that they do not pass dc. Thus because of leakage current the capacitors can have offset in the division. To overcome this problem the voltage between the two capacitors is shorted to ground at the moment that the switch $S_1$ is on. This is shown in Fig. 4.12. At the moment that switch $S_1$ is on the voltage over the switch is low

![Figure 4.12: switch node voltage divider](image)

and thus when we short the lower capacitor it is discharged and has no offset during the following cycle.

For the output voltage sensing circuit there is the same problem as with the switching node voltage that the gate source voltage of the mos transistors cannot be higher than 3.3V otherwise they are will break down. Thus the output voltage must also be divided to make the output voltage lower. This division we will also implement by capacitors. To overcome the dc problem we can’t do it in the same way as with the switching node because the output voltage is constant and not every cycle going to a lower voltage thus we must do it in another way. We can short both capacitors to ground as shown in Fig.4.13(b). But when we look to the implementation of switch $S_6$ there is a problem because this switch will switch from the high $V_{out}$ and when we implement this switch with a nMOS we need a gate voltage 3.3volt lower than $V_{out}$ and to make this we burn
extra energy. There is also another disadvantage with this method because during the time that we switch the capacitors to ground we can’t measure the output voltage.

Another method is sampling with a resistive divider. This will be done by making a resistive divider and connect this to the voltage divider for a short time as shown in Fig. 4.14. The resistors of this divider could be smaller leading to smaller area but they will burn more energy. However, because the divider will only be loaded by two comparators and thus the leakage current will be low, it can track the output voltage accurately for a long time and we only need to sample for a short time. Thus the resistors burn energy only for a short while. We must ensure that the voltage on resistance of the switch is low because this leads also to a offset in the resistive divider. Switch $S_4$ we have implemented with a high voltage nMOS transistor ($M_1$) because the voltage over this switch is $V_{out}$ at the moment that the switch is open. Switch $S_5$ we have implemented with a high voltage nMOS transistor ($M_2$) with a low voltage nMOS transistor ($M_4$) in series at the side of the capacitors and between the two transistors a low voltage pMOS transistor ($M_5$) with the other terminal to $V_{dd}$ as shown in Fig. 4.15. Transistors $M_2$ and $M_4$ are minimum size to keep the area low and to keep the charge injection from $M_4$ to the capacitors low. Transistor $M_3$ is used so that the transistors switch off fast.

The capacitors are implemented using MIM capacitors with a finger length of 20µm and 10 fingers and 90 fingers respectively. The resistors are implemented as hi-poly
resistors with a width of 2\( \mu m \) and 20 and 180 numbers of squares.

Now by comparing the divided output voltage with the divided switching node voltage we can detect the moment that the signal is going from high to low. For this comparator we use a pMOS differential pair (transistors \( M_1 \) and \( M_2 \)) see Fig. 4.16 for the input. Because the voltages will be low. For good matching of transistors \( M_3 \), \( M_4 \) and \( M_5 \) so that we have low offset we choose an nMOS output stage (transistor \( M_3 \)) as also shown in Fig. 4.16. The bias currents are chosen such that the transistors are all in saturation and so low as possible so that the comparator does not burn too much power. But the bias current can’t chosen too small because otherwise the comparator will be too slow to detect the zero current accurately. The dimensions of the transistors are summarized in Table. 4.2. We use this comparator to compare the output voltage with the voltage over the switch. The output of the comparator is high when the voltage over the switch is lower than the output voltage. And when the voltage over the switch is larger than the
<table>
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<th>Transistor</th>
<th>width(μm)</th>
<th>length(μm)</th>
<th>Transistor</th>
<th>width(μm)</th>
<th>length(μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_1$</td>
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<td>1</td>
<td>$M_5$</td>
<td>3</td>
<td>1</td>
</tr>
<tr>
<td>$M_2$</td>
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<td>1</td>
<td>$M_6$</td>
<td>4*4</td>
<td>1</td>
</tr>
<tr>
<td>$M_3$</td>
<td>3</td>
<td>1</td>
<td>$M_7$</td>
<td>2*4</td>
<td>1</td>
</tr>
<tr>
<td>$M_4$</td>
<td>3</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 4.3: Dimensions of the transistors in the zero current detector

output voltage the output signal of the comparator is going low. Now at the moment that the signal from the comparator is going from low to high is at the moment when the diode goes from forward biased to reverse biased and that is also the moment that the current is zero in the inductor.

4.2.4 Output voltage detector

For the comparison of the output voltage with the reference voltage see Fig.4.8 we use the same comparator topology and same dimensions of the transistors as is used for the zero current detection (Fig.4.16). The output of the comparator will be high when the output voltage is smaller than the reference voltage. And low when the output voltage is larger than the reference voltage. With this signal we can switch the converter on and off.

4.2.5 Clock driver

For the driver of the power MOSFET we choose a simple inverter topology. But we design it not so that the inverter switch in the same speed to the low voltage as to the high voltage because the switch can be slowly turned on but must have fast turn off. This is because the fact that we switch the switch on when the current is zero and thus we don’t need to switch it on fast. Because we turn the switch slowly on we can design the pMOS of the inverter a lot smaller, which leads to a lower gate capacitance of the pMOS transistor and thus lower losses for every switching cycle because we need to charge and discharge every cycle a lower capacitance. By designing the driver to be asymmetrical we make it also faster because the AND gate that drives the inverter needs to charge a lower capacitance.

4.2.6 Logic

The timing of the different circuits and the clock generation is done by a logic circuit. This logic circuit is shown in fig 4.17. To guarantee the correct signal from the $I_{peak}$ detector we need to insert a delay in the signal, because at the moment that we switch from op-amp mode to comparator mode there could become a wrong signal from the $I_{peak}$ detector on the flip-flop. This signal will otherwise set the flip-flop directly. To overcome this problem a second clock signal is introduced is delayed from the clock signal. This is shown in Fig 4.17. To make the delay for the second clock we have used
two inverters where the first inverter is minimum size, so that this inverter is minimally loading the clock signal. The second inverter is a lot bigger so that it gets a delay. The delayed clock signal is connected to an “AND” port together with the signal from the $I_{peak}$ detector so that the signal from the detector is only connected to the flip-flop after the delay. The time of the delay must be made as long as the detector needs to come in its comparator mode.

The flip-flop we have built up with two NOR ports, so we must take care of that the two input signals are not both high as then the output is not defined. Thus we will only need a short pulse from the zero current detector. To make a short pulse we invert the signal from the zero current detector with a delay and connect the normal and delayed inverted signal to an “AND” port as shown in Fig.4.17. Now there is a short pulse when the signal from the zero current detector is going from low to high. We can make the pulse longer by making the delay of the inverted signal longer.

The clock signal to the nMOS will only be present at the moment that the output voltage is lower than the reference voltage. We will also make the whole charge and discharge cycle such that the converter can’t oscillate and will work efficiently. This we do by connecting the output signal of the output voltage detector to an “OR” port and at the other input of the “OR” port we connect an “AND” port with the signals from the flip-flops as shown in Fig. 4.17. The “AND” port is used so that the D flip-flop only detects when the clock is low so that we always make the whole charge and discharge cycle. And the D flip-flop is feedback so that we have a short pulse on the “OR” port and thus the voltage detector can set the signal when the output voltage is falling down under the voltage that we want. The output of the D flip-flop is connected to a “NAND” port together with the output from the RS flip-flop as shown in Fig 4.17. Hence, the clock signal to the nMOS can be high only when the output voltage is lower than the reference voltage. As a consequence, the boost converter is only on when the output voltage is lower than the reference voltage.

In fig 4.18 is the whole circuit shown on transistor level.
Figure 4.18: Schematic of the whole circuit on transistor level
5 Simulation results

In this chapter we will discuss the simulation results of the converter to prove the correct functionality and to find the performance of the circuit. We have done this with circuit simulations in the Cadence design environment using the Spectre simulator. The models for the On Semiconductor I3T25 (High voltage 0.35μ) technology used are version Rev4.0

5.1 The circuit

![Graph showing transient plot of output voltage V_o from zero initial conditions. The reference voltage is from 6V to 17V. The peak current in the inductor I_{peak} is set to 200mA. At t=1.3ms the stimulation pulse is activated and lasts until 1.55ms.](image)

Figure 5.1: Transient plot of the output voltage $V_o$ from zero initial conditions. The reference voltage is from 6V to 17V. The peak current in the inductor $I_{peak}$ is set to 200mA. At $t=1.3$ms the stimulation pulse is activated and lasts until 1.55ms.
In Fig. 5.1 we have plotted a sweep of the output voltage as a function of time for various reference output voltages and we can see in this plot that the output voltage can be varied. When the output voltage reaches the reference voltage the converter switches off. The moment the voltage falls under the reference value, the converter is switched back on. The minimum voltage at the output is 3.3V. This due to the input voltage and the conversion topology chosen. The maximum voltage of the output is 18 Volt this comes from the technology.

At 1.3 ms we switch on a load current of 1 mA and switch off the load current at 1.55 ms to simulate a stimulation cycle. We can see that the converter holds the output voltage at the set output voltage. We see also that the ripple for lower voltages is bigger than for higher voltages. This can be explained by the fact that the average current due to the time required for discharge of the inductor for one charging cycle to the output is lower for higher voltages than for lower voltages. And a higher average current to the same capacitive load leads to a higher voltage ripple.

When we look into the efficiency defined as $\eta = \frac{\int (I_{\text{input}} \cdot V_{\text{input}}) dt}{\int (I_{\text{output}} \cdot V_{\text{output}}) dt} \cdot 100\%$, where the whole cycle (2 ms) in fig. 5.1 is taken for the integral time, the efficiency of charging the output capacitor from zero initial conditions and one stimulation cycle plot in Fig. 5.2.
Figure 5.2: Efficiency for the output voltage $V_o$ over the range of 6V to 17V. The peak current in the inductor $I_{peak}$ is set at $I_{peak}$ (200mA).

From Fig. 5.2 we can deduce that the efficiency is greater than 80% for all values of the output voltage. $\eta$ is lower for higher output voltages because it is charging longer with the same peak current in the inductor.
Figure 5.3: Plot of the current in the inductor $I_L$ over time for different settings of the peak current in the inductor $I_{peak}$.

In Fig. 5.3 we have plotted the current through the inductor for different values of the peak current, $I_{peak}$. We can see that the current through the inductor rises until the moment that the current reaches the value of $I_{peak}$. At the moment that the current through the inductor reaches $I_{peak}$, switch S1 (Fig. 4.8) is switched off and the current falls down to zero. Thus the $I_{peak}$ detector works well. When the current reaches zero switch S1 is switched on again. Thus the zero current detector works also well. After reaching the zero current the charging cycle starts again.
Figure 5.4: Plot of the current in inductor $I_L$ for one charging cycle of the converter, with a sweep over the offset voltage $V_{offset}$ ($-100mV$ to $100mV$) on the input of the $I_{peak}$ detector.

To verify whether the offset cancellation of the current sense circuit works properly, we have put a voltage source in series with one of the inputs of the peak detector. See Fig 4.10. We sweep the voltage of the voltage source from $-100mV$ until $+100mV$ (variation of $\pm100\%$). We observe the current through the inductor and monitor the variation of the moment at which the switch is turned off. In Fig. 5.4 we have plotted the results. We see that the peak currents are almost the same. This is shown in Fig. 5.5 where the plot of fig. 5.4 is zoomed in.
conduction

Figure 5.5: Zoom in of the previous plot at the peak of the current through the inductor

In Fig. 5.5, we see that the inductor current only changes by 50uA (variation of 0.05%) over the full sweep. Hence the offset cancellation works properly. In the next section we will consider what of the input variations.
5.2 Input variations

![Graph showing inductor current $I_L$ vs. time with different input voltages $V_i$ (1.8V to 3.3V). The peak current in the inductor $I_{peak}$ is set to 100mA.]

Figure 5.6: Plot of the inductor current $I_L$ for one charging cycle, with a sweep over the input voltage $V_i$ (1.8V to 3.3V). The peak current in the inductor $I_{peak}$ is set to 100mA.

In Fig. 5.6 we have plotted the current through the inductor. In this plot we have swept the input voltage over the range 1.8-3.3V. The voltage can’t be higher than 3.3V because the gate voltage of the transistors cannot be higher as otherwise breakdown occurs. 1.8V is the minimum because otherwise some transistors will go out of saturation in the circuit. In this plot we can see that the slope of the current is changing for different input voltages. This can be explained by the fact that the slope $\frac{di}{dt} = \frac{V_i}{L}$ thus when $V_i$ is smaller the slope will be also smaller. In this plot we can also see that the peak of the current $I_{peak}$ is not changing (it was set at 100mA) and thus that the peak current detector works well over the input voltage range 1.8-3.3V. We also see that the converter is reset at zero current and thus the zero current detector works also well over this range.
Figure 5.7: Plot of the efficiency of the converter versus the input resistance $R_{in}$. With a sweep over the peak current in the inductor $I_{peak}$ (50mA to 200mA).

In Fig. 5.7 we have plotted the efficiency versus the source resistance of the input voltage source. The efficiency is taken the same as in section 5.1 but there was the input resistance 1 ohm because of the model of the inductor. We can see that the efficiency is highest for lower source resistances. The efficiency has a linear relation with $R$. This can be explained by the fact that $P = I^2R$ and thus the bigger the $R$, the more power is dissipated in the resistor, which results in a lower efficiency.

We can also explain by the same fact that the efficiency is highest for lower currents, because the bigger the current through the resistor the bigger the loss in the resistor.

But because of the static contribution of the biasing and controller system this is not with the lower current peaks. Because the energy consumption of the controller and biasing circuit is constant and the energy delivered to the output is more for higher current the energy consumption of the controller is more important for lower currents and thus the efficiency will be lower. In the next section we look into the effects of load variations.
5.3 Load variations

![Plot of output voltage $V_o$ at start-up and over one stimulation cycle, with a sweep over the stimulation current $I_o$ (1mA to 20mA). The peak current in the inductor $I_{peak} = 100mA$.](image-url)

In the plot of Fig. 5.8 the output voltage for different loading currents $I_o$ has been depicted. For this plot we have used a current pulse because the stimulator will also consume a pulsating current. The current pulse is enabled at the load at 1.3ms and is switched off at 1.55ms. The peak current in the inductor ($I_{peak}$) has been set at 100mA. From this plot we can see that for higher output currents the converter brings not enough energy to the output what results in discharging the capacitor. After switching off the current pulse we see that the converter charges again the output capacitor to the correct output voltage. From this plot we can also see that the converter switches off at the moment that the output voltage reaches the correct voltage again. Thus the circuit that must switch off the converter works well.
Figure 5.9: Plot of output voltage $V_o$ at start-up and over one stimulation cycle, with a sweep over the stimulation current $I_o$ (1mA to 20mA). The peak current in the inductor $I_{peak} = 300mA$.

In Fig. 5.9 we have also plotted the output voltage and load the output with different output loading currents but with a difference with respect to the plot before that the peak current is now set to 300mA. In Fig. 5.10 we have zoomed in on the plot of Fig. 5.9. We can see that the converter now brings enough energy to the output because the output capacitor is not discharged too much (10%). This results in that the output voltage does not fall down to a low voltage.
Figure 5.10: Zoomed in on the stimulation cycle of the previous plot.

Increasing the value of $I_{\text{Peak}}$ has disadvantages. The ripple on the output voltage for lower output load current is bigger than in the plot of Fig. 5.8. This is because the current peak is higher thus every cycle there is more current delivered to and taken away from the output capacitor, which results in a higher voltage ripple.

Increasing $I_{\text{Peak}}$ means also the efficiency will drop at lower output loads, because there is more energy loss in the parasitics.

In the next section we will look into the influence of temperature and process variations.
5.4 Temperature/process variations

![Plot of the inductor current $I_L$ for one charging cycle with a sweep over temperature ($-40^\circ$ to $150^\circ$)](image)

Figure 5.11: Plot of the inductor current $I_L$ for one charging cycle with a sweep over temperature ($-40^\circ$ to $150^\circ$)

In Fig. 5.11 we have plotted the current through the inductor for different temperatures. We can see that the peak of the current is not changing a lot over temperature in the range from -40 to 150 degrees Celsius. This can be explained from the fact that the switches in Fig. 4.8, $S_1$ and $S_3$, used to determine $I_{Peak}$, are matched and thus their $R_{on}$ resistances are varying in the same way over temperature. Thus from this we can conclude that the peak detector works well over temperature.

The zero current detector works also well because the cycle is restarted at the moment that the current in the inductor crosses zero.

We see that the slope of the current during the discharging state is changing over temperature. This is because the fact that the forward bias voltage of the diode is changing over temperature. This influences the slope a little, because $\frac{dI}{dt} = \frac{V_s - V_{diode}}{L}$.
Figure 5.12: Plot of the inductor current $I_L$ for one charging cycle, for a sweep over process corners

In Fig. 5.12 we have plotted the current through the inductor over all process corners. We can see in this plot that the peak current is changing only slightly. Thus for different chips that we make, the peak current is the same and is not influenced much by the process parameters. The slope of the current at the discharging state is changing for the same reason as stated before for the diode and variations in $R_{ds, on}$ and $C_{par}$. 
Figure 5.13: Plot of inductor current $I_L$ for one charging cycle, for a 100 run Monte Carlo sweep without matching properties for $S1$ and $S3$.

In Fig. 5.13 we have plotted the current through the inductor following from a Monte-Carlo analysis. We see that for the whole sweep the peak current is not changing. And thus the peak current detector works also well in case of mismatch.
6 Conclusions

6.1 Conclusion

In this work we have designed an implantable and power efficient DC-DC converter, which has been designed to be implemented in the 0.35μ High Voltage I3T25 Technology of On Semiconductor. The converter needs to convert the 3.3V input voltage up to a variable output voltage with a maximum voltage of 18V. This needs to be done with a power efficiency of at least 80%. Also the converter must not be sensitive to input variations and temperature changes.

First we considered the fundamentals of a DC-DC converter. For an up-conversion of the voltage we need to store energy for a particular amount of time so that we can discharge the energy while generating a different voltage. There are two components that can store energy and these are the inductor and the capacitor. Thus we looked into the fundamental difference between storage of energy in the inductor and in the capacitor. We saw that when we charge a capacitor from zero to the supply voltage the efficiency cannot be higher than 50%. When we charge an inductor with a voltage source the initial efficiency is 100% and the longer the inductor is charging, the more the efficiency drops to zero. With a current source this is exactly the opposite.

At the end of the first chapter we look into the practical difference between a capacitor based converter and an inductor based converter. We saw that an on chip capacitor based converter is not power efficient, because it loses a lot of energy due to parasitic capacitances. By employing off-chip capacitors we don’t have this problem but when we need an 18V output voltage we need a lot of capacitors to get this high conversion factor which results in a lot of bondpads on the chip. Thus at the end of the first chapter the inductor based converter was chosen. For the up-conversion we choose to charge first an inductor with a voltage source and up-convert the voltage by discharging the inductor into a capacitor.

In the second chapter various topologies of an inductor-based converter was considered. There are three basic types of inductor based converters: the buck, the boost and the buck-boost. The boost converter is selected because we only want to convert the voltage up and because for a boost converter the input voltage source is always in series with the inductor, which results in an always higher conversion factor. Thus we achieve the best up-conversion factor with the boost converter topology.

Further, in this chapter the working principles of the boost converter are considered. There are two different types of operation: continuous current mode and discontinuous current mode. The discontinuous current mode is chosen because of the easily stability of the system, which is needed because of possible abrupt changes in the load of the converter.
Next step is to consider the design of the controller. We should assure that the system is always working in discontinuous current mode. To do this a new type of current sensing is introduced. This current sensing technique works well over a wide temperature range and over process variations. To ensure that the output voltage does not grow to a dangerous high voltage we have introduced an efficient capacitor based voltage sensing technique.

In Chapter 3 we have implemented the various system blocks at transistor level. The inductor and switches are dimensioned and the controller blocks are implemented with transistors from the I3T25 technology. Also the challenges that we get with the implementation of the system blocks are analyzed and solved in this chapter.

In the last chapter we have verified our design by means of circuit simulations and saw that the converter can up-convert the voltage to a variable output voltage, with a maximum voltage of 18V, with a power efficiency over the full range of more than the 80%. We saw also that the converter doesn’t react too much on input and output variations. Also the influence of temperature and process variations is small, enabling a robust design.

6.2 Own contribution

The following contributions are made in this thesis:

- The boost converter topology was chosen as the best topology for this DC-DC converter.

- We have designed a DC-DC converter with a variable output voltage and variable peak current up to 18V.

- We have designed a new method for current sensing in a boost converter with a low variation (0.05% by a sweep of ±100mV offset) due to of the offset cancellation circuit and well matched switches.

- We have designed a low loss voltage sensing system with capacitors, where the leakage current is considered.

- We have designed a control system for a boost converter where the converter is kept in the discontinuous current mode. The $I_{peak}$ current can be varied in the range from 20mA until 300mA and the output voltage can also varied in the range from 3.3V up to 18V.

The circuit is designed at transistor level and its correct operation verified by means of circuit simulations.
6.3 Recommendations

Recommended further work:

- design a current source circuit that is temperature independent. This current source is needed for the $I_{\text{peak}}$ reference voltage for the current sense circuit, because this is now implemented with a ideal current source with a current mirror.

- After the implementation of the current source chip layout for the whole designed circuit can be made. The parasitic capacitance needs to be taken into account for the whole circuit. Also there must take into account that there is enough ground plane around the power switch. And the switch S1 and S3 of fig. 3.15 need to be well matched for good performance of the current sense circuit. The transistors in the comparator for the $I_{\text{peak}}$ detector, zero voltage detector and the output voltage detector also need to be matched well for good performance.

- The high voltage signal lines could be inference with the controller signals, because we have a lot of pulsating currents in the high voltage signal lines. Thus the high voltage and controller signal lines need to be not too close to each other so that the high voltage signals can’t interfere the control signals.

- After the chip layout the Post layout simulations can be made to prove the circuit with the parasitic capacitance.

- After good results in the Post layout simulations the chip can be fabricate and tested to check the performance of the converter on chip.

- If the circuit is fabricated also the inductor could be optimized, because in this thesis there is looked to a good model of the inductor so that the circuit could proofed with circuit simulations and not to the best inductor.
Bibliography


