Delft University of Technology
Master’s Thesis in Computer Engineering

Wirelessly Powered Non-Volatile Memory

Stefan van Breukelen
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Master’s Thesis in Computer Engineering

Embedded Software Section
Faculty of Electrical Engineering, Mathematics and Computer Science
Delft University of Technology
Mekelweg 4, 2628 CD Delft, The Netherlands

Stefan van Breukelen
a.g.vanbreukelen@student.tudelft.nl

5th October 2014
Author
Stefan van Breukelen (a.g.vanbreukelen@student.tudelft.nl)

Title
Wirelessly Powered Non-Volatile Memory

MSc presentation
5th October 2014

Disclaimer
This MSc work has been fully performed at NXP Semiconductors in Eindhoven, The Netherlands in the period from January 2014 until August 2014 and supervised by ir. P. Niessen and ing. M.G. Verhoeven

Graduation Committee
prof. dr. K. Langendoen Delft University of Technology
dr. P. Pawelczak Delft University of Technology
dr. ir. J. Pouwelse Delft University of Technology
ir. P. Niessen NXP Semiconductors
Abstract

Content creation and content sharing have become part of our daily lives. With modern electronics, creating and sharing content has become very convenient, but this convenience has come at a price. Devices like smartphones that enable us to easily share content, are costly and complex. Devices like USB flash drives, on the other hand, are low cost and simple. However, they do lack the convenience of smartphones when it comes to sharing content.

The wireless memory presented in this thesis aims to overcome the gap between simplicity and convenience. We have designed a world-first wireless memory system composed of two components: a reader and a tag. The tag is a simple device to store user content while, the reader is able to access and manipulate the content on the tag. This thesis details the components required for designing and implementing a wireless memory. This knowledge is then used to build a proof-of-concept wireless memory. The resulting design is capable of wirelessly powering the tag and exchanging end-to-end data with a maximum speed of 31 kBps for reading and 27 kBps for writing. The peak power measured in the experiments was 2450 mW, with a system efficiency of 57%. The peak efficiency was measured at 69%. Furthermore, the tag can be positioned in various orientations with respect to the reader while maintaining normal operation.
Preface

This MSc thesis represents the work I did during my time at NXP Semiconductors in Eindhoven. However, before I got to this point I had to find a suitable group at TU Delft.

During my masters I have met numerous people that made a lasting impact on my life. These people were professors, teaching me new ways to look at things, or students that made my life easier and full of joy. During the course of this master I found myself intrigued by Embedded Systems and their influences on our daily life. After wandering around in search of a suitable group with the same interest I stumbled upon the Embedded Software group.

Although they had really interesting projects waiting for me, I was planning to search for a company where I could do my thesis. As this would prepare me for the hard life outside of the university. After several interviews I wound up at NXP Semiconductors. More precisely the Advanced Application Lab in Eindhoven, where NXP strives to develop applications to promote their semiconductors, but also to research new applications that could spark development.

During my time at NXP I met new and interesting people and gained so much knowledge on everything and on nothing. Therefore I would like to thank all the students at NXP that had to bear with me in this hardship and suffering (just kidding) and my two supervisors at NXP, Patrick Niessen and Marc Verhoeven.

I would like to thank my beloved family for putting up with me for so long and for supporting me throughout my masters. Also I cannot forget my girlfriend for all the support and love she has given me, which kept me going. I hope I made them all proud and I hope all of their (and my) worries are gone and have been replaced by new ones when I am graduated.

Last but not least I would like to thank Przemek Pawelczak, my supervisor at TU Delft, for the guidance and inspiration he has given me, so dziekuje Przemek.

Stefan van Breukelen

Delft, The Netherlands
5th October 2014
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Chapter 1

Introduction

1.1 Context

No one can deny the impact wireless communication has on the world. It has become a key, or even a necessity, in many consumer products. Our society has adapted to the usage of (wireless) communication and it has made sharing one of the corner stones. Sharing, particularly sharing content, has been made easy by modern technology. People can produce all sorts of content, like videos and photos, with their smartphone and share it with the world.

However, the ease of sharing content does come at a price. Smartphones that enable easy content sharing are fairly expensive. Furthermore, smartphones need to be recharged frequently. USB flash drives on the other hand are low in cost, simple and do not require recharging. However, they lack the convenience provided by the wireless communication capability of the smartphone. It would be much more convenient if we were able to share content wirelessly without the need to recharge anything, without the need to find an empty port and without the need to think about device orientation and of all that at the cost and with the simplicity of a common flash drive.

1.2 The Wireless Memory Concept

There is a gap between content sharing devices such as the smartphone and the common flash drive. This gap is caused by the high cost and complexity of the smartphone and the inconvenience of the flash drive. Currently effort is being made to overcome this gap and launch a new type of memory. This memory will allow for easy content sharing at the low cost of a flash drive, but with the convenience of a smartphone. This type of memory will be henceforth referred to as wireless memory. This section provides background information about the wireless memory concept, in order to have a better understanding of the meaning and the purpose of a wireless memory.

1.2.1 Concept

The wireless memory as defined in this thesis describes a non-volatile memory that is wirelessly powered and can be accessed wirelessly. This wireless memory
can be as small as a micro SD card and can have the same capacity as current micro SD cards. The difference between an SD card and a wireless memory lies in the easy accessibility of the wireless memory.

The basic components of the Wireless Memory System (WMS) are a Wireless Memory Reader (WMR) and a Wireless Memory Tag (WMT), where the WMT contains the non-volatile memory used for storing content and the WMR is able to access and manipulate this content. The WMR can be anything ranging from a smartphone to a stand alone device (various use cases are presented in Section 1.2.2). Also the WMT can come in various forms such as a card, a bracelet, a micro SD card, depending on the application. Figure 1.1 illustrates the basic components of the WMS according to this concept. The two key features of this system are the wireless power transfer and the high-speed data transfer. The combination of these two features makes this system unique.

1.2.2 Use Cases

Several use cases are presented here to give a better understanding of the possibilities of a wireless memory.

Device Storage Extension

Nowadays micro SD cards are often used to extend the memory capacity of a mobile devices such as smartphones. A wireless memory can be used in a similar fashion but would not require a physical connector. The connector-less design of this system can reduce the design complexity, increase the lifetime and decrease the cost of the device. Furthermore, a wireless memory can increase the ease in which people can share content when compared to memories that require physical contact. Wireless memories can easily be integrated in sleeves for mobile phones without any physical contact.

Multimedia Carrier

A (read-only) wireless memory can be used to store multimedia content and in essence replace the multimedia discs (i.e. DVD, Bluray). Integrating various multimedia codecs in the WMR creates a multimedia player, which can read multiple multimedia carriers simultaneously. People can easily view, share and add multimedia content just by placing the multimedia carrier near to the WMR. A wireless memory multimedia player can increase longevity, safety and
decrease cost because it does not require any moving parts or a laser like a DVD player.

**Personal Data**

Current technologies like RFID and NFC have a limited memory capacity. This limited memory capacity also limits the applications of these technologies. With the memory size limitation removed, all sorts of personal data can be gathered and stored on a single device. Personal data like medical records, passport information, driver license, etc. can all be accessed from this device. Children and elderly could wear such a device and in case of emergency it could be read to obtain medical information, a home address and a phone number. It can also allow people to travel, pay or gain access to services or buildings. This device could be anything from a credit card to a bracelet. In Figure 1.2 a wireless memory is built into a smartwatch. People would only have to carry this device with them at all time.

![Figure 1.2: Smartwatch with personal data for contactless payment, identification and other personal information (figure courtesy of J. Jim).](image-url)
Advertisement

Very low cost wireless (read-only) memories can be used for advertisement purposes. These memories can be added to newspapers, posters and catalogs containing promotional material, coupons and other advertisement material. For instance a movie production company can add a wireless memory to their posters that contain a trailer promoting their new movie. Business cards could contain an entire resume and more. Figure 1.3 illustrates the advertisement concept for a newspaper.

Figure 1.3: Advertisement concept for newspapers. To download the newspaper a user would have to come close enough to start the data transfer (figure courtesy of J. Jim).

PC Reader Pad

Another concept is the PC WMR pad. The PC WMR pad can easily be connected to a PC and used for reading and writing content to the wireless memory. The PC WMR pad can be compared with a reader for SD cards but users can
easily place the wireless memories on top of the pad. This concept should be a stepping stone for people to purchase wireless memories. Further development of the WMR can lead to the integration in a laptop as illustrated in Figure 1.4.

Figure 1.4: Concept for a WMR integrated in a laptop. Comparable to a USB port but more convenient (figure courtesy of J. Jim).

1.3 The Wireless Memory Market

The WMS discussed in Section 1.2.1 could bring forth a whole new niche in the memory market. The wireless memory would be competing with USB flash drives, SD cards, Bluray discs and other technologies primarily focused on consumers.

1.3.1 Competing Technologies

USB Flash Drives

USB flash drives are flash memories with an integrated USB interface as a means of accessing the content. They are often used because of their high capacity (>GBs), portability and low cost. USB flash drives utilize the Mass Storage Class (MSC) standard, which is supported by modern operating systems, as well as many BIOS boot ROMs. The USB flash drives market has been forecast to reach volume sales of 561 million units by 2018 worth billions of dollars[8].

Secure Digital Memory

The Secure Digital or SD standard was introduced in 1999 as an improvement on Multi Media Cards (MMC). SD memory cards can be found in many portable
devices as a means to safely store content and increase capacity. They are similar to USB flash drives as they also use flash memories. However, the interface is different and SD cards are typically smaller. The global market for SD memory cards is forecast to reach $21.3 billion by 2018.

Eye-Fi

Eye-Fi is a company based in California, which produce SD cards with Wi-Fi capabilities. Inserting an Eye-Fi card in a digital camera allows for uploading photos and videos to a device in the network automatically. Although this memory could be classified as a wireless memory it still has the inconvenience of manually connecting it to a network. Furthermore, it requires to be physically inserted in a device to power it.

1.3.2 Goals

As the market for memories is forecast to be worth billions of dollars, stepping into this market could prove to be very profitable. When wireless memories will be introduced it is likely that this will be a niche market with new opportunities. The first goal is to develop a working demo. Next, the wireless memory standard should be finished and a prototype should be ready for consumer testing. The final step is to develop a fully functional product for consumers, potentially for one of the use cases presented in Section 1.2.2. Intermediate steps and goals are not taken into consideration as this thesis does not present a thorough market research.

1.4 Problem Statement

Currently, wireless memory is being standardized in the TG649.1 standard by the Jedec standardization body. Members of the committee dealing with the wireless memory standard include Nokia, Samsung Semiconductor, Micron and NXP. The interest of NXP to participate in the standardization of wireless memory comes forth from the potential circuits, drivers and chips that could be a part of the wireless memory. These include power circuitry, memory controllers, NFC readers/tags, security systems and antenna circuitry. However, before a truly wireless memory can be realized, many steps have to be taken.

In this thesis we answer the question: how to build a wireless memory and implement an operational proof-of-concept system?

1.5 Thesis Organization

This thesis is organized as follows. Chapter 2 presents an overview of the components required for a WMS. In this chapter the theory behind wireless power transfer will be presented and various characteristics of a wireless power transfer system will be discussed in detail. The last section of this chapter presents a discussion about potential wireless and memory technologies for integration in a wireless memory.
In Chapter 3, all the components forming a proof-of-concept WMS are presented. This chapter will elaborate on the hardware and software design of the WMR and WMT. Furthermore, the setup of the proof-of-concept WMS and the experimental results are presented.

Finally, the conclusions of this thesis and possible future work are presented in Chapter 5.
Chapter 2

Wireless Memory Components

This chapter presents the various components required for implementing a WMS. It includes aspects from wireless power transfer as well as memory and wireless technologies. In Section 2.1 the wireless power transfer systems are classified. Sections 2.2 and 2.3 present the theory of wireless power transfer. Finally Section 2.4 discusses possible memory and wireless technologies for integration in a WMS.

2.1 Wireless Power Transfer Systems

Wireless power transfer systems can be classified, based on the distance from the power source, in near-field and far-field systems.

2.1.1 Near-Field and Far-Field

Electromagnetic fields or EM fields are produced by electrically charged objects and extends indefinitely throughout space. The EM field describes the electromagnetic interaction that the electrically charged object has on other objects. It is one of the four fundamental forces of nature.

For objects producing an EM field, the space surrounding the object can be divided into regions. For an electrically small antenna\(^1\) there are two distinct regions: the (reactive) near-field and the (radiating) far-field. Typically, the boundary between these two regions is assumed to be a distance \(r\) from the antenna, defined as \[ r = \frac{\lambda}{2\pi}. \] (2.1)

In the case of an electrically large antenna, the radiating field is split into a radiating near-field and a radiating far-field. Therefore the space surrounding the antenna is divided into three regions: the near-field region, the far-field

\(^1\)An antenna is considered electrically small if the total conductor length is less than a tenth of the wavelength [26].
region and the transition zone that separates the near-field and far-field regions. In the transition zone both near-field and far-field effects are important. In Figure 2.1 the different regions are presented as a function of the wavelength $\lambda$.

![Figure 2.1: Definition of the regions surrounding an electromagnetic source in terms of wavelengths [20, p.20].](image)

### 2.1.2 Near-Field Systems

This section presents several wireless power transfer systems that operate in the near-field.

**Electrostatic Induction**

Electrostatic induction or capacitive coupling is a technique where energy is transferred by means of the capacitance between electrodes. An electric field is created by charging the electrodes with a high potential, high frequency AC power supply.

When the charged object comes near an uncharged (electrically conducting) object, the force of the nearby charge will attract the electrons in the object. This results in a positive and a negative charge in the previously uncharged object, thus transferring energy from one object to the other.

Electrostatic induction systems benefit from the simplicity and low cost of their designs, making them attractive for wireless charging stations. The system reported in [31] is able to transfer up to 3.7 W with more than 80% efficiency. The electrostatic induction system also confines the electromagnetic fields between the electrodes, removing the need for magnetic flux guiding and shielding components. However, the amount of coupling capacitance is limited by the area of the receiver and the distance between the transmitter and receiver. A large area and a small distance is required to enable efficient power transfer, thus imposing a serious design constraint on the system.

**Electromagnetic Induction**

Electromagnetic induction or inductive coupling is a technique where energy is transferred wirelessly by means of magnetic fields. The magnetic field is generated by applying an AC current to a (primary) conductor. When a secondary conductor enters the magnetic field of the primary conductor a force is applied
to the free electrons in the secondary conductor. This will cause the electrons to move and induce a current thereby transferring energy from one conductor to the other.

Inductive coupling is used by numerous systems as a means to transfer power \[60, 24, 23\]. In \[29\] a system is reported that is able to transfer 69 W with a system efficiency of 69 %.

Beside the academic research, inductive coupling is implemented in various products and standards. The Wireless Power Consortium or WPC was one of the first to standardize wireless power transfer for mobile devices in their Qi standard \[59\]. This standard utilizes inductive coupling to charge mobile devices such as smartphones. Members of the WPC include NXP, Philips, Nokia, Asus, HTC, Huawei, LG Electronics, Nokia and many more. The current version of the Qi standard aims to deliver a maximum of 5 W over a distance of 4 cm. Newer versions aim for higher power levels and larger distances.

2.1.3 Far-Field Systems

This section presents several wireless power transfer systems that operate in the far-field.

RF Power

In RF power transmissions two systems can be classified, passive and active RF power systems. Passive systems only harvests ambient RF energy and active systems have an active transmitter as part of the system. In \[47\] a passive RF power system is presented. This system is reported to harvest 60 \(\mu\)W from a distance of approximately 4 km. Although this ambient energy is 'free', the power densities in these systems are typically very low.

Using an active system could increase the power transfer as ‘more’ power is available for the receiver. In \[45\] an active system is presented that is able to transfer 2.8 mW. Although this is a considerable increase when compared to \[47\], the power density is still low. These systems typically have a large operating range, but a low efficiency and low power densities.

Solar Power

Solar power is the ultimate form of green energy when harvested from natural sunlight. It can be harvested directly from sunlight, using photovoltaics or indirectly, using Concentrated Solar Power (CSP). CSP systems use lenses or mirrors to focus sunlight into a small beam that is used as a heat source for a conventional power plant. CSP systems are used for large-scale solar-power plants and are not suited for small-scale integration.

A photovoltaic cell or solar cell, directly converts light into electricity using the photovoltaic effect and can be integrated in small scale devices. Recently the Fraunhofer Institute for Solar Energy Systems achieved a solar cell efficiency of 44.7 % \[58\], setting the record for highest efficiency. The disadvantage of this system is the rapid decrease in power when the light source is blocked. Encasing the solar cell would render it useless.
Laser Power

The laser is another form of electromagnetic radiation, which is closer to the visible region of the spectrum than the previously discussed RF power. The power transmitted from a laser can be converted back into electricity by aiming it at a solar cell. However, the laser should be aimed precisely at the solar cell and a clear line-of-sight is required. This system can actively power a receiver at higher efficiencies when compared to receiving ambient light. Laser systems are primarily used in military weaponry and aerospace applications. In an experiment performed by the US Jet Propulsion Laboratory in 1975 30 kW was transmitted over a distance of 1.54 km with an efficiency of 85% [51]. However, these laser systems require precise guidance and a line-of-sight to ensure that energy is transferred.

Ultrasound

Ultrasound power transfer systems are able to harvest energy from acoustic waves. This system utilizes ultrasonic acoustic transducers, which are able to convert the pressure of an acoustic wave into electricity and vice versa. In [34], a system is presented that can transfer only 37 µW at an efficiency of 16%. The advantage of this system is the freedom of movement and the reasonable efficiency, but the power density of this system is typically very low.

2.1.4 System Conclusion

The choice of the power transfer technology mainly depends on the application. Reviewing the use cases presented in Section 1.2.2 it can be concluded that the requirements of a wireless power transfer system, with the intended use in a wireless memory, are as follows:

- Low power transfer is required, as the power consumption of the WMT should be minimal (in the order of milliwatts);
- A short range of 30 mm, according to the current version of the TG649.1 standard [7];
- High power transfer efficiency of at least 50% is preferred to keep the transmission power and the losses to a minimum;
- Small footprint, especially on the WMT side where strict size constraints can be implemented. For instance the integration of a wireless memory in ID-1 cards.\(^2\)

Due to these requirements, near-field systems, like the capacitively coupled and inductively coupled system, are preferred. However, the size constraints imposed by the capacitively coupled system is a serious risk to the future success of the WMS. Therefore the capacitively coupled system can be excluded leaving only the inductively coupled system, which has been implemented on numerous occasions \(^{23}\), \(^{14}\), \(^{25}\) and is utilized in the Qi standard [59].

\(^2\)ID-1 is a standard card size of 85.60 x 53.98 mm, defined in the ISO/IEC 7810 standard [2].
2.2 Inductively Coupled System

Two configurations are possible in a wireless power transfer system utilizing inductive coupling: an inductively coupled system and a resonant inductively coupled system.

2.2.1 Inductive Coupling

The inductively coupled system utilizes a magnetic field to wirelessly transfer power. The magnetic field is generated by a transmitter and is picked up by a receiver. In Figure 2.2 the model of an inductively coupled system can be found.

![Figure 2.2: Model of an inductively coupled system](image)

In this figure the left circuit represents the transmitter. In the transmitter an AC power supply provides an alternating current to the conductor (or coil) \( L_1 \), which generates a magnetic field around the conductor. When the receiver, represented by the right circuit, is placed in the magnetic field, a current will be induced in coil \( L_2 \). This current will flow through the load represented by the resistor \( R_L \). Resistors \( R_1 \) and \( R_2 \) represent the resistance of coil \( L_1 \) and \( L_2 \) respectively.

In inductively coupled systems characteristics such as efficiency and power transfer are determined by the degree of coupling between the transmitter and the receiver. The degree of coupling depends on the quantity of the magnetic field that penetrates the receiver coil. This quantity is also referred to as, magnetic flux. Higher coupling contributes to higher efficiencies and power transfer (see Figure 2.4). The degree of coupling highly depends on the orientation of the receiver coil with respect to the transmitter coil. Misalignment between the receiver and transmitter coils reduces the amount of magnetic flux that penetrates the receiver coil thereby decreasing power transfer and efficiency [20].

2.2.2 Resonant Inductive Coupling

In order to improve the power transfer and the efficiency, resonant inductive coupling is introduced. In physics, resonance is the tendency of a system to oscillate with greater amplitude at a certain frequency, called the resonant frequency. Resonance is a well-known phenomenon in mechanics but resonance occurs with all types of vibrations and waves. In resonant coupled systems, each coil is capacitively loaded to form a tuned LC circuit. If both coils are tuned to the same resonant frequency, significant power can be transferred. Figure 2.3 illustrates the model of an resonant inductively coupled system.

In the transmitter and receiver a compensation (or tuning) capacitor is added to tune both the transmitter and receiver to the same resonant frequency. In
the transmitter \( C_1 \) and \( L_1 \) form a series LC circuit. In the receiver \( C_2 \) and \( L_2 \) form a parallel LC circuit. Depending on the chosen compensation topology, the characteristics of the resonant coupled system may vary. The possible topologies are [46, chp.2]

- Primary series - Secondary series (PSSS);
- Primary series - Secondary parallel (PSSP);
- Primary parallel - Secondary series (PPSS);
- Primary parallel - Secondary parallel (PPSP).

According to [22], the secondary parallel compensation reduces the active power loss while the series compensation has no effect on the power loss. Furthermore, the parallel compensation improves the system power factor significantly when compared to the series compensation. A secondary series compensation, however, reduces the total reactive power loss significantly when compared to a parallel compensation. In this thesis the PSSP topology is implemented, but the compensation topology can be altered depending on the requirements of the application.

2.3 Resonant Coupled System Characteristics

In this section various key characteristics, with respect to resonant coupled systems, are identified and presented.

2.3.1 Link Efficiency

The link efficiency is a key characteristic as it indicates the quality of power transfer over the air without including the losses that occur in the rest of the system. Link efficiency is often used to compare wireless power transfer techniques without a degradation in the efficiency due to lower quality components or varying setups. To obtain the maximum link efficiency, the following equation is given [14]

\[
\eta_{\text{link}} = \frac{k^2 Q_1 Q_2}{\left(1 + \sqrt{1 + k^2 Q_1 Q_2}\right)^2},
\]

where \( k \) is the coupling factor, \( Q_1 \) the quality factor of the transmitter and \( Q_2 \) the quality factor of the receiver. This equation provides us with a theoretical
limit of the power transfer efficiency between the two coils. Figure 2.4 illustrates
the link efficiency for various quality factors.

![Figure 2.4: Link efficiency as a function of the coupling factor for various quality factors (2.2). The quality factors of the transmitter and receiver are considered to be equal.](image)

This figure shows the relationship between the coupling factor, quality factor and the efficiency in a wireless power transfer system. The quality factors 10, 100 and 1000 represent a low, average and high quality factor for a wireless power transfer system, respectively. The quality factor for a typical NFC enabled system is 35 [18].

**Coupling Factor**

The coupling factor or coupling coefficient is a quantitative representation of the degree of coupling between a primary and secondary coil. The quantity of flux that penetrates the secondary coil determines the degree of coupling. Higher quantities of flux result in better coupling and therefore a higher coupling factor. The coupling factor can range from 0 to 1, where 1 is perfect coupling and 0 is no coupling. In the case of perfect coupling all the flux penetrates the secondary coil. In the case of no coupling, none of the flux penetrates the secondary coil, meaning that the secondary coil is completely removed from the magnetic field. The coupling factor is expressed as [19, p.70]

\[ k = \frac{M}{\sqrt{L_1 L_2}}, \] (2.3)

where \( M \) is the mutual inductance, \( L_1 \) is the inductance of the primary coil and \( L_2 \) is the inductance of the secondary coil.

Mutual inductance is introduced when the secondary coil is placed within the magnetic field of the primary coil and the two coils are connected together by the magnetic flux. Figure 2.5a illustrates the concept of mutual inductance and Figure 2.5b illustrates the model equivalent.
Mutual inductance is always present between two electric circuits. The mutual inductance has the same dimension and unit as the inductance and can be determined by

\[ M = \frac{|L_{\text{ser}} - L_{\text{par}}|}{4} \]  

where \( L_{\text{ser}} \) is the series inductance and \( L_{\text{par}} \) is the parallel inductance of the transmitter and receiver coil. The mutual inductance two coils depends on the inductance of coils and the misalignment between the coils. Separating the coils will result in a lower mutual inductance and therefore a lower coupling factor and a lower link efficiency (see Figure 2.4).

**Quality Factor**

In physics and engineering the quality factor or Q factor is a dimensionless parameter that indicates the energy losses within a resonant element. High Q factors indicate a lower rate of energy loss relative to the stored energy in the resonator. The resonating element in a wireless power transfer system is the LC circuit, formed by the coil and the capacitive compensation in both the transmitter and receiver. The Q factor is expressed as the ratio of the inductive reactance to the resistance

\[ Q = \frac{\omega L}{R}, \]  

where \( \omega \) is the angular frequency, \( L \) is the inductance of the coil and \( R \) is the resistance of the coil.

Resonators with a high Q factor have a low damping that allow the oscillation to be sustained for a longer period and with greater amplitudes. This tells us
that higher Q factors can lead to better performance in wireless power transfer systems by reducing the losses. However, when the Q factor increases the bandwidth decreases, as can be seen in Figure 2.6.

![Figure 2.6: Effect of the Q factor on the gain][3]

A small bandwidth leads to very sharp peaks where a small deviation from the resonant frequency can result in a significant decrease in power transfer. Therefore systems with very high Q factors require precise tuning making it more difficult to mass produce. So the designer has the outweigh the increased performance against the tuning precision.

Furthermore, systems that require power transfer and data transfer over the same link (i.e. NFC) prefer a higher bandwidth. In these systems the Q factors are typically low [18] (i.e. 35) and therefore the link efficiency is typically low (see Figure 2.4).

### 2.3.2 System Efficiency

System efficiency is a more realistic method of indicating the efficiency than the previously discussed link efficiency. This is because the system efficiency takes the entire end-to-end system into account allowing for a fair comparison between complete systems in stead of system components. The system efficiency can be expressed as

\[
\eta_{sys} = \eta_{link}\eta_{tx}\eta_{rx} = \frac{P_{load}}{P_{input}}, \tag{2.6}
\]

where \(\eta_{link}\) is the link efficiency, \(\eta_{tx}\) the transmitter efficiency, \(\eta_{rx}\) the receiver efficiency, \(P_{load}\) is the power measured at the receiver load and \(P_{input}\) is the power measured at the transmitter input.

This equation includes all the losses that occur in the system. The link efficiency includes losses caused by misalignment and environmental influences. The transmitter and receiver efficiency includes losses caused by circuit components, such as the DC-AC converter, power amplifier, DC-AC converter, power regulator, etc.

Now consider a system where the transmitter and receiver have a high efficiency of 90%. The resulting system efficiency will be about 20% lower when compared to the link efficiency, as can be observed in Figure 2.7.
The simplest method for accurately determining the system efficiency is to calculate the ratio between the power dissipated at the load on the receiver side and the input power at the transmitter side, as done in (2.6). In this thesis the system efficiency will be used to define the efficiency of the proof-of-concept WMS. The results of the system efficiency measurement are presented in Section 4.1.2.

### 2.3.3 Power Transfer

In (2.6) the load power $P_{load}$ is used to calculate the system efficiency. However, the load power is also a key characteristic of the system because it indicates the quantity of power available for an application. This power co-determines the capabilities of a system. In the case of a WMS, the power transfer determines the types of WMTs that can be used in the WMS. Certain WMT types can require more power than other types, depending on the application. Also increasing the power transfer can lead to an increase in the amount of WMTs that can be used simultaneously. On the other hand decreasing the power can lead to integration of the WMR in battery powered devices where power should be conserved.

![Model of a resonant inductively coupled receiver](image)

To determine the maximum power that can be transferred, consider a system with the receiver illustrated in Figure 2.8. If the receiver is tuned to the correct resonant frequency and the load $R_l$ is properly matched, the maximum power that can be transferred is...
where $Q$ is the quality factor of the receiver, $U_{\text{ind}}$ is the induced voltage in the coil, $\omega$ is the angular frequency and $L_1$ is the coil inductance. In Figure 2.9 the maximum power is illustrated in terms of the induced voltage in the receiver coil.

**Figure 2.9:** Maximum power in terms of induced voltage at the receiver (2.7). The receiver operates on 13.56 MHz, the coil inductance is $1 \, \mu\text{H}$ and the Q factor is 100.

### 2.3.4 Spatial Freedom

The spatial freedom indicates the freedom of movement a user has in a particular system. Therefore the spatial freedom can also be a measure for the degree of user comfort. In the WMS, the spatial freedom reflects the positioning freedom of the WMTs with respect to the WMR without rendering them inoperational. A high spatial freedom allows a user to use the WMT without carefully positioning it on the WMR. The spatial freedom depends on the longitudinal, lateral, angular misalignment and the size of the coils due to the direct influence of these parameters on the efficiency and power transfer. With the help of the coupling factor approximation given by [20], the effects of misalignment can be illustrated. The coupling factor is expressed as

\[
k \approx \frac{a^2b^2}{\sqrt{ab(\sqrt{x^2 + a^2})^3}}, \tag{2.8}
\]

where $a$ is the transmitter coil radius, $b$ is the receiver coil radius and $x$ is the distance or longitudinal misalignment between the coils. Integrating equation (2.8) in (2.2) the link efficiency can be plotted as in Figure 2.10. A larger separation of the coils will result in a reduced efficiency because the coupling between the coils decreases. Using higher Q factors reduces the impact of the coil separation on the efficiency.
Figure 2.10: Maximum link efficiency in terms of the relative distance between the transmitter and receiver for various Q factors (2.2), (2.8). The relative distance is the distance between the transmitter and receiver (x) and the coil diameter (d=a=b). The diameter for the transmitter and receiver coil is 5 cm.

2.3.5 Integration in Wireless Memories

The requirements for a wireless power transfer in a typical WMS presented in Section 2.1.4 are: low power, short range, high power-transfer efficiency and small footprint. The small footprint is especially important at the receiver or WMT side where the size constraint is greatest.

To achieve a high efficiency and a small footprint two characteristics are of great importance. First using a resonant system, as discussed in Section 2.2.2, will increase the efficiency when compared to a non-resonant system. Secondly, using a higher frequency allows for smaller components, making it easier to comply with the size constraints of the system.

Effects of Resonance

Systems using resonant coupling have been proven to be more efficient than plain inductively coupled systems [57]. To investigate the reason behind this, consider the system illustrated in Figure 2.5b. In case of resonance the reactances of the capacitor and the coil cancel each other out, leaving only the real impedance. The impedance calculation for an PSSP topology, used in the WMS, is expressed as [46, p.27]

\[
Z = \frac{M^2 \omega^2}{j\omega(L_2 + M) + R_2 + \frac{R_1}{1 + jR_1C_2\omega}} + j\omega(\frac{L_1 + M}{\omega C_1} + R_1), \quad (2.9)
\]

where \(M\) is the mutual inductance, \(\omega\) is the angular frequency, \(L_1\) and \(L_2\) are the inductances of the transmitter and receiver coil respectively, \(R_1\) and \(R_2\) represent the resistance of the transmitter and receiver coil and \(C_1\) and \(C_2\) are the tuning capacitors of the transmitter and receiver circuits respectively.
Inserting the component values for a system with a resonance frequency on 13.56 MHz leads to Figure 2.11. This figure shows a significant drop of the impedance at 13.56 MHz. At this frequency only the real part of the impedance remains and is dissipating power. In a non-resonant system the distinction can be made between real power and reactive power. The reactive power is unwanted because it cannot be consumed by the load but it does heat up the reactive components thereby wasting energy. So deviating from the resonant frequency results in a degradation in efficiency.

![Impedance graph](image)

Figure 2.11: Impedance for an PSSP topology with the resonance frequency on 13.56 MHz [2.9].

The downside of operating at the resonant frequency is the need for tuning both the transmitter and receive to the same frequency. For mass produced and low cost devices, this tuning can be very difficult as mass production and lower quality components can lead to variations between the devices. Furthermore, the precision of the tuning is linked to the Q factor of the system. As high Q factors increase both the slope and the gain of the power transfer (see Figure 2.6), higher precision tuning is required. Lowering the Q factor would decrease the slope and thereby increase the bandwidth. A larger bandwidth results in a larger tuning range, therefore decreasing the need for precise tuning.

The link between the Q factor \( Q \) and the bandwidth \( BW \) can be expressed as \[ Q = \frac{f_c}{f_c - 3\text{dB}\text{high} - f_c - 3\text{dB}\text{low}} = \frac{2\pi f_c L}{R} \] (2.10),

where \( f_c \) is the center frequency, \( f_c - 3\text{dB}\text{high} \) and \( f_c - 3\text{dB}\text{low} \) are the \(-3\text{dB}\) points of the upper and lower slope. The difference between them is known as the
bandwidth ($BW$). The center frequency and the bandwidth are expressed as

$$f_c = \frac{1}{2\pi \sqrt{LC}}, \quad (2.11a)$$

$$BW = f_{c-3dB_{high}} - f_{c-3dB_{low}} = \frac{f_c}{Q}, \quad (2.11b)$$

Consider two systems with identical center frequencies and inductances but varying Q factors. One system has a low Q factor of 10 and the other system has a high Q factor of 1000. The high Q factor system will require more precise tuning to remain within the −3 dB range. To be more precise the tuning range has decreased by a factor 100 when compared to the low Q factor system. The trade-off between complexity and performance has to be made by the system designer. In this thesis performance is more important to reach the goals, set in Section 2.1.4.

**Effects of Frequency**

Systems based on the Qi standard operate in the low frequency (LF) band, around 110 kHz [56]. Using higher frequencies has two advantages. First, the system components can be smaller and second, the efficiency is increased. The wireless power transfer system proposed for the wireless memory operates in the high frequency (HF) band on 13.56 MHz. To explain the effects of frequency on the component size and efficiency consider a system with an operating frequency of 110 kHz and a system with an operating frequency of 13.56 MHz. Both systems use identical coils with an inductance of 1 $\mu$H. To calculate the value of the tuning capacitor, the following equation can be deduced from (2.11a)

$$C = \frac{1}{(2\pi f_c)^2 L}. \quad (2.12)$$

The tuning capacitor of the LF system would have a value of 2 $\mu$F and the tuning capacitor of the HF system would have a value of 138 nF. The tuning capacitor of the high frequency system is considerably smaller, which allows us to use smaller packages.

Calculating the link efficiency with (2.2) for the two systems results in Figure 2.12. Clearly the HF system has a higher link efficiency for the full coupling range.

Although higher frequencies can reduce the component size and improve efficiency it also increase losses in the power transfer circuit. The two major losses caused by frequencies are: conduction losses and switching losses. Conduction losses occur due to the skin effect, which is the tendency of an alternating current to be most dense near the surface of a conductor. The current flows mainly at the ‘skin’ of the conductor, between the outer surface and the skin depth. The skin effect causes the effective resistance of the conductor to increase at higher frequencies. This is due to the decreased skin depth, which reduces the effective cross-section of the conductor. The skin depth is expressed as [55]

$$\delta = \sqrt{\frac{\rho_c}{\pi \mu_f}}, \quad (2.13)$$
Figure 2.12: Link efficiency for a LF system (110 kHz) and a HF system (13.56 MHz)

where \( \rho_c \) is the resistivity of the conductor, \( f \) is the frequency and \( \mu \) is the combination of the permeability of space and the relative permeability of the conductor.

Switching losses occur when semiconductors such as MOSFETs are switching from a conducting to a non-conducting state and vice versa. During the transition to the conducting state the current rises and the voltage drops simultaneously. In the transition from the conducting state to the non-conducting state, the voltage rises and the current decreases. During these two transitions power is lost due to the overlap in switching current and voltage. The power loss increases as the frequency of the switching increases.

### 2.4 Memory and High Speed Data Channel

This section presents a discussion about suitable memory technologies for the WMT memory and suitable technologies for transferring data between the WMR and WMT.

#### 2.4.1 Non-Volatile Memory

A key component in the WMS is of course the memory. Current RFID/NFC systems have a limited memory capacity making them unsuitable for multimedia applications or even sharing content. The WMS promises memory capacities in the order of gigabytes, comparable to current flash drives. To make the wireless memory more competitive with flash drives or SD cards one can also look at other memory technologies, which could decrease cost, increase transfer speeds or increase capacity. Selecting the appropriate memory technology highly depends on the use case even within a wireless memory. Perhaps mul-
Table 2.1: Comparison of various memory technologies for integration in a WMS [44].

<table>
<thead>
<tr>
<th>Cell Size [a]</th>
<th>Read Latency</th>
<th>Write Latency</th>
<th>Energy per bit access</th>
<th>Static Power</th>
<th>Endurance [b]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Disk</td>
<td>NAND Flash</td>
<td>PCRAM</td>
<td>RRAM</td>
<td>MRAM</td>
<td></td>
</tr>
<tr>
<td>Maturity</td>
<td>Product</td>
<td>Advanced development</td>
<td>Early development</td>
<td>Advanced development</td>
<td></td>
</tr>
<tr>
<td>2/3 F²</td>
<td>8.5 ms</td>
<td>25 μs</td>
<td>48 ns</td>
<td>&lt;10 ns</td>
<td>&lt;10 ns</td>
</tr>
<tr>
<td>4-5 F²</td>
<td>200 μs</td>
<td>40-150 ns</td>
<td>10 ns</td>
<td>12.5 ns</td>
<td></td>
</tr>
<tr>
<td>8-16 F²</td>
<td>48 ns</td>
<td>&lt;10 ns</td>
<td>10 ns</td>
<td>10 ns</td>
<td>&gt;10¹⁰</td>
</tr>
<tr>
<td>&gt;5 F²</td>
<td>&lt;10 ns</td>
<td>&lt;10 ns</td>
<td>2 pJ</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>&gt;37 F²</td>
<td>10 ns</td>
<td>0.02 pJ</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
</tbody>
</table>

*a* Cell size is expressed as the feature size, which is the size of the smallest feature on an IC, usually the length of the transistor channel [4].

*b* Number of write cycles that a memory cell endures before eventually wearing out.

Multiple memory technologies should be used in order to provide the best fit for the application. However, all use cases presented in Section 1.2.1 have a common requirement, the memory technology should be non-volatile. Meaning that the memory should retain the content without the need for a continuous power source.

Other considerations that have to be made in selecting an appropriate memory technology are: the maturity of the technology, power consumption, memory density, data retention, reliability, endurance, cost and transfer speeds.

Various memory technologies and their characteristics are discussed in [44]. Table 2.1 presents a comparison between the non-volatile memories (NVMs) discussed in [44]. In this table current NVM technologies are compared against emerging NVM technologies.

PCRAM, RRAM and MRAM are the three most promising memory technologies under development at this moment. The ideal future memory technology should be non-volatile, low cost, high in density, energy efficient and should have a high endurance. Unfortunately none of the presented technologies possess all of the aforementioned characteristics. However, all three can potentially be used as main memory if the cost per bit of each is low enough to be competitive with NAND flash and disk memories. At this moment in time however, the NAND flash and disk memories remain the best choice for storing content. Although disk memories provide higher densities they lack in transfer speed and consume the most energy per bit. Therefore the most practical memory technology for a wireless memory is NAND flash.
2.4.2 High Speed Data Channel

One of the major differences between the WMS and a typical RFID system (i.e. NFC), is the need for high data rates. Typical NFC readers have a bit rate of 424 kbps (see Table 3.2), which is far too low for multimedia applications and sharing large files.

Another technology has to be found to provide a high-speed data channel to exchange data between the WMR and the WMT. Fortunately multiple technologies are available that provide a high data rate. However, power consumption, interference, reliability and cost also have to be taken into account. In this section several wireless technologies are discussed and compared in order to find a suitable technology for the WMS.

Ultra-wideband

Ultra-wideband or UWB, is a wireless technology for short range and high data rate communication. UWB transmits energy at specific time intervals and thereby occupies a large amount of bandwidth that is used to achieve high data rates. To keep the interference in the occupied band to a sustainable level, the transmission energy has to be kept low, which results in a short range. In [32] a system is presented that is able to transmit data at a rate of 112.5 Mbps with a power consumption of only 58 pJ per bit and 48 pJ per bit for transmitting and receiving respectively. The UWB transceiver in [50] was able to achieve a maximum data rate of 4 Gbps with an overall power consumption of 61 mW for transmission. UWB systems are very diverse and have sparked the interest of many researchers. However, UWB technologies have not been very successful in consumer products and this shows in the limited number of companies bringing UWB technologies to the market.

TransferJet

TransferJet is a close range wireless technology developed by Sony and promoted by the TransferJet consortium. It operates in a similar fashion as NFC does, only on much higher data rates. The concept of TransferJet is based on the "touch" model where a user (almost) touches another TransferJet device to start sharing data.

TransferJet has a peak data rate of 560 Mbps [16], it has a maximum operating range of a few centimeters. TransferJet uses a point-to-point topology that allows for a short connection setup time. The spectrum is centered at 4.48 GHz and occupies a bandwidth of 560 MHz. Similar to UWB, TransferJet uses the 'high' bandwidth to achieve high data rates. Furthermore, the transmission energy has to be kept low to minimize interference, resulting in a short operating range. Although TransferJet is gaining momentum, the popularity of the technology still remains low.
Wi-Fi

Wi-Fi is one of the most common wireless technologies nowadays. It can be found in millions of devices worldwide as a means of connecting these devices to wireless networks. Wi-Fi is based on the IEEE 802.11 standards and the trademark is owned by the Wi-Fi Alliance.

The two basic components in a Wi-Fi network are the Access Point (AP) and the clients that connect to the AP. This setup is prone for interferences because multiple clients could be connected to a single AP, congesting the network. Furthermore, Wi-Fi devices have a typical range of tens of meters making them more susceptible for eavesdropping and man-in-the-middle attacks (see Section 5.2.3). Therefore, Wi-Fi supports a fairly high security to setup a secure link between a client and an AP. Wi-Fi technology supports high data rates, is very versatile and is used worldwide.

The latest standard in the Wi-Fi range, is the 802.11ac, which was released on December 2013. It has been implemented in various devices and chipsets including the QSR1000 that has a theoretical throughput of 1700 Mbps [4].

WiGig

WiGig is a wireless technology that is still in development. WiGig is based on the IEEE 802.11ad standard and is established by the Wi-Fi Alliance. In order to promote the WiGig technology the Wi-Fi Alliance launched a new trade association called the WiGig Alliance.

WiGig operates in the unlicensed 60 GHz frequency range and promises data transmission rates up to 7 Gbps [21]. Although the high frequency allows for these high data rates it also comes with its limitations. The higher frequency means a shorter wavelength and a shorter wavelength results in higher attenuation and shorter range. Furthermore, the shorter wavelengths have more difficulty passing through walls and therefore limit the usage indoors.

Bluetooth

Bluetooth is a wireless technology specified in the IEEE 802.15.1 standard. It operates in the unlicensed 2.4 GHz frequency band that is also utilized by other wireless technologies such as Wi-Fi. The low cost, low power and small footprint has made Bluetooth a popular technology [53]. Especially to interconnect different devices in a Personal Area Network (PAN).

The low cost, low power and small footprint make Bluetooth a suitable wireless technology. However, the low throughput when compared to the other technologies make Bluetooth unsuitable for future use in wireless memories.

Conclusion

In Table 2.2 the wireless technologies discussed in this section are compared in terms of maturity, power consumption, data rate and used frequency band. These characteristics can aid in the selection of a suitable technology for the future WMS.

\footnote{Using an access point topology.}
Reviewing Table 2.2, the UWB, TransferJet and Bluetooth technologies have a low power consumption, which is highly preferred for integration in the WMS. However, Bluetooth has a low data rate and UWB technologies are mostly academic research. At this moment TransferJet is a suitable candidate for integration as its power consumption is very low, the data rate is fairly high and the technology is already available as a product. However, a proprietary wireless technology could be implemented to provide in all the needs of a WMS.

Although TransferJet is available on the market it was not available for integration in the proof-of-concept WMS. Likely due to missing agreements between NXP and Toshiba, which manufactures TransferJet chips. The most practical solution for the integration in the system is then the **Wi-Fi** technology. Chips for this wireless technology are in abundance and available in a large range of sizes and with varying characteristics.

---

Table 2.2: Comparison of various wireless technologies for integration in a WMS.

<table>
<thead>
<tr>
<th></th>
<th>UWB</th>
<th>TransferJet</th>
<th>Wi-Fi 802.11n/ac</th>
<th>WiGig 802.11ad</th>
<th>Bluetooth</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maturity</td>
<td>Mostly academic</td>
<td>Product</td>
<td>Product/</td>
<td>Advanced</td>
<td>Product</td>
</tr>
<tr>
<td></td>
<td>research</td>
<td></td>
<td>Product/</td>
<td>development</td>
<td></td>
</tr>
<tr>
<td>Power Consumption</td>
<td>Very low</td>
<td>Very low</td>
<td>High/High</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td>Data Rate (Mbps)</td>
<td>112.5*</td>
<td>560</td>
<td>600/1700</td>
<td>4600</td>
<td>4</td>
</tr>
<tr>
<td>Band (GHz)</td>
<td>3.1 - 10.6</td>
<td>4.2 - 4.76</td>
<td>2.4/5</td>
<td>60</td>
<td>2.4</td>
</tr>
</tbody>
</table>

*UWB is the only technology in this table that presents the application throughput, the other technologies present the physical data rate.
Chapter 3

System Design and Implementation

In this chapter the design and implementation of the proof-of-concept WMS is presented. This proof-of-concept WMS is setup according to the PC WMR pad use case, presented in Section 1.2.2. In this setup a WMR is connected to a PC via a USB connection and is able to mount a WMT as a mass storage device.

The primary tasks of the WMR are to detect the WMT, power the WMT and provide an interface between the WMT and the PC. The primary task of the WMT is to provide the WMR with an interface to the non-volatile memory.

The chapter is organized as follows. In Section 3.1 the design of the WMR is presented. Section 3.2 presents the design of the WMT and finally the complete WMS setup is described in Section 3.3.

3.1 Wireless Memory Reader

This section presents the WMR design, where Section 3.1.1 describes the hardware and Section 3.1.2 describes the software.

3.1.1 Circuit Design

The WMR implements five building blocks that are presented in Figure 3.1. These blocks are: the power transmitter, the NFC reader, the high-speed data channel, the USB peripheral and the controller. Physical connections between the blocks are represented by solid lines and wireless connections are represented by dashed lines.

These building blocks form the basis of the WMR schematic. The complete WMR schematic and layout can be found in Appendix B. All the schematics throughout this thesis are designed in EAGLE PCB designer (v6.5.0).

Controller and USB Stack

The task of the controller is to monitor and manipulate the behavior of the other blocks. Monitoring and controlling the blocks can consume a large amount of resources, in both memory and processing power. Therefore the LPC4337.
is utilized as the controller. This chip is the most powerful processor currently available from NXP. The LPC4337 has a dual core design with a primary Cortex-M4 core, for computing intensive tasks and a secondary Cortex-M0 core, for low power tasks. The controller can operate at a frequency of 204 MHz but can easily be scaled down in order to reduce the power consumption.

The LPC4337 also includes a USB ROM stack with built-in support for the following classes: Communication Device Class (CDC), Human Interface Device (HID), Mass Storage Class (MSC) and Device Firmware Upgrade (DFU). Utilizing this stack reduces the code size and the effort required in building USB applications. In the proof-of-concept WMS the Mass Storage Class is required. This class removes the need for a file system on the WMR, thereby reducing the development time, the code size and allowing for more versatility. Key features of the LPC4337 controller are presented in Table 3.1.

The schematic of the controller block can be found in Figure 3.2. The remaining blocks are connected to the controller (U1) via the SPI, I2C, UART, USB or GPIO peripheral. Finally, a button (S1) is included to reset the controller.
<table>
<thead>
<tr>
<th>Category</th>
<th>Component</th>
<th>Value/Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core Performance</td>
<td>Core</td>
<td>ARM Cortex-M4</td>
</tr>
<tr>
<td></td>
<td>Frequency</td>
<td>204 MHz</td>
</tr>
<tr>
<td></td>
<td>Flash Size</td>
<td>1 MB</td>
</tr>
<tr>
<td></td>
<td>RAM Size</td>
<td>136 kB</td>
</tr>
<tr>
<td>Serial Interfaces</td>
<td>USB</td>
<td>Communication with host</td>
</tr>
<tr>
<td></td>
<td>UART</td>
<td>Debugging</td>
</tr>
<tr>
<td></td>
<td>SSP</td>
<td>Communication with NFC reader and High-Speed Data Channel</td>
</tr>
<tr>
<td></td>
<td>I2C</td>
<td>Power regulator</td>
</tr>
<tr>
<td>Digital Peripherals</td>
<td>SDIO</td>
<td>micro SD card</td>
</tr>
<tr>
<td></td>
<td>GPIO</td>
<td>Various</td>
</tr>
<tr>
<td>Analog Peripherals</td>
<td>ADC</td>
<td>Voltage metering</td>
</tr>
</tbody>
</table>

Table 3.1: Key features of the LPC4337 controller [38].

Figure 3.2: Schematic of the controller used in the WMR.
The task of the NFC reader is to detect and read the NFC tag (located on the WMT) when it enters the magnetic field generated by the NFC reader. The requirement for an NFC reader and NFC tag comes forth from the need to detect devices without enabling the power transfer, as this can overload and permanently damage certain devices. These devices are mainly other tags operating on the same frequency (i.e., NFC tags).

The NFC reader can communicate passively with NFC tags by powering the NFC tag with the magnetic field generated by the NFC reader itself. The NFC tag utilizes active load modulation [19, chp.2] to dampen the transmission voltage at the NFC reader thereby transmitting data in the form of backscatter. So before enabling the wireless power transfer it can be confirmed that the device in the magnetic field is an authentic WMT. Otherwise, the power transfer is not enabled, thereby protecting the device from overloading.

As NXP is interested in using their own technology in the WMS to boost future sales, an NFC reader from NXP has to be implemented. Fortunately, NXP has a wide range of NFC readers available with varying operating distances, supporting protocols, and power requirements. An overview of the various NFC readers is given in [6]. The reader should have a minimum operating distance of 30 mm and it should be able to support the ISO/IEC 14443 protocol, used for most contactless cards. The PN512 [41] NFC reader fits all of those characteristics and is suitable for implementation in the WMS. The key features of the PN512 are presented in Table 3.2 and the schematic of the NFC reader is presented in Figure 3.3. The left part of the schematic shows the actual PN512 IC (IC2). The right part shows the coil, the tuning circuit, the EMC filter, and the detuning circuit. The PN512 is connected to the controller via an SPI interface and several test points are added for debugging purposes.

The performance of the reader circuit and in particular the operating distance highly depends on how well the system is tuned. With [37], the correct values for the tuning circuit and the EMC filter can be calculated. First, the coil inductance, resistance, and parasitic capacitance have to be measured. The NFC reader coil is wound from 0.75 mm² thick copper wire with 5 turns. The coil has an inductance of 2 µH (L), a resistance of 0.047 Ω (R₀) and a capacitance of 10 pF (C₁). The resulting Q factor, calculated with (2.5), is 3625.53. This value is well above the required 35 [37]. To lower it external damping resistors have to be inserted on both sides of the coil. The calculation for the damping

<table>
<thead>
<tr>
<th>Category</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standards</td>
<td>ISO/IEC 14443 A/B, ISO18092, Peer-to-Peer and FeliCa</td>
</tr>
<tr>
<td>Operating Distance</td>
<td>50 - 100 mm</td>
</tr>
<tr>
<td>Bit Rate</td>
<td>424 kbps</td>
</tr>
<tr>
<td>Interfaces</td>
<td>Serial, I2C, SPI, S2C and 8 bit parallel</td>
</tr>
</tbody>
</table>

Table 3.2: Key features of the PN512 NFC reader [41].
The calculated damping factor should be 2.41 Ω. However, 2 Ω resistors for R27 and R28 are close enough. The next step is to determine the values of the parallel equivalent circuit

\[ R_q = 0.5 \left( \frac{\omega L}{35} - R_l \right). \]  

\[ (3.1) \]

Calculating the equivalent resistance with the known parameters results in a value of 5965.92 Ω. For the EMC filter components, the recommended values in [37] will suffice. These are 220 nF (\(C_0\)) for C22 and C23, and 560 nH (\(L_0\)) for L2 and L3. The next step is to calculate the components of the matching circuit (C8, C9, C27 and C28). First the impedance of the matching circuit can
be calculated with the following equations \[Z_{tx} = R_{tx} + jX_{tx}, \quad (3.3a)\]
\[R_{tx} = \frac{R_{\text{match}}}{(1 - \omega^2 L_0 C_0)^2 + (\omega R_{\text{match}} C_0)^2}, \quad (3.3b)\]
\[X_{tx} = \frac{2\omega L_0 (1 - \omega^2 L_0 C_0) - \frac{R_{\text{match}}^2 C_0}{2}}{(1 - \omega^2 L_0 C_0) + (\omega R_{\text{match}} C_0)^2} \quad (3.3c)\]

where \(R_{tx}\) is the real part of the impedance, \(X_{tx}\) is the imaginary part and \(R_{\text{match}}\) is the matching resistance of the reader IC. According to [41] the matching resistance is 40Ω. Inserting the proper values in these equations leads to the values 263.67Ω and -32.37Ω, for the real and imaginary part respectively.

The components C8 and C9 can be approximated with [3.4b] and C27 and C28 can be approximated with [3.4a] and are expressed as
\[C_{8,9} \approx \frac{1}{\omega \left(\sqrt{R_{tx} R_{eq}} \frac{R_{eq}}{4} + \frac{X_{tx}}{2}\right)}, \quad (3.4a)\]
\[C_{27,28} \approx \frac{1}{\omega^2 L_{eq}} - \frac{1}{\omega \sqrt{\frac{R_{eq} R_{eq}}{4}}} - 2C_{eq} \quad (3.4b)\]

Inserting the previously calculated values results in a value of 19.21 pF for C27/C28 and 139.04 pF for C8/C9. As this is an approximation, the values of 20 pF and 140 pF will suffice.

**High Speed Data Channel**

A separate high-speed data channel is required due to the unpractical bit rates associated with NFC systems. According to Section 2.4.2 the most practical wireless technology is Wi-Fi. Multiple Wi-Fi modules are available on the market, but not all are suited. The Wi-Fi module should include a software stack to reduce code complexity and size. To realize a working model in the short time window the coding effort for this block should be minimal. Therefore a Wi-Fi module and an NXP controller must be integrated onto a single evaluation board, which will minimize the effort in porting the application. The only Wi-Fi module fitting these descriptions is the CC3000 [52] developed by TI. The key features of the CC3000 can be found in Table 3.3. In Figure 3.4 the schematic of the CC3000 Wi-Fi module (U4) can be found. The CC3000 is connected to the controller via an SPI bus. Test points and breaker circuits have been added for debugging purposes.
<table>
<thead>
<tr>
<th>Category</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standards</td>
<td>IEEE 802.11b/g</td>
</tr>
<tr>
<td>RF performance</td>
<td>Tx power: +20 dBm @11 Mbps (CCK) Rx sensitivity: -89 dBm @11 Mbps (CCK)</td>
</tr>
<tr>
<td>Wi-Fi security modes</td>
<td>WEP, WPA/WPA2 (AES and TKIP - Personal)</td>
</tr>
<tr>
<td>Embedded networking software</td>
<td>TCP/IP stack (IPv4 - DHCP client, DNS, ARP), Wi-Fi driver, embedded security supplicant, Auto transmit calibration</td>
</tr>
<tr>
<td>Throughput</td>
<td>TCP: 4 Mbps, UDP: 7 Mbps</td>
</tr>
<tr>
<td>Connections</td>
<td>4 sockets (UDP or TCP)</td>
</tr>
</tbody>
</table>

Table 3.3: Key features of the CC3000 Wi-Fi module [52].

Figure 3.4: Schematic of the CC3000 Wi-Fi module used in the WMR.

Power Transmitter

The power transmitter is one of the key elements in the WMRs design, as this will generate the magnetic field required to power the WMTs. There are two basic components required for the power transmitter: an DC-AC converter and
Table 3.4: Power requirement of the WMT for both typical and maximum power required by the major power consuming components.

<table>
<thead>
<tr>
<th>Component</th>
<th>Typical Power (mW)</th>
<th>Maximum Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Controller</td>
<td>85.8</td>
<td>247.5</td>
</tr>
<tr>
<td>Wi-Fi Module</td>
<td>684</td>
<td>745.2</td>
</tr>
<tr>
<td>microSD Card</td>
<td>330</td>
<td>330</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>1099.8</strong></td>
<td><strong>1322.7</strong></td>
</tr>
</tbody>
</table>

a power amplifier/regulator. The DC-AC converter generates the AC wave for the magnetic field and the power amplifier/regulator will supply ‘sufficient’ power to the magnetic field. First the minimum power requirement has to be obtained to determine what ‘sufficient’ power is.

The three major power consumers in the WMT are the controller, the Wi-Fi module and the memory (micro SD card). The power consumption of these three components forms the minimum power requirement. Other components are not taken into account as they present only a very small fraction of the total power consumption. The power requirement is presented in Table 3.4 and is divided in a typical power consumption and a maximum power consumption. The typical power consumption of the WMT is 1099.8 mW, this is the minimum power requirement for the WMT to become operational. To guarantee safe operation, the WMT requires a minimum of 1322.7 mW.

The power transmitter should supply enough power to meet the minimum power requirements of the WMT. Meaning that the power level transmitted should reach at least the minimum power requirements. However, it is unlikely that the power transfer efficiency is a 100% so the power levels at the power transmitter should be higher.

Properly designing the power transmitter can lead to high efficiencies and enable high power transfer [49]. To find a suitable power transmitter design, experiments are conducted to measure the power transfer. In this section the power transfer results are briefly discussed to verify the design of the power transmitter the experimental results are discussed in detail in Section 4.1.1.

The first experiment evaluates the suitability of current NFC readers as power transmitters. Utilizing an NFC reader as both a reader and a power transmitter will likely reduce the cost, footprint and power consumption when compared to a design where the two are separated.

The wide range of available NFC readers from NXP also contains a family of high output readers [6]. The CLRC663 [39] is part of this family and supports a large variety of protocols. This NFC reader will be the starting point of this experiment, its key features are presented in Table 3.5.

In this experiment the peak of the power transfer lies at 58.7 mW (see Figure 4.2a), far below the targeted 1099.8 mW. Furthermore, the low Q factors in this system (see Table 4.1a) makes it difficult to achieve high efficiencies. Therefore the NFC reader is not suitable to be used in the WMS as a power transmitter.
<table>
<thead>
<tr>
<th>Category</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standards</td>
<td>ISO/IEC 14443 A/B, ISO18092, ISO 15693 and FeliCa</td>
</tr>
<tr>
<td>Operating Distance</td>
<td>120 - 160 mm</td>
</tr>
<tr>
<td>Bit Rate</td>
<td>424 kbps</td>
</tr>
<tr>
<td>Interfaces</td>
<td>RS232, I2C and SPI</td>
</tr>
</tbody>
</table>

Table 3.5: Key features of the CLRC663 NFC reader [39].

Having excluded NFC readers leads to the separation of the NFC reader and power transfer components. A separate power transmitter will make power scaling easier, but the separation will increase the footprint and the power consumption.

In [33] three power transmitter designs are discussed: a single-ended class-E oscillator design, a cross-coupled oscillator design and conventional class-E power amplifier design. The authors of the paper concluded that both power oscillators outperformed the conventional class-E power amplifier by achieving higher link efficiencies. Furthermore, the cross-coupled oscillator achieved even higher efficiencies than the single ended class-E oscillator, making this the preferred design for the WMS.

The cross-coupled oscillator can be classified under the category of LC circuit Voltage Controlled Oscillators (VCOs). These types of VCOs are very common in high-speed systems. The simple but symmetric configuration allows for high-speed and differential designs with large swing, reasonable tuning range, and low power consumption [27]. In Figure 3.5 a basic cross-coupled oscillator design is illustrated.

![Figure 3.5: Basic cross-coupled oscillator design](image)

The center-tapped coil $L_1$ forms an LC circuit together with capacitor $C_1$. The combination of this LC circuit and the N-channel MOSFETs form the cross-coupled oscillator, with the oscillation frequency expressed as [27]

$$\omega_{\text{osc}} = \frac{1}{\sqrt{L_1 C_1}}. \quad (3.5)$$

With (3.5) the oscillator can be tuned to the resonant frequency of the system.
However, for high frequencies the tuning capacitor $C_1$ becomes low (around 140 pF for a 13.56 MHz system with a 1.7 $\mu$H coil) and the output capacitance of the MOSFETs begin to play a role, making it difficult to tune the transmitter.

The second power experiment evaluates this cross-coupled oscillator design and verifies whether it is possible to properly tune it to a frequency of 13.56 MHz.

The peak power transfer in this experiment is measured at 1266.5 mW (see Figure 4.2b). Thereby meeting the minimum power requirement of 1099.8 mW and proving that the cross-coupled oscillator design is capable of supplying sufficient power.

In Figure 3.6, the final schematic of the power transmitter is illustrated. This schematic shows the cross-coupled oscillator with a center-tapped coil $L_1/L_2$ and the parallel capacitance $C_{37}$. Furthermore, to indicate the transmitted power level, a small circuit (surrounding $T_1$) is added. The brightness of LED1 increases when more power is used in the cross-coupled oscillator. To stop the power transfer the controller can disable the oscillator with the GPIO peripheral. Finally, the input voltage of the power transmitter can be measured with the ADC peripheral.

For the third and final power experiment a transmitter and receiver prototype is designed and fabricated. The schematics and layout of these prototypes can be found in Appendix A. The prototype transmitter is the forerunner of the power transmitter schematic illustrated in Figure 3.6. This experiment evaluates the power indicator, voltage metering and the impact of the dual coil design caused by the separation of the NFC reader and power transmitter. The peak power transfer in this experiment is measured at 2450 mW (see Figure 4.2c), well above the safe operating power requirement of 1322.7 mW. Thereby proving that the dual coil design functions. Again, more detailed results can be found in Section 4.1.1.

The final step in designing the power transmitter, is to make it suitable for multiple and varying types of WMTs. To do this the WMR must be able to regulate the power transfer to the WMTs. To do so, a simple regulation scheme

![Figure 3.6: Schematic of the power transmitter used in the WMR.](image)
is built around a high efficiency (95%) variable regulator (IC3: TSR 3-24150). The schematic of the power regulator can be found in Figure 3.7.

Figure 3.7: Schematic of the power regulator used in the WMR.

To regulate the power transfer, the voltage regulator (IC3) adjusts the output voltage downwards with respect to the input voltage. This will lower the voltage in the power transmitter circuit (V+) and thereby lower the power. The voltage regulator requires a reference voltage to stabilize the output voltage. Adjusting this reference voltage will adjust the output voltage. With a digital potentiometer (U2: AD5110) the reference voltage can be adjusted by increasing/decreasing the resistance. The digital potentiometer is controlled by the controller via an I2C interface. The voltage operating range of the voltage regulator now lies between 0 and 15 V. However, the power transmitter requires a minimum of 9 V to bring the MOSFETs T2 and T3 into a conducting state. So the effective range of the power regulator schematic lies between 9 and 15 V. Furthermore, the WMR utilizes a high efficiency (85.5%) 3.3 V regulator (IC1: OKI-78SR-3.3) to power the controller, NFC reader and Wi-Fi module. Finally, the WMR is powered by a 18 VDC source via connector J1 and is protected against reversing the polarity with D1.

3.1.2 Software Flow

As stated in the previous section, the task of the controller is to monitor and manipulate the behavior of the WMR. In this section the controller software is presented. The software is written in the programming language C, in the LPCExpresso IDE (v7.2.0). The libraries utilized by the controller are the NFC reader library (v2.1), the CC3000 library, the Redlib library (v2) and the LPCOpen library (v2.9). The NFC reader library controls the PN512 NFC reader and is originally build for NXP microcontrollers with a Cortex-M0 core so effort had to be made to port this library to the Cortex-M4 core used in the LPC4337. The CC3000 library is only used as a low level interpreter of the Wi-Fi module, as the high level functions like UDP, TCP, etc. are built into the software stack of the CC3000. However, effort had to be made to port
this library to the LPC4337 controller. The Redlib library is a proprietary C90 runtime library that is smaller than the normal GNU C library, in terms of code size, and is better suited for embedded applications. The Reblib library is provided by the LPCExpresso IDE. The last library is the LPCOpen library, which is actually an open source development platform for NXP microcontrollers that provides users with various low-level drivers to reduce the coding effort and required knowledge of the microcontroller.

The controller software is divided into two phases: a detection phase and an operational phase. Figure 3.8 illustrates the flowchart of the detection phase. This flowchart and the flowcharts throughout the thesis are drawn with the Ipe extensible drawing editor (v7.2.0).

The first step of the controller software is to initialize the peripherals, such as the GPIO, ADC, SPI, I2C, clocks and timers. In the initialization also the NFC reader and Wi-Fi module are configured using the designated libraries. After the initialization the detection phase is entered. In this phase the controller will activate the NFC reader and send out a beacon every second.
Listing 3.1: Reset RF field, apply protocol and transmit beacon.

This beacon is actually a sine wave with a frequency of 13.56 MHz. When an NFC enabled device is close enough to receive this beacon, it is powered by this beacon and the contents of the device are read. The contents are then analyzed to determine whether the NFC enabled device is an authentic WMT. The controller will search the content for the key "WMT" to establish if this device is a WMT as can be seen in Listing 3.2, line 1. After the NFC device has been authenticated as a WMT, line 8 and 10 of Listing 3.2 will initiate the power transfer.

Listing 3.2: Establish WMT authenticity and initialize power transfer.

In line 34 of Listing 3.3 the WMR pushes a device size request to the WMT. When the WMT replies to this request it will provide the WMR with its memory capacity. The nr_blocks variable in line 18 will contain the memory capacity as the amount of 512 byte blocks of the WMT. The WMR will check this value to make sure the memory capacity of the WMT is not larger than 2 GB. This limitation is set by the USB ROM stack included in the controller. If the memory capacity is less or equal to 2 GB the WMT is connected to the WMR and is mounted as a mass storage device in line 53. If the memory capacity is higher, the WMR will return to the detection phase.

If the WMT does not reply to the initial device size request the WMR will retransmit the request after ten seconds, with a maximum of three attempts. When this limit is passed the WMR will return to the detection phase.
```c
int8_t mount_tag(void) {
    ErrorCode_t ret = LPC_OK;
    uint32_t timer = 0;
    uint32_t nr_blocks = 0xFFFFFFFF;
    uint8_t mount_buffer[5];
    uint8_t retries = 0;

    /* Prepare buffer */
    mount_buffer[0] = 's';
    /* Padding */
    mount_buffer[1] = 0;
    mount_buffer[2] = 0;
    mount_buffer[3] = 0;
    mount_buffer[4] = 0;
    /* Wait for device size */
    while(nr_blocks == 0xFFFFFFFF) {
        /* Check for received data */
        nr_blocks = UDP_NrBlocksReceived();
        /* Timer is set to 10s */
        if(!timer)
            timer = Chip_RIT_GetCounter(LPC_RITIMER);
        else if(((Chip_RIT_GetCounter(LPC_RITIMER) - timer) >= (SYSTICK_MS * 10000))) {
            toggle_Green_LED();
            /* After 3 attempts tag is potentially removed */
            if(retries >= 3) {
                /* Reset tag detected flag */
                setTagDetected(0);
                return ERR_FAILED;
            }
            else {
                retries++;
            }
        /* Re-transmit */
        UDP_Tx((char*)mount_buffer, 5);
        /* Reset timer */
        timer = 0;
    }
    /* Number of blocks check (max. 2GB cards) */
    if(nr_blocks > 4194304) {
        /* Reset tag detected flag */
        setTagDetected(0);
        return ERR_FAILED;
    }
    /* Connect as mass storage device */
    ret = mscDisk_init(g_hUsb, &desc, &usb_param, nr_blocks);
    if (ret == LPC_OK) {
        /* Set USB interrupt priority */
        NVIC_SetPriority(LPC_USBIRQ, 3);
        /* Enable USB interrupts */
        NVIC_EnableIRQ(LPC_USBIRQ);
        /* Now connect */
        USBD_API->hw->Connect(g_hUsb, 1);
    }
    return ret;
}
```

Listing 3.3: Push device size command and check memory capacity. When a suitable WMT is connected the WMR mount the WMT as a mass storage device.

When the WMT is mounted, the operational phase is entered. The flowchart of this phase is illustrated in Figure 3.9. In the operational phase the USB
interrupt handler will execute the primary tasks like processing read and write requests from the host. The USB interrupt handler is triggered when a request is made from a host (e.g. PC) to either read or write data. The interrupt following the request can either be a bulk read or a bulk write. Bulk transfers are typically used to transfer large amounts of data. The maximum packet size for bulk transfers is 64 bytes for full-speed USB and 512 bytes for high-speed USB. Due to the 512 byte block sizes used in the NVM the high-speed USB allows for direct writing and reading of the data blocks.

When a user wants to open a file, the file system will request a bulk read. At this time the USB stack will generate a bulk read interrupt and will jump to the read function on line 2 of Listing 3.4. In line 17 the WMR pushes a read request to the WMT with the block address from the initial request. The block address is a 32 bit word and will be split up in four bytes. When the requested data block is obtained from the WMT, it is pushed to the USB handler on line 39, which directs is to the host. If the requested data block is not obtained within two seconds after transmission, the request is re-transmitted. When the number of retries has reached three in line 25, the WMT is unmounted and the WMR will return to the detection phase.
/** USB device mass storage class read callback routine */
static void translate_Rd(uint32_t offset, uint8_t *buff_adr,
    uint32_t length, uint32_t hi_offset) {
    uint32_t block_num = 0;
    uint32_t timer = 0;
    uint8_t retries = 0;

toggle_Blue_LED();
    /* Prepare read buffer */
    packet_buffer[0] = 'r';
    /* Block number */
    block_num = offset / 512;
    packet_buffer[1] = block_num & 0x000000FF;
    packet_buffer[2] = (block_num & 0x0000FF00) >> 8;
    packet_buffer[3] = (block_num & 0x00FF0000) >> 16;
    packet_buffer[4] = (block_num & 0xFF000000) >> 24;
    /* Transmit offset */
    UDP_Tx((char*)packet_buffer, 5);
    /* Wait until data is received */
    while (!UDP_Data_Received()) {
        /* Timer is set to 2s */
        if (!timer)
            timer = Chip_RIT_GetCounter(LPC_RITIMER);
        else if (((Chip_RIT_GetCounter(LPC_RITIMER) - timer) >= (SYSTICK_MS * 2000))
            /* After 3 retries dismount tag */
            if (retries >= 3) {
                unmount_Tag();
                return;
            } else {
                retries ++;
            }
        /* Re-transmit */
        UDP_Tx((char*)packet_buffer, 5);
        /* Reset timer */
        timer = 0;
    }
    /* Copy data */
    memcpy(buff_adr, SSUDP_RX_BUFFER, 512);
}
Listing 3.4: Transmit read request with block address and wait for data block.

During the bulk write the WMR receives a block address and the data block from the USB handler. In line 22 of Listing 3.5 the data block is copied to the packet_buffer and pushed with the request identifier and the block address to the WMT. In line 26 the WMR waits for an acknowledgement from the WMT concluding a successful write action. If no acknowledgement is received the write request will be re-transmitted. When the retry limit of three is passed the WMT will again be unmounted and the WMR will return to the detection phase.
Listing 3.5: Transmit write request with block address and block data and wait for acknowledgement.

When there is no data exchange during the operational phase, the WMR will transmit a message to the WMT every ten seconds to check whether the WMT is still present and connected. In line 15 of Listing 3.6, the WMR will check for a response from the WMT. When the WMT responds to the message, normal operation will continue. When the timer, in line 19, expires it can be assumed that the WMT is removed or the connection with the WMT has been lost. The WMR will unmount the WMT in line 22 and will return to the detection phase, where it again will wait for an NFC enabled device. In the case the WMT is still present, the connection will be re-established and data can once again be exchanged between the WMR and the WMT.

45
Listing 3.6: Check connection with the WMT.

3.2 Wireless Memory Tag

This section presents the WMT design, where Section 3.2.1 describes the hardware and Section 3.2.2 describes the software.

3.2.1 Circuit Design

Five building blocks are required for the WMT: the power regulator, the controller, the NFC tag, the high-speed data channel and the non-volatile memory. These blocks are illustrated in Figure 3.10 and form the basis of the WMT.
schematic. The complete WMT schematic and layout can be found in Appendix C.

Figure 3.10: Block diagram illustrating the major building blocks of the WMT and the placement of the WMT in the WMS.

The various building blocks should remain simple to make the WMT reliable, low cost and energy efficient. Although this is only a proof-of-concept WMS, this simplicity is maintained where possible.

**Power Regulator**

The power regulator block has two primary functions: to rectify the AC voltage and to regulate the rectified voltage. Rectifying circuits can perform either half-wave or full-wave rectification [12]. In half-wave rectification only a single half of the input waveform is passed resulting in a lower output voltage, when compared to full-wave rectification. Furthermore, the half-wave rectifiers produce more ripple and require more filtering than full-wave rectifiers. However, the half-wave rectifier only requires a single diode, making it the simplest rectifier. None-the-less, half-wave rectifiers are not commonly used in power applications.

In full-wave rectification both halves of the input waveform are passed, yielding a higher output voltage. Two designs are common in full-wave rectification: the bridge rectifier and the center-tapped rectifier [12]. The bridge rectifier, illustrated in Figure 3.11a, requires four diodes and the center-tapped rectifier, illustrated in Figure 3.11b, requires two diodes thereby reducing the voltage drop over the rectifier. However, the center-tapped design requires a center-tapped coil, which is more complex to fabricate. Also to obtain the same output voltage

1 Only single-phase rectifiers are taken into consideration as the transmitter design allows for only single-phase rectification.
the center-tapped rectifier requires twice as many turns in the coil because the
coil is essentially cut in half. The relationship between the number of turns and

\[
\frac{V_s}{V_p} = \frac{N_s}{N_p},
\]

(3.6)

where \(V_s\) is the voltage over the secondary coil, \(V_p\) is the voltage over the primary
coil, \(N_s\) is the number of turns on the secondary coil and \(N_p\) is the number of
turns on the primary coil. The RMS voltage for a half-wave rectifier and a
full-wave rectifier respectively [12]

\[
V_{\text{rms},h} = \frac{V_{\text{pk}}}{2},
\]

(3.7a)

\[
V_{\text{rms},f} = \frac{V_{\text{pk}}}{\sqrt{2}},
\]

(3.7b)

where \(V_{\text{rms}}\) is the root mean square voltage and \(V_{\text{pk}}\) is the peak voltage. From
the output voltage of a full-wave rectifier is higher,
therefore achieving a higher energy efficiency in the WMT. Depending on the
application, either a bridge rectifier or a center-tapped rectifier can be used. In
the WMS a center-tapped rectifier is required because the power transmitter in
the WMR utilizes a center-tapped coil. To keep the (secondary) input voltage
within operating boundaries a low number of turns in the secondary coil is pre-
ferred. Using a center-tapped coil is the best solution to reduce the number of
turns. According to (3.6), one could also increase the number of turns on the
primary side or decrease the voltage on the primary side. However results show
that both have a negative effect on either the received power or the tuning of
the power transmitter.

After the AC voltage has been rectified it is regulated to 3.3 V, which is re-
quired for the controller, NVM and the Wi-Fi module. In order to keep the
regulator design simple, low cost and small, a low-dropout (LDO) regulator is
used. The chosen LDO regulator is the LT1129-3.3 [28]. Figure 3.12 illustrates
the schematic of the rectifier (D2), the power regulator (IC1) and the LC circuit
used for tuning the WMT.
NFC Tag and Non-Volatile Memory

The NFC tag and the NVM are the last two building blocks of the WMT. The NFC tag (NT3H1201 [40]) holds the identification key ("WMT") in order for the WMR to establish that this device is a WMT. However, the NFC tag can also hold information about the memory capacity, file system, security, etc. Also the WMR can write data to the NFC tag that can later be read by the WMT controller. The WMR could store information like security keys for setting up a secure link between the WMR and the WMT. When the NFC tag is powered by the regulator, the controller can retrieve this data via an I2C interface. The schematic of the NFC tag is presented in Figure 3.13.

Figure 3.13: Schematic of the NFC tag and circuitry used in the WMT.
The NFC tag also requires a detuning circuit to protect it from overloading during the power transfer. The detuning is activated when the voltage (V+) at the power coil reaches the breakdown voltage (2.7 V) of zenerdiode D1.

Finally, the NVM is a vital part of the WMTs design. In Section 2.4.1 a discussion is presented about possible technologies suitable for a wireless memory. This discussion concluded that NAND flash is still the most practical technology due to the high density and its maturity [2.4]. Furthermore, NAND flash is mass produced leading to a low cost per bit and wide availability. Other technologies can out perform NAND flash in terms of energy efficiency and speed but are still under development.

For the proof-of-concept WMS a micro SD card is implemented as the main flash memory for storing data. The micro SD card is connected to the controller via the SDIO interface. The schematic is presented in Figure 3.14.

3.2.2 Software Flow

The primary task of the WMT is to provide the WMR with access to the NVM located on the WMT. The software for the WMT is also written in the programming language C and in the LPCExpresso IDE. The controller utilizes the CC3000 library, the Redlib library and the LPCOpen library. To assist the software description, flowcharts and code snippets are added throughout the section. Figure 3.15 illustrates the flow of the WMT software.

Even before initialization the contents of the NFC tag on the WMT, are read by the WMR in order to determine whether the device is an authentic WMT. The NFC tag is a separate part of the WMT and is powered by the field of the NFC reader. Using the TagInfo and TagWriter applications for Android the contents of the NFC tag can easily be read and altered. Figure 3.16a illustrates the TagInfo application on an NFC tag with cleared contents and Figure 3.16b illustrates the TagInfo Application on an NFC tag containing the "WMT" key. This key is used to establish the NFC enabled device as an authentic WMT.
After establishing the authenticity of the WMT, the WMR initiates the power transfer. At this point the microcontroller is powered and the WMT can start its initialization procedure. The next step is to connect to the WMR via the high-speed data channel. After establishing the connection, the WMT waits for the reception of a packet from the WMR. When a packet is received, it is decoded and, depending on the data in the command field, a follow-up action is taken. Possible commands are: read command ('r'), write command ('w') and device size command ('s').

```c
/* Socket initialized? */
if ((SS_RecvUdpSocket != 0xFFFFFFFF) && (SSUDP_Listening)) {
  if (Wifi_IsConnected()) {
    retVal = recvfrom(SS_RecvUdpSocket, SSUDP_RX_BUFFER, sizeof(SSUDP_RX_BUFFER), 1, (sockaddr *)&tSocketAddr, &tRxPacketLength);
    /* Packet received? */
    if (retVal > 4) {
      /* Get the block number */
      block_num = SSUDP_RX_BUFFER[1];
      block_num |= SSUDP_RX_BUFFER[2] << 8;
      block_num |= SSUDP_RX_BUFFER[3] << 16;
      block_num |= SSUDP_RX_BUFFER[4] << 24;
      /* Switch on command */
      switch(SSUDP_RX_BUFFER[0]) {
        /* Read a block */
        case 'r':
```

Figure 3.15: Flowchart illustrating the behavior of the WMT.
(a) TagInfo application for Android OS illustrating an NFC tag with cleared memory content.

(b) TagInfo application for Android OS illustrating an NFC tag with the "WMT" key written to it.

Figure 3.16: TagInfo application for Android with cleared and written memory.

```
... break;
    /* Write a block */
    case 'w':
        ...
        break;
    /* Get number of blocks */
    case 's':
        ...
        break;
    default:
        break;
    }
} else {
    if (retVal != lastRetVal)
        lastRetVal = retVal;
}
```

Listing 3.7: Receive and decode packet
When the received packet contains a read command the block address in line 3 of Listing 3.8 is used to read the data block from the NVM. In line 5 the data block is posted by the WMT and should be received and processed by the WMR.

```
toggle_Blue_LED();
/* Read block from memory */
Chip_SDMMC_ReadBlocks(LPC_SDMMC, (void*)SSUDP_TX_BUFFER, block_num, 1);
/* Send block */
if (sendto(SS_RecvUdpSocket, SSUDP_TX_BUFFER, 512, 1, &tSocketAddr, sizeof(sockaddr)) == -1) {
    DEBUGOUT("UDP : Failed to send");
}
```

Listing 3.8: Read data block from NVM

When the write command is found the block address in line 3 of Listing 3.9 is used to write the received data block to the NVM. Finally in line 5 an acknowledgement is posted by the WMT signaling to the WMR that the data is written.

```
toggle_Red_LED();
/* Write block to memory */
Chip_SDMMC_WriteBlocks(LPC_SDMMC, (void*)SSUDP_RX_BUFFER[8], block_num, 1);
/* Send acknowledge */
if (sendto(SS_RecvUdpSocket, WRITE_ACK, strlen(WRITE_ACK), 1, &tSocketAddr, sizeof(sockaddr)) == -1) {
    DEBUGOUT("UDP : Failed to send");
}
```

Listing 3.9: Write data block to NVM

When the device size command is pushed to by WMR, the WMT will read the number of 512 byte blocks in line 3 of Listing 3.10. In line 4 to 7 the 32 bit long device size is split into four bytes. In line 9 the device size is transmitted to the WMR.

```
toggle_Green_LED();
/* Get number of blocks */
nr_blocks = (uint32_t)Chip_SDMMC_GetDeviceBlocks(LPC_SDMMC);
SSUDP_TX_BUFFER[0] = nr_blocks & 0x000000FF;
SSUDP_TX_BUFFER[1] = (nr_blocks & 0x0000FF00) >> 8;
SSUDP_TX_BUFFER[2] = (nr_blocks & 0x00FF0000) >> 16;
SSUDP_TX_BUFFER[3] = (nr_blocks & 0xFF000000) >> 24;
/* Send the number of blocks */
if (sendto(SS_RecvUdpSocket, SSUDP_TX_BUFFER, 4, 1, &tSocketAddr, sizeof(sockaddr)) == -1) {
    DEBUGOUT("UDP : Failed to send");
}
```

Listing 3.10: Get number of NVM blocks

### 3.3 System Setup

In this section the completed proof-of-concept system developed during this thesis is presented. The complete proof-of-concept system consists of a WMR, a WMT and a host, which in this case is a PC.
3.3.1 Hardware Setup

The schematics and layout of the WMR and WMT are designed in EAGLE PCB designer. The resulting assembled WMR and WMT PCB’s are illustrated in Figure 3.17. A more detailed illustration of the WMR and the WMT can be found in Figure 3.18a and Figure 3.18b respectively.

Figure 3.17: Assembled WMR PCB (left) and WMT PCB (right) without coils.

The WMR PCB has a size of 83 x 65 mm without the coils. The WMT PCB has a size of 58 x 50 mm, giving it a total area 2900 mm\(^2\). This is considerably smaller when compared to a standard ID-1 card (credit card), which has a size of 85.60 x 53.98 mm and a total area of 4620.69 mm\(^2\), making it 59 % larger than the WMT.

Figure 3.19: Wireless memory system.

The area of the WMT will not increase when the coils are assembled but the area of the WMR will increase when the coils are assembled. The WMR assembly with coils can be found in Figure 3.19a. The outer (square) coil is used for the power transfer and the inner (circular) coil is used for the NFC.
(a) WMR setup as used in the WMS. Key components are: **T1**: LPC4337 microcontroller, **T2**: PN512 NFC reader, **T3**: CC3000 Wi-Fi module, **T4**: OKI-78SR-3.3 regulator, **T5**: AD5110 digital potentiometer, **T6**: TSR 3-24150 variable power regulator, **T7**: connector for the power transfer coil, **T8**: connector for the NFC reader coil, **T9**: micro USB connector, **T10**: programming connector for the microcontroller, **T11**: debugging connector for serial communication, **T12**: reset button for the microcontroller, and **T13**: RGB LED for debugging purposes.

(b) WMT setup as used in the WMS. Key components are: **T1**: LPC4337 microcontroller, **T2**: micro SD card holder, **T3**: CC3000 Wi-Fi module, **T4**: NT2H301 NFC tag, **T5**: LT1129-3.3 LDO regulator, **T6**: connector for the power transfer coil, **T7**: connector for the NFC tag coil, **T8**: programming connector for the microcontroller, **T9**: debugging connector for external power and serial communication, and **T10**: RGB LED for debugging purposes.

Figure 3.18: Detailed WMR and WMT PCB’s.

data transfer. The differently shaped coils reduces the coupling between the two and reduces the influence the coils have on each other. The coils are also assembled in this fashion to keep the total area on the WMT side low, as the WMT will have the same coil setup. Also the WMT orientation, with respect to the WMR, is far less critical when compared to a system with the coils setup side by side, as presented in [9]. Using a larger transmitting coil or multiple coils will allow for more WMTs to be powered by the WMR. However, this would reduce the efficiency as the degree of coupling between the WMR and the WMT drops because a larger portion of the magnetic flux will miss the receiver coil.

Although the coil assembly of the WMT is similar to the coil assembly of the WMR, it does require some special attention. To keep the area of the WMT as small as possible (no larger than 2900 mm$^2$) the coils must be assembled underneath the WMT. However, placing the coils so close to the WMT can cause problems in the WMT when it is placed in the magnetic field of the WMR. The magnetic field can cause currents to flow in the large conductors (i.e. ground plane) on the WMT. These currents are called eddy currents and are a reaction on the force applied by the magnetic field. Eddy currents flow through conductors as a normal current would and will also dissipate energy as heat in the conductor resulting in a power loss. Besides the power loss, the dissipated power can damage components resulting in the failure of the WMT. Therefore, eddy currents are unwanted and steps have to be taken to eliminate
or minimize the eddy currents. There are three methods of doing this: lowering the intensity of the magnetic field by moving the WMT PCB away from the magnetic field, removing the large conductors by either PCB design or using lamination\(^2\) and shielding the WMT PCB from the magnetic field.

![Magnetic field simulations](image)

(a) Magnetic field generated at the transmitter coil without the receiver assembly. The transmitter coil is made from magnetic wire with a diameter of 0.25 mm and 4 turns. Purple is the highest field intensity and blue is the lowest field intensity.

(b) Transmitter coil with receiver assembly at a distance of 2 cm. Receiver assembly consists of a receiver coil and a copper ground plane in the center of the coil. The receiver coil has the same parameters as the transmitter coil and the copper ground plane is 2 mm thick.

(c) Transmitter coil with receiver assembly consisting of a receiver coil, a sheet of ferrite shielding and a copper ground plane. The receiver coil has the same parameters as the transmitter coil and the copper ground plane is 2 mm thick. The sheet of ferrite is 1 mm thick and placed between the receiver coil and the copper ground plane.

Figure 3.20: FEMM simulations.

Lowering the intensity of the magnetic field is not a suited option as the goal is to keep the area of the WMT as small as possible while still receiving sufficient power. Removing the large conductors is also not an option as the micro SD card holder and the W-Fi module are large conductors (see Figure 3.18b) and are not laminated during the production process. The best option is to use shielding to protect the WMT. To understand the magnetic field and the effect of shielding the Finite Element Method Magnetics or FEMM (v4.2) simulation tool is used. FEMM is a finite element package for solving 2D planar and axisymmetric problems in magnetics and electrostatics. In Figure 3.20 three FEMM simulations are presented, the simulations show a cross section view of the magnetics problem. Figure 3.20a presents the magnetic field of a transmitter without the receiver. The field lines from the transmitter coil can extend uninterrupted in all directions but the intensity fades as the distance from the transmitter coil grows. Figure 3.20b presents the magnetic field of a transmitter with the receiver at a distance of 2 cm. Here the receiver is composed of a

\(^2\)Lamination is the technique of manufacturing a material in multiple layers.
receiver coil and a solid copper ground plane centered between the edges of the receiver coil. The field lines extending from the transmitter are clearly influenced by the copper ground plane as this dissipates energy from the magnetic field. In Figure 3.20c, the receiver assembly is altered. Here the receiver coil and the copper ground plane are separated by a sheet of ferrite to shield the copper ground planes from the magnetic field. The ferrite conducts the magnetic field lines away from the copper ground plane and thereby shielding it. The fully assembled WMT contains a coil for the power transfer and a coil for the NFC data transfer with the same setup as in Figure 3.19a. Furthermore, the coils and PCB are separated by a sheet of 0.5 mm thick ferrite.

3.3.2 Software Setup

The initial placement, shown in Figure 3.19b, activates the WMS and initializes the software flow illustrated in Figure 3.21. In this figure the flow of the WMS, including the user actions, can be seen. After the WMT is placed on the WMR, the WMT is identified and verified. After the WMR verified the authenticity of the WMT, the power transfer is initiated and the connection with the WMT is finalized. The WMT is then mounted and presented to the user as a mass storage device. From this point on the user initiates all data exchanges. When the user wants to open a file, the file system on the host will perform a read request to the WMR, which is then pushed towards the WMT. In turn the WMT will respond with the requested data, which is pushed through the WMR to the host.

Writing to a file works in a similar fashion except data is written to the WMT and an acknowledgement is sent from the WMT to the WMR, indicating a successful write to the memory. When the WMT is removed or the connection has been lost, the WMR will unmount the WMT and reports this to the host. From here the WMR will go back to sending beacons to once again, find potential WMTs.
Figure 3.21: Flow of the WMS including the host, WMR and WMT.
Chapter 4

Experimental Results

This chapter presents the setup and results of experiments conducted during the course of this thesis. First, experiments regarding the power transfer and system efficiency are presented. These experiments lead to the final design of the wireless power transfer components in the WMS. These experiments were briefly introduced in Section 3.1.1. Second, the read and write speed measurement results are presented.

4.1 Power

4.1.1 Load Power

A considerable part of this project is delivering a working proof-of-concept WMS. One of the key elements in making this system operational, is the ability to deliver sufficient power to the WMT. The power requirements of the WMT can be found in Table 3.4. The following experiments were conducted in order to determine whether these power levels could be transferred from the WMR to the WMT and to evaluate various designs for the power transfer system.

Power Experiment 1

The first power experiment is conducted to evaluate the suitability of a current NFC reader for both NFC data transfer and power transfer. The experimental setup is as follows. The power transmitter is a CLEV663B evaluation board, which includes the CLRC663 high output reader [39] to generate the magnetic field for power and data transfer. The receiver is an altered CLEV663B evaluation board, where the CLRC663 reader has been replaced by an add-on board containing a full-wave bridge rectifier [12], a variable load and a potential tuning capacitor. The schematic of the add-on board can be found in Figure 4.1. The full-wave bridge rectifier is assembled from four 1N4148 diodes and a potentiometer with a resistance from 0 to 10 kΩ is used as the variable load. To evaluate the power transfer, the power dissipated in the variable load is measured.

The link parameters of this experiment are presented in Table 4.1a and measurement results are presented in Figure 4.2a. This figure shows the power for both resonant and non-resonant operation. In resonant operation the receiver
Table 4.1: Link parameters for the first 4.1a, second 4.1b and third 4.1c power experiment.

(a) Power experiment 1. (b) Power experiment 2. (c) Power experiment 3.

is tuned to the same resonant frequency as the transmitter. Tuning the receiver can be done with capacitor C1 in Figure 4.1. In non-resonant operation the receiver is not tuned to the resonant frequency but operates at the self-resonant frequency of the coil.

In Figure 4.2a both the resonant and non-resonant power transfer show a similar line but the resonant power transfer maintains higher power levels for a larger portion of the load variation. The similarity between the resonant and non-resonant power transfer is due to the low Q factor of the coils, which reduces the effect of resonance. The peak power at the load is 58.7 mW, which is far below the targeted 1099.8 mW (see Table 3.4). These results conclude that the NFC reader is not suited as a power transmitter for this WMS.

Power Experiment 2

At this point it is clear that the NFC reader is not suited for this WMS. Separating the NFC reader and the power transmitter is the only option and lead to the power transmitter discussed in Section 3.1.1. This second power experiment utilizes this separate power transmitter. The setup of this experiment is as follows. The add-on board 4.1 of the first power experiment is also used here but the coils have been replaced to better suit this experiment. The link parameters
Power Experiment 3

The next goal is to ensure safe operation of the WMT by achieving the minimum power requirement of 1322.7 mW (see Table 3.4). For the third and final power experiment a transmitter and receiver prototype is designed and fabricated. The schematics and layout of these prototypes can be found in Appendix A. These prototypes are used to verify the design before implementing them in the proof-of-concept WMS. The transmitter prototype is designed for higher input voltages resulting in a higher output power. The receiver prototype utilizes a center-tapped rectifier, an optional 3.3 V regulator, a potential tuning capacitor, an NFC tag, a variable load and detuning hardware. This experiment will test the power transfer, the dual coil design and the detuning capabilities of the prototypes.

The link parameters can be found in Table 4.1c. The dissipated power in the variable load is measured and the results are presented in Figure 4.2c. The results show that the peak power of both the single coil (2381 mW) and dual coil design (2450 mW) are well above the safe operating power of 1322.7 mW. The dual coil design does have a slightly negative impact on the power transfer after the peak. This is likely due to the detuning effect of the coil required for the NFC tag. None-the-less the dual coil design can provide ample power and the detuning of the NFC tag circuitry will protect it from overloading.
4.1.2 System Efficiency

The previous experiments concluded that the power transfer components in the WMS are able to supply the WMT with the minimum power requirement. However, it is important to know at what efficiency this power transfer is possible. A low system efficiency would imply that energy is lost and a lot more energy has to be transmitted in order to achieve the power requirement. Let’s assume that the RF power transfer system discussed in [17] has been implemented instead of the inductively coupled system. This system has a link efficiency of 0.8%. For the WMT to receive a minimum of 1099.8 mW the WMR would have to transmit a 137.48 W, which would not be realistic and would violate regulations. Let’s go back to the original inductively coupled system.

In Section 2.1.3 the efficiency requirement was set to 50% in order to avoid these issues. The goal of this experiment is to reach or surpass the 50% mark. The experiment uses the same setup as the third power experiment presented.
in Section 4.1.1. The system efficiency is determined by calculating the ratio between the input power and the output power and is expressed as

$$\eta_{sys} = \frac{P_{load}}{P_{input}},$$

where $P_{load}$ is the power measured at the load on the receiver side and $P_{input}$ is the power measured at the input of the transmitter. The system efficiency for various loads is illustrated in Figure 4.3. Furthermore, a distinction is made between the single and dual coil design.

![Figure 4.3: System efficiency for a single coil design and a dual coil design.](image)

The results show the same behavior as with the last power experiment where the dual coil design has a slightly negative impact on the performance, as expected. However, both the efficiency of the single and dual coil design peak above the required 50%. The peak efficiency for the dual coil design is measured at 59% and for the single coil design at 69%. Although the dual coil design has a slightly negative impact on the performance of the wireless power transfer, it is within the set boundaries and suitable to be utilized in the proof-of-concept WMS.

### 4.2 Transfer Speed

The final experiments concern the data transfer speeds of the proof-of-concept WMS. This is an important characteristic as the wireless memory should be able to support high data rates for convenient content sharing. However, as this concerns a proof-of-concept WMS high data rates are not crucial.

There are three interfaces in the WMS that could form a potential bottleneck for data transfer. These are the USB interface, the Wi-Fi module and the SDIO interface. The most unlikely bottleneck is the USB interface that is provided by the USB ROM stack in the controller. The controller is able to provide both
Hi-Speed and Full-Speed USB interfaces with Direct Memory Access (DMA) support. The Full-Speed USB interface is able to transfer data at 12 Mbps and the Hi-Speed interface is capable of even higher data rates.

The two most likely bottlenecks are the SDIO interface and the Wi-Fi module. In Table 3.3 the maximum throughput of the Wi-Fi module is 4 Mbps for a TCP connection and 7 Mbps for a UDP connection. The throughput is higher for UDP packets because there is no error checking done for these packets. However, this throughput is measured in ideal conditions and with the maximum packet size. The measured throughput for a UDP packet, containing 512 bytes of data and using WPA2 security, is approximately 4 Mbps or 500 kBps.

The last possible bottleneck is the SDIO interface used for communication with the NVM. The SDIO interface is one of the features of the controller and communicates with the micro SD card over a 4-bit bus. The SDIO interface utilizes the DMA controller to transfer data between the NVM and the controller without loading the CPU. To measure the transfer speed of the SDIO interface a single 512 byte sector is transferred on a CPU frequency of 72 MHz. The NVM is a 4 GB class 4 micro SD card. The 512 bytes represents a single block of data and the 72 MHz CPU frequency is used to reduce the power consumption of the controller. The resulting read speed is 706 kbps and the write speed is 284 kbps. The measured transfer speed differs between reading and writing, as was expected in accordance to Table 2.1. Various methods can be implemented to increase the transfer speed of the SDIO interface. Increasing the number of sequential sector transfers would increase the transfer speed because of the manner in which a NAND flash memory is build. In this memory, access times for random reads and writes are very long. Reading or writing a continuous block of data would reduce the impact of the long random access time. Increasing the transfer size from 512 bytes to 4096 bytes, increases the read speed to 1662 kbps and the write speed to 1042 kbps. This is an increase of 235 % for read speeds and 367 % for write speeds. Secondly, increasing the CPU frequency would lead to higher transfer speeds because the DMA controller uses the same clock as the CPU. The transfer speeds, in terms of CPU frequency and with a transfer size of 4096 bytes, are presented in Figure 4.4.

![Figure 4.4: Transfer speed for the SDIO interface with increasing CPU frequencies.](image)

The impact of the CPU frequency can be clearly seen in this figure. The minimum read and write speed are 631 kbps and 543 kbps, respectively on a CPU frequency of 24 MHz. The maximum read and write speed are 3518 kbps and 1782 kbps, respectively on a CPU frequency of 204 MHz.
Table 4.2: ATTO Disk Benchmark parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>File Size</td>
<td>2 MB</td>
</tr>
<tr>
<td>Transfer Size</td>
<td>0.5, 1, 2, .., 512kB</td>
</tr>
<tr>
<td>Overlapped I/O</td>
<td>10</td>
</tr>
<tr>
<td>Direct I/O</td>
<td>On</td>
</tr>
</tbody>
</table>

Bringing all interfaces together in the proof-of-concept WMS and measuring the end-to-end transfer speed is the next step. The measurements are done on the complete system and are gathered with the ATTO Disk Benchmark. This benchmarking tool is used to test hard drives, SSD drives, HBAs, RAID adapters and storage controllers. The parameters used in the benchmark are presented in Table 4.2. The benchmark results are presented in Figure 4.5.

![Graph showing transfer speed VS size (kB)](image)

Figure 4.5: Transfer speed of the WMS.

From this figure it can be concluded that the transfer speeds vary so little from each other that changing the transfer size does not impact the performance. This is because the transfer size in the WMS is fixed on 512 bytes. This will ultimately lead to a decrease in performance when compared to a system where the transfer size can be varied up. The resulting mean read speed is 30.27 kBps and the mean write speed is 24.82 kBps.
Chapter 5

Conclusions and Future Work

5.1 Conclusions

In today’s world content creation and content sharing have become very important. The question is: how to bring this concept to a larger audience? In modern smartphones this is not an issue as they contain the hardware and software to create and share content. However, these devices are typically expensive and a high-speed connection is required to stream audio and video. In addition, they need to be charged regularly. Another option would be to use USB flash drives as they often have high-speed capabilities, do not require recharging and are low cost. However, these devices lack the convenience of the smartphone and present another hurdle for easily content sharing.

The wireless memory presented in this thesis overcomes this gap. In this thesis the components required for a wireless memory (Chapter 2) and the design and implementation of a proof-of-concept system (Chapter 3) were presented.

The proof-of-concept system is composed of a wireless memory reader and a wireless memory tag and has the following functionalities:

- The WMR is able to access the contents of the NAND flash located on the WMT and forms an interface between the WMT and the user. To do so, the WMR will detect the WMT when it is in the vicinity and will wirelessly power the WMT by means of a magnetic field;

- The peak power transfer was measured at 2450 mW, which is well above the safe power requirement of 1322.7 mW;

- The efficiency at this power is 57% but the peak efficiency measured is 69% as found in Section 4.1.1;

- The end-to-end mean transfer speed is 30.27 kBps for reading from the WMT and 24.82 kBps for writing to the WMT.

This thesis has presented the requirements of wireless memory, the components that are needed to fulfill these requirements and the design and implementation of these components in a proof-of-concept system. The results of this
thesis have set the baseline for wireless memories and can potentially accelerate the development of a wireless memory.

5.2 Limitations and Future Work

Although this thesis presented an operational WMS, we have still a long way to go to develop a wireless memory suitable for the market. In this section the limitations of the current system and future work is discussed that can lead to a consumer wireless memory.

5.2.1 Wireless Power Transfer

The wireless power transfer is a key feature of a WMS. However, the importance of the wireless power transfer depends on the wireless memory application. In this thesis the PC WMR pad was demonstrated as a WMS. In this use case the design constraints like power consumption and size are not that strict. Looking at integration of a WMS in smartphones however, puts a lot of strain on power consumption and size. In this case the power consumption of the WMT must be extremely low to conserve battery power in the WMR (e.g. smartphone). Also the size constraint for the WMR is much larger when compared to the PC WMR pad. Therefore optimization of the wireless power transfer component is wanted to increase efficiency and decrease size. Methods like impedance matching \[13, 30\] and frequency tracking \[43\] can improve the wireless power transfer. Frequency tracking is especially interesting for systems with multiple WMTs. Here the introduction of the WMTs can detune the resonant frequency of the entire system, the frequency tracking method can keep the system on the same resonant frequency.

5.2.2 Wireless Technology

Obtaining practical transfer speeds should be a high-priority task in the development of wireless memories. Although Wi-Fi was the most practical wireless technology in the proof-of-concept system it is definitely not the best suited. The wireless technology should be short range, low power and have a high throughput to be of any practical use as a wireless memory, especially as a multimedia carrier. In \[10\] a wireless transmission is presented with a data rate of 6 Gbps for usage in non-contact memory cards. The wireless technology TransferJet shows promises for integration in a wireless memory. This technology is already available on the market and could be an intermediate step for wireless memories.

5.2.3 Security

In order to safely store and share memory content the WMS must guarantee a certain level of security. This security includes preserving the integrity, availability and confidentiality of the data held by the wireless memory. The level of security should be modified according to the use case which is applicable. Depending on the security level the system should be protected against common threats like: eavesdropping, man-in-the-middle attacks, radio jamming, radio overloading, skinning and denial-of-service attacks.
Bibliography


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Acronyms

**WMS**  Wireless Memory System

**WMT**  Wireless Memory Tag

**WMR**  Wireless Memory Reader

**NFC**  Near Field Communication

**RFID**  Radio Frequency IDentification

**MSC**  Mass Storage Class

**CDC**  Communication Device Class

**HID**  Human Interface Device

**DFU**  Device Firmware Upgrade

**UART**  Universal Asynchronous Receiver/Transmitter

**SSP**  Synchronous Serial Port

**SPI**  Serial Peripheral Interface

**I2C**  Inter-Integrated Circuit

**S2C**  Serial to Serial Converter

**USB**  Universal Serial Bus

**SDIO**  Secure Digital Input Output

**GPIO**  General-Purpose Input/Output

**ADC**  Analog Digital Converter

**ARM**  Acorn Risc Machine

**AC**  Alternating Current

**DC**  Direct Current

**RF**  Radio Frequency

**LF**  Low Frequency

**HF**  High Frequency
NVM  Non-Volatile Memory
PCRAM  Phase-Change Random-Access Memory
RRAM  Resistive Random-Access Memory
MRAM  Magnetoresistive Random-Access Memory
NAND  Negated AND
PSSS  Primary Series Secondary Series
PSSP  Primary Series Secondary Parallel
PPSS  Primary Parallel Secondary Series
PPSP  Primary Parallel Secondary Parallel
SD  Secure Digital
MMC  Multi Media Card
DVD  Digital Versatile Disc
ROM  Read Only Memory
GB  Giga Bytes
MB  Mega Bytes
kB  Kilo Bytes
BIOS  Basic Input/Output System
WPC  Wireless Power Consortium
CSP  Concentrated Solar Power
UWB  Ultra-WideBand
AP  Access Point
CCK  Complementary Code Keying
WEP  Wired Equivalent Privacy
WPA  Wi-Fi Protected Access
AES  Advanced Encryption Standard
TKIP  Temporal Key Integrity Protocol
UDP  User Datagram Protocol
TCP  Transmission Control Protocol
IP  Internet Protocol
DHCP  Dynamic Host Configuration Protocol
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
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<tbody>
<tr>
<td>ARP</td>
<td>Address Resolution Protocol</td>
</tr>
<tr>
<td>DNS</td>
<td>Domain Name System</td>
</tr>
<tr>
<td>PC</td>
<td>Personal Computer</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>LDO</td>
<td>Low-DropOut</td>
</tr>
<tr>
<td>RGB</td>
<td>Red Green Blue</td>
</tr>
<tr>
<td>LED</td>
<td>Light Emitting Diode</td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage Controlled Oscillator</td>
</tr>
<tr>
<td>RMS</td>
<td>Root Mean Square</td>
</tr>
<tr>
<td>EMC</td>
<td>ElectroMagnetic Compatibility</td>
</tr>
<tr>
<td>DoS</td>
<td>Denial-of-Service</td>
</tr>
<tr>
<td>IEEE</td>
<td>Institute of Electrical and Electronics Engineers</td>
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Appendices
Appendix A

Wireless Power Transfer Prototype

Figure A.1: Layout of the transmitter prototype.
Figure A.2: Schematic of the transmitter prototype.
Figure A.3: Layout of the receiver prototype.
Figure A.4: Schematic of the receiver prototype.
Appendix B

Wireless Memory Reader

Figure B.1: Layout of the wireless memory reader.
Figure B.2: Schematic of the wireless memory reader.
Appendix C

Wireless Memory Tag

Figure C.1: Layout of the wireless memory tag.
Figure C.2: Schematic of the wireless memory tag.