Reduction of UHF Power Transistor Distortion With a Nonuniform Collector Doping Profile

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Abstract—The linearity of a class-A, bipolar UHF power transistor is investigated. The device is intended for transmission of signals with multiple (TV) channels. Mixing between the various channels must be suppressed, which makes linearity an important parameter. This paper presents a novel approach, where process technology is specifically optimized to minimize distortion. It is shown that particularly the nonlinear collector–base capacitance strongly affects the linearity of this type of device. With a modified collector–base doping profile, the capacitance is manipulated. A nonuniform profile is introduced that significantly reduces third-order intermodulation. The profile consists of an arsenic doped spike that is grown epitaxially into the (otherwise) lightly doped collector. This reduces the bias dependence of $C_{BE}$ and improves the tradeoff between linearity and breakdown or ruggedness. The reduction in third-order intermodulation is demonstrated both experimentally and by mixed-level MDS/MAIDS simulations.

Index Terms—Bipolar transistor, collector–base capacitance, epitaxy, intermodulation distortion.

I. INTRODUCTION

INTERMODULATION distortion is a key parameter for many RF circuits. In particular, transmitters for signals containing multiple channels (e.g., TV signals) have tight constraints on intermodulation to suppress mixing between channels.

Despite the fact that distortion originates primarily inside the active devices of a circuit, solutions are most often sought in the domain of systems and circuit design. Here a different approach is presented where distortion is minimized by specifically optimizing process technology.

An important source of distortion comes from nonlinear feedback by the collector–base capacitance. This capacitance is primarily determined by the doping profile of the $n^-$ collector region. Unfortunately, optimization of this profile is restricted by requirements on breakdown voltage ($BV_{CEO}$). $BV_{CEO}$ of HF power devices is typically much higher than strictly necessary for normal operation because the device must be able to withstand some degree of abuse (ruggedness). The device must not be destroyed when it is loaded with a large impedance mismatch. Therefore, $BV_{CEO}$ is increased by using a (too) wide and lightly doped collector. This shifts the optimum bias point for minimum distortion [1] away from the nominal bias point. In fact, it is shifted completely out of the safe operating area (SOA) into the area in the $I_C-V_{CE}$ plane where the maximum power dissipation of 50 W is exceeded. Consequently, the point of maximum linearity cannot be used without exceeding the maximum power-dissipation limit.

Ruggedness will be represented by $BV_{CEO}$ under the assumption that these two parameters are strongly correlated. Although many other parameters can be associated with ruggedness (e.g., packaging, emitter-ballasting, transistor-layout), $BV_{CEO}$ is considered to be the most strongly related to the areas of process technology and device physics, which are most relevant for the concept discussed here.

In this paper, a nonuniform collector doping profile is introduced that improves the tradeoff. Linearity and ruggedness are decoupled to a certain degree, which makes ruggedness a less dominant factor. This allows the bias point with maximum linearity to be shifted back into the SOA. The concept is evaluated using the mixed-level simulator MAIDS (Microwave Active Integral Device Simulator) [2].

MAIDS is a device simulator incorporated within Hewlett-Packard’s Microwave Design System (MDS). This combination is capable of performing combined harmonic-balance and device simulations of complete RF circuits [3]. A bipolar device is specified in terms of doping profile and semiconductor material parameters rather than extracted compact model parameters. This explicit specification of the doping profile circumvents the limitation of compact models which must implicitly assume a certain shape in the doping profile (in most cases a uniformly or linearly graded profile). Hence, a tool like MAIDS is essential for evaluating devices with a more exotic, nonuniform collector doping profile as that presented here.

The simulated profile is then experimentally verified. For this purpose, special devices have been fabricated and measured. They are based on the (commercially available) Philips BLW-898 bipolar UHF linear power transistor, intended for linear amplification of signals in the 470 to 860 MHz frequency band. Experimental collector doping profiles were fabricated by using a newly developed epitaxy process that enables fabrication of sharp (50 nm wide) arsenic doped spikes [4], [5].
II. BACKGROUND

In bipolar transistors, two nonlinear components are of importance:

• the exponential dependence of collector–current and emitter–base (e–b) storage charge on e–b voltage; closely related to the transconductance ($g_m = dI_c/dV_{be}$);
• the nonlinear dependence of collector–base admittance on collector current and voltage; closely related to collector–base capacitance ($C_{cb}$).

In the following qualitative explanation, it will be clarified why these nonlinear elements are fundamentally different and why they should be considered separately.

All the higher order derivatives of $g_m$ are approximately proportional to $I_c$ due to the near exponential relationship between $I_c$ and $V_{ce}$. By increasing $I_c$, the forward gain can be increased. In this case, the overall gain already stabilizes at a low current density (where high current effects are still insignificant) due to low feedback from bondwires and emitter resistance. $P_3$ (power at third-order intermodulation frequencies), however, continues to decreases sharply with increasing $I_c$ (at a constant input power) because the forward gain is still increasing. This is equivalent to the case whereby amplifier distortion is decreased by increasing the loop gain.

However, when a dominating nonlinearity appears in the feedback ($\beta$), an increase in loop gain ($A_\beta$) will not decrease $P_3$ anymore ($\lim_{A_\beta \to \infty} P_{3,\text{out}}/P_{3,\text{in}} = 1/\beta$) [6]. So when $I_c$ is increased, distortion dominated by $g_m$ will decrease until it eventually drops below distortion caused by feedback nonlinearity that depends on the nonlinear coefficients of $\beta$ (primarily $C_{cb}$ for HF power BJTs [7]).

This is verified by examining $P_3$ and $P_{out}$ versus $I_c$, shown in Fig. 1. It has been measured by applying a two-tone input signal (at $f_1 = 850.5$ MHz and $f_2 = 800.5$ MHz; $P_{in} \approx 6$ dBm) to the device. $P_3$ is then measured at $f = (2f_2 - f_1)$ and $f = (2f_2 - f_1)$ (the magnitude of both components is equal).

Indeed, a sharp slope in $P_3$ is observed at low $I_c$, followed by an abrupt transition (also observed in [1], [7], [8]). The high-frequency (HF) class-A power transistor considered here is typically biased beyond this point (nominal bias in the figure). Here $g_m$-related distortion is negligible compared to that caused by $C_{cb}$.

It must be emphasized that these two regimes correspond to effects taking place in different regions of the device. Therefore, it is imperative to determine which regime is relevant prior to attempting technology optimization.

These considerations indicate that the collector region is most relevant. Hence, efforts to improve the linearity of this device must be directed toward $C_{cb}$ nonlinearity, which can be influenced by modifying the collector doping profile. However, this could also affect the breakdown-voltage ($BV_{ce0}$). Therefore, $BV_{ce0}$ must also be evaluated for a fair comparison.

III. THE COLLECTOR DOPING PROFILE

Traditionally, a collector doping profile consists of a highly doped sub-collector which is formed by the substrate or a buried layer, and a lightly, uniformly doped epi-layer placed between the sub-collector and the collector–base junction. This region is required to accommodate the electric field induced by the collector–base voltage ($V_{cb}$). In Fig. 2 the field distribution in such a collector is shown schematically for different $V_{ce}$ (the triangular area). To prevent breakdown, $E_{max}$ must be kept below a given threshold ($E_{crit}$, determined by material parameters). To achieve this, the collector is made wide and lightly doped when operation at high $V_{cb}$ is required. Conversely, for a low $V_{cb}$, a narrow and highly doped collector can be used, which is beneficial for the high-frequency performance.

The power transistor considered here has a very wide collector. Under normal operation, the space charge region does not extend all the way into the highly doped subcollector, but ends somewhere in the lightly doped collector region. As $V_{cb}$ increases, both $E_{\text{max}}$ (the maximum electric field) and the width of the space charge region increase. The net result is that $E_{\text{max}}$ increases approximately as the square root of $V_{cb}$.

Once the space-charge region touches the highly doped subcollector, the reach-through condition is reached. The depletion layer is now confined between the highly doped regions of the base and subcollector. As a result, $E_{\text{max}}$ increases nearly linearly with $V_{cb}$. This is shown in Fig. 2, where $V_{rt}$ indicates the onset of “reach-through.”

Beyond $V_{rt}$, $E_{\text{max}}$ in a narrow collector increases more rapidly with increasing $V_{cb}$ than in a wide collector that has not reached the “reach-through” condition yet. Therefore, a narrow
collector results in a lower \(BV_{CEO}\) and a poor ruggedness. For linearity, however, the “reach-through” condition is highly desirable because the fixed depletion-layer width reduces the bias dependence of the collector–base depletion capacitance.

Both collector design concepts can be found in commercially available transistors. For devices where ruggedness is most important, a wide collector is used, and for devices where linearity is more important, the “reach-through” concept is used. This paper introduces a profile that is actually a combination of the two, resulting in a better tradeoff between breakdown and linearity.

The profile consists of a sharp n-type spike that is introduced in the collector. It is designed so that with normal bias the collector–base depletion layer ends in the spike \((V_{CEO} = 25\, \text{V})\). This is shown in Fig. 3. The depletion boundary is pinned to the spike, thus reducing the variation in depletion width. This results in a lower \(C_{ch}\) variation. When a high collector–base voltage \((V_{CEO} = 50\, \text{V})\) is (inadvertently) applied, the spike is depleted, and the depletion layer extends into the low-doped region between the spike and the buried layer \((3 < x < 6\, \mu\text{m})\). The regained square root dependence of \(E_{max}\) on \(V_{cb}\) will now enhance buffering of the excess voltage.

In the ideal situation, a delta-doped spike is placed so that, under normal bias, the depletion layer boundary is pinned at this one position. When \(V_{CEO}\) is further increased, the spike is fully depleted. The limitation on the total doping in the spike is that it should be completely depleted well before breakdown. To meet this requirement, the increase in electric field, \(\Delta E\), resulting from depletion of the spike, must be kept below 0.20 MV/cm \((E_{crit})\). \(\Delta E\) will be used to represent the magnitude of the spike. It follows from Poisson’s equation that this value is proportional to the total charge in the spike.

In the experimental situation, the as-grown spike has a finite width of about 50 nm and maximum doping levels around \(10^{27}\) cm\(^{-3}\). Thus the spike width is 100 times smaller and the peak doping 100 times higher than that of the \(\approx 5\, \mu\text{m}-\)wide, lightly doped \((3 \times 10^{15}\, \text{cm}^{-3})\) collector region. This is a good approximation of a delta-doped spike. In the experimental situation, the distance from the spike to the silicon surface \((W_{top})\) is used to adjust the optimal bias point. The situation shown in Fig. 3 with \(\Delta E = 0.07\, \text{MV/cm}, W_{top} = 3\, \mu\text{m}\) and biasing at \(V_{CEO} = 25\, \text{V}\) results in a \(BV_{CEO}\) that is about 20% lower than that for a uniform profile of the same width and magnitude. Doubling the collector voltage to 50 V increases the maximum electric field by only 53%, which demonstrates the buffering mechanism. The pinning effect can be traded for buffering by varying the magnitude or position of the spike, resulting in more flexibility when making the tradeoff between breakdown/ruggedness and linearity.

IV. SIMULATIONS

In the following simulations, two devices with the basic doping profile shown in Fig. 3, have been compared:

- a reference device with no spike in the collector;
- a spike device where the spike itself is defined as a Gaussian profile with a width of 50 nm and \(\Delta E = 0.07\, \text{MV/cm}\).

Moreover, the accuracy of the simulations has been verified by comparison to measurements of the standard Philips BLW-898 transistor as reference device.

A. Device Simulations

The influence of the spike on the current–voltage dependence of \(C_{ch}\) has been investigated with device simulations carried out in MAIDS. The collector–base capacitance and \(cb\)-conductance (caused by avalanche) of the intrinsic device have been calculated for various collector voltages and currents. This analysis gives no quantitative information about the device linearity, but it is very suitable for determining (within a short simulation time) the optimum bias point and the bias regions where various physical effects dominate.

First contours of constant collector–base (feedback) conductance and susceptance \((\text{juω} \cdot C_{ch})\) have been simulated. In Figs. 4 and 5 they are plotted on the \(I_c-V_{CEO}\) plane. The feedback varies 0.5 mS between adjacent contours. In addition to the contours, two other lines are shown: the line enclosing the safe operating area \((L_c \cdot V_{CEO} \leq 50\, \text{W}, \text{the upper limit for power dissipation})\) and lines approximating the domain of a 35-dBm two-tone signal at the output (load line).

The region with the lowest density of contours has the lowest variation in feedback admittance and can therefore be assumed to have the highest linearity [1]. This region is indicated by the dotted circle in Figs. 4 and 5.

Important sources of nonlinearity can be identified from the figure. The depletion capacitance variations dominate when \(V_{CEO}\) is low (indicated by D.C.), the effects of quasi-saturation dominate at high \(L_c\) and low \(V_{CEO}\) (indicated by Q.S.), and avalanche multiplication effects dominate at high \(V_{CEO}\) (indicated by A.M.).

The position of the load-line in Fig. 4 confirms that the linearity is limited by the variation of depletion capacitance at low power levels, whereas quasi-saturation dominates at high power levels.

Fig. 4 shows the situation for the reference device. The most linear region is seen to lie outside the safe operating area (indicated by the dotted circle) and can therefore normally not be exploited.

The situation for the spike device is shown in Fig. 5. With respect to the reference device, the most linear region has be-
Fig. 4. Contour lines of constant feedback admittance (in mS at 860 MHz) and conductance (in mS) for the reference device. Also included are the boundary of maximum power dissipation ($P_{\text{max}} = 50 \text{ W}$) and an approximate load line that corresponds to 35-dBm output power. The dotted circle indicates the optimum bias region.

The observed improvement was not caused by the increase of $C_{gb}$. When $C_{gb}$ of the reference device was increased artificially by adding a lumped capacitor, no improvement (in terms of output power) was observed.

The measurements were performed with a setup of bias tees and tuners (Microlab FXR SF-11N), which is more flexible than the test circuit. The tuners were configured to match the output and input impedance to obtain a maximum output power and a minimum input reflection ($\leq -20 \text{ dB}$), respectively. The tuners provide a good impedance matching at the fundamental frequency, but at the higher harmonics it differs from the test circuit. This affects the intermodulation distortion at high power levels, but at low power levels ($\leq 25 \text{ dBm}$), a good agreement was found between the measurements and the (MAIDS or MEXTRAM) simulations of the test circuit with the reference device. Simulations where the test circuit was replaced by a dataset of S-parameter measurements of the tuners also shows good agreement with the measured values (not shown in Fig. 8). The measurements on the devices with a spike are discussed in more detail in the next section.

V. EXPERIMENTAL RESULTS

With a few minor adjustments in the process flow, the experimental BLW-898 transistor was fabricated on a series of wafers with an arsenic doped epilayer. The layers were grown in a commercially available, lamp-heated, single-wafer CVD reactor (the ASM Epsilon One). To obtain a sharp arsenic spike in the profile, a newly developed technique was applied. Hereby the in situ arsenic doping is accurately controlled during the growth process.
the entire epi-growth process [4], [5]. The growth conditions (gas pressures, deposition time, and temperature) are kept well within the specification of the CVD equipment and no exceptional accuracy is required of any parameter. Hence, these layers are grown with the same reproducibility as normally achieved with this reactor (in the order of a few percent).

The doping profiles of typical “as-grown” spikes, as determined by CV profiling through a thin top-layer, are shown in Fig. 9. The corresponding $\Delta E$ is also calculated from these measurements. It increases from 0.05 to 0.35 MV/cm as the doping in the spike is increased.

In the epi-layers used for the experimental transistor fabrication, two parameters were varied: the spike magnitude, resulting in $\Delta E$ values of: 0.04, 0.046, 0.077, and 0.10 MV/cm, and the top-layer thickness, resulting in $W_{\text{top}}$ values of 2, 2.5 and 3 $\mu$m. Uniformly doped epi-layers with a thickness of 2, 3, and 5.5 $\mu$m were also included for comparison.

The (on-wafer) measured $C_{\text{eb}}$ of devices with a $\Delta E$ of 0.077 MV/cm is shown in Fig. 10. The transition of the depletion boundary from the pinning to the buffering region can be identified from the figure.

For the available devices, the open-emitter breakdown voltage ($BV_{\text{CEO}}$ ) is shown in Table I. The table shows that the buffering is only effective in devices with a 2-$\mu$m top layer. This is the result of slight autodoping that is still present in the epi-layers. It has doped the top layer somewhat higher.
than anticipated. Despite considerable efforts to prevent this, the undesirable effect could not be completely eliminated. We speculate that further refinement of the epitaxy process can improve this.

Two-tone measurements were performed at 860 MHz (and 1-MHz tone spacing) with the setup of tuners and bias tees discussed in the previous section. Devices with 2 μm \( W_{\text{top}} \) are compared, as these show the most effective buffering. The results for the 0.046- and 0.077-MV/cm spike are shown in Fig. 11. With an intercept point (OIP3) in excess of 62 dBm (total output power), the experimental devices have a linearity comparable to the simulated values. The reference device has an OIP3 of 57 dBm, thus, an improvement of 5 dBm (10 dB in IM3) is achieved. However, due to the thinner top layer, this performance is obtained at a lower \( V_{\text{ce}} \) of 20 V. For the 2-μm uniformly doped collector, biased in a “reach-through” condition (the c-b depletion region extends from the base into the n+ substrate), an OIP3 of 60 dBm was found (also shown in Fig. 11). We attribute this lower value to the fact that this device could not be biased at \( V_{\text{ce}} \) above 15 V due to oscillations caused by operating the device too close to \( B V_{\text{CEO}} \).

The deviation of the measurements from the simulations at high power levels \( (P_{\text{in}} > 25 \text{ dBm}) \) is attributed to limitations of the measurement setup. For these measurements, a low ohmic bias network at the collector would be preferred over a bias tee to prevent modulation of the supply voltage [11].

### VI. CONCLUSION

A nonuniform collector doping profile is introduced for bipolar RF power transistors enabling a more flexible tradeoff between breakdown/ruggedness and linearity. It is demonstrated that a doping spike in an otherwise lightly doped collector profile can reduce the variation of the collector–base depletion capacitance at a specific bias point, and thus improve the linearity of the device. With mixed-level harmonic-balance circuit/device simulations using MDS and MAIDS, the effects on linearity have been evaluated. Simulations show that the intermodulation distortion of an UHF linear power transistor is decreased by 7 dB.

Measurements on experimental devices show that the novel collector–profile increases the linearity (IM3) by 10 dB,
reaching levels that are comparable to a “reach-through” collector, while its $BV_{CEO}$ is 35% higher.

With a stronger suppression of autodoping in the top layer, it will be possible to fabricate devices that can operate at the nominal bias point ($V_{ce} = 25$ V). Nevertheless, the present experiments clearly demonstrate the improvement that was aimed for.

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