# DELFT UNIVERSITY OF TECHNOLOGY

A Low-Power Area-Efficient SAR-Assisted Hybrid ADC for Ultrasound Imaging

Yixin Shi



Faculty of Electrical Engineering, Mathematics and Computer Science

Delft University of Techno



# A Low-Power Area-Efficient SAR-Assisted Hybrid ADC for Ultrasound Imaging

## THESIS

submitted in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

in

ELECTRICAL ENGINEERING

by

Yixin Shi Student number: 4466837

This work was performed in:

Electronic Instrumentation Laboratory Department of Microelectronics Faculty of Electrical Engineering, Mathematics and Computer Science Delft University of Technology

Copyright  $\bigodot$  2017 Electronic Instrumentation Laboratory All rights reserved.

# Delft University of Technology Department of Microelectronics

The undersigned hereby certify that they have read and recommend to the Faculty of Electrical Engineering, Mathematics and Computer Science for acceptance a thesis entitled "A Low-Power Area-Efficient SAR-Assisted Hybrid ADC for Ultrasound Imaging" by Yixin Shi in partial fulfillment of the requirements for the degree of Master of Science.

Dated: August 14, 2017

Chairman:

Dr. Michiel Pertijs

Committee Members:

Dr. André Bossche

Dr. Vasso Giagka

Ir. Zhao Chen

# Abstract

This thesis presents a Low-Power Area-Efficient SAR-Assisted Hybrid ADC for ultrasound imaging systems. This ADC combines a 5-bit SAR ADC per channel with a 4-bit single-slope ADC that produces the converter's LSBs and is implemented using shared hardware. The number of unit capacitors of the proposed ADC is about 1/16th of that of a 9-bit conventional SAR ADC, thus saving die area. The power consumption is reduced by sharing the delay line and ramp generator of the single-slope ADC among an ADC array. The simulated ENOB is 8.48bits, the power consumption is 419.3 $\mu$ W at a sampling rate of 33MS/s, the achieved FoM is 36fJ/conv-step. The estimated die area per channel is 150 $\mu$ m×107 $\mu$ m.

# Acknowledgments

I wish to express my sincere gratitude to my supervisor Dr.Michiel Pertijs, who provided me the opportunity to do my thesis project in his group. He guided me into the field of analog circuit design, helped me solve lots of problems and taught me the method to demonstrate and solve problems.

I want to thank my daily supervisor Ir.Zhao Chen. With his support and help, I learned how to use the circuit design tools to do different simulations. He also gave me a lot of suggestions to improve my design.

In addition, I want to thank my friends in Delft: Yang Qiao, Kangli Huang, Xianwei Zeng, Bo Jiang, Guanchu Wang, Dezhi Lin, Jiahan Lu, Jinyi Liu, Xuefei You, He Zhang, Chengyu Huang. They gave me lots of happiness and made my life in Netherlands more colorful.

Finally, I want to thank my beloved family, my parents. Their support, understanding and love gives me courage and confidence to overcome difficulties in my life.

Yixin Shi

August 14, 2017

# Contents

Al	bstra	$\mathbf{ct}$	$\mathbf{v}$
A	cknov	wledgments	vii
Li	st of	Figures	xi
Li	st of	Tables	xiii
1	Intr	oduction	1
	1.1	ADC application and challenges	1
	1.2	Previous research	1
	1.3	Motivation and objectives	2
	1.4	ADC requirements	3
	1.5	Organization of the Thesis	5
2	Ove	rview of SAR and digital slope ADC	7
	2.1	SAR ADC overview	7
		2.1.1 Switching scheme	8
		2.1.2 Redundant weighing method	16
	2.2	Digital slope ADC overview	18
		2.2.1 Conventional digital slope ADC	18
		2.2.2 Asynchronous digital slope ADC	19
	2.3	Method of combining SAR and Slope ADC	20
3	Syst	tem level design	23
	3.1	SAR ADC architecture	23
	3.2	Unit capacitor value in C-DAC	25
	3.3	Voltage level shift	26
	3.4	Digital slope conversion	27
	3.5	Time-domain interpolation	29
	3.6	Input signal range and resolution	31
4	Circ	cuit and layout design	33
	4.1	Dynamic comparator	33
		4.1.1 Kick back noise	34
		4.1.2 Dynamic comparator noise	35
	4.2	Asynchronous timing sequence implementation	37
	4.3	Level shift voltage value verification	38
	4.4	Time-continuous comparator	40
	4.5	Comparator delay compensation	42
	4.6	Sampling switch	43
	4.7	Encoder	44

	4.8	Delay line	45				
	4.9	Layout	47				
<b>5</b>	System level simulation results 4						
	5.1	Linearity	49				
	5.2	SNDR	51				
	5.3	Cross talk	53				
		5.3.1 Simulation with two frequency input	53				
		5.3.2 Simulation with pulse signals	54				
	5.4	Power consumption	55				
6	Con	clusion	57				
	6.1	Thesis contribution	57				
	6.2	Future work	57				
Re	efere	aces	<b>59</b>				

$1.1 \\ 1.2$	Block diagram of the TEE Imaging System with Hybrid Beamformer[4] Block diagram of proposed TEE imaging system[4]	$\frac{2}{3}$
$1.3 \\ 1.4$	State-of-the art $ADCs(a)[5]$	$\frac{4}{4}$
2.1 2.2	SAR ADC principle	8 8
2.3	3-bit differential Conventional SAR ADC	9
2.4	Waveform of conventional switching scheme	10
2.5	Conventional switching scheme conversion procedure <sup>[6]</sup>	11
2.6	3-bit differential monotonic switching scheme SAR ADC	12
2.7	Waveform of monotonic switching scheme	12
2.8	Monotonic switching scheme conversion procedure[6]	13
2.9	3-bit differential Vcm-based switching scheme SAR ADC	14
2.10	Waveform of Vcm-based switching scheme	14
2.11	$V_{cm}$ -based switching scheme conversion procedure[6]	15
2.12	Conventional binary search[7]	17
2.13	Redundant weighing search procedure[7]	17
2.14	Block diagram of conventional digital slope ADC	18
2.15	Time domain behaviour of conventional digital slope ADC[8]	18
2.16	Block diagram of asynchronous digital slope ADC	19
2.17	Time domain behaviour of asynchronous digital slope ADC[8]	19
2.18	Ramp generator	20
2.19	Hybrid SAR and single slope ADC[4]	20
2.20	Hybrid SAR and digital slope ADC[9]	21
2.21	SAR-Assisted single slope ADC[10]	22
3.1	Building block diagram of proposed ADC	23
3.2	Proposed SAR ADC architecture	24
3.3	Wave form of proposed switching scheme	24
3.4	Combine comparison results into binary code	25
3.5	Basic principle of digital slope ADC	26
3.6	Proposed digital slope ADC	27
3.7	Equivalent circuit of voltage level shift	28
3.8	Working principle of proposed ADC	28
3.9	Diagram of proposed hybrid ADC	29
3.10	Delay line and ramp DAC	30
3.11	Filtering function	30
4.1	Dynamic comparator	33
4.2	Time domain behaviour of Dynamic comparator	34
4.3	Kick back noise	35

4.4	C-DAC differential voltage	5
4.5	Dynamic comparator noise simulation test bench	3
4.6	Curve fitting of simulation results	3
4.7	Timing sequence implementation	7
4.8	Timing sequence diagram 37	7
4.9	SAR logic	3
4.10	Test bench to record residue voltage 39	)
4.11	Differential input voltage	)
4.12	Residue voltage simulation	)
4.13	Time-continuous comparator	)
4.14	Bode diagram of time-continuous comparator	1
4.15	Time-continuous comparator and switching logic	1
4.16	Comparator delay compensation	2
4.17	Sampling switch	3
4.18	Sampling switch with dummy switch compensation 43	3
4.19	Encoder	4
4.20	An example of the proposed Encoder	õ
4.21	Delay line	5
4.22	Delay line time variation	3
4.23	Layout floor plan	7
5.1	ADC array with 4 ADCs	9
5.2	INL simulation	)
5.3	INL	)
5.4	INL after calibration	1
5.5	Differential input signal of SNDR simulation	1
5.6	Ideal DAC output	2
5.7	Simulated ADC output spectrum	2
5.8	Cross talk simulation	3
5.9	Spectrum of cross talk simulation(a) 54	1
5.10	Spectrum of cross talk simulation(b)	1
5.11	Input signals of pulse signal simulation	5
5.12	Reconstructed output signals	5
5.13	Power consumption breakdown	3
6.1	Block diagram of the measurement set-up 58	3

1.1	Performance comparison with respect to similar $designs(a)$	5
2.1	Performance comparison with respect to similar $designs(b)$	22
3.1	Mismatch ratio of MIM capacitor	26
$5.1 \\ 5.2$	Power consumption of sub blocks	56 56
6.1	Performance comparison with prior works	57

# 1

This thesis describes the design of an analog to digital converter, which can be used in the readout circuit of ultrasound transducers. In this work, successive approximation register(SAR) and digital-slope concepts are combined to meet the stringent power and area requirements of the ultrasound application. The application of this work is described in this chapter, followed by the motivation and ADC requirements. At the end of this chapter, the organization of this thesis is given.

# 1.1 ADC application and challenges

Transesophageal echocardiography(TEE) is a cardiac imaging modality that uses the esophagus as the imaging window to the heart. In a TEE system, a TEE probe which consists of an ultrasound transducer array is inserted into the esophagus of the patient. The transducer array will transmit ultrasound waves to the heart and receive the echo signals. After signal processing, the heart image is available [1]. In order to get an accurate diagnosis, a TEE probe needs to be capable of providing real-time-3-D images. To realize such a TEE probe, there are several challenges. In order to provide high quality 3-D images, a 2-D matrix transducer array with thousands of independent elements needs to be integrated in the probe tip. In such situation, if the signal processing is done only by the image processor outside the patient body, the gastroscopic tube needs to accommodate thousands of cables. Apparently, it is not a feasible method [2]. In order to reduce the number of cables, in particular, integrating ultrasound transducers with readout circuits realized as an application-specific integrated circuit(ASIC) that does some signal processing, in particular, partial(sub-array) beamforming, locally is an efficient way. Moreover, it can also improve the signal immunity to the cable noise. However, it will bring the challenge to the ASIC design. Firstly, the circuit per element should fit within very small element pitch. Furthermore, to avoid overheat of human tissue, the power dissipation of the circuit is limited by self-heating.

# 1.2 Previous research

Figure 1.1 shows a hybrid beam-forming solution. The echo signals of different channels are firstly amplified by LNA (low-noise amplifier). Then, analog micro-beamforming is applied to align the signals from each subgroup in time and then add them constructively. After that, there is a gain compensation done by TGC. This compensation helps to maintain image uniformity and relaxes the dynamic-range requirements for the remaining circuits. Finally, the analog signal is converted into a digital signal to be further aligned by digital delay in the ultrasound machine [1]. In this system, the beam formation is split in two steps. The first step is analog delay of micro-beamformer

and the second one is the digital delay. The major drawback of this solution is that the control signals in analog beamformer have significant frequency components within the desired ultrasound pass-band, which will produce undesired noise on the image [3]. What's more, since the analog beamformer is based on capacitor, there is charge leakage, which will limit the delay range.



Figure 1.1: Block diagram of the TEE Imaging System with Hybrid Beamformer[4]

## **1.3** Motivation and objectives

Full digital beam formation could be a solution to improve the system. Figure 1.2 shows the block diagram of the full digital received beam formation 3D TEE imaging system. Compared with figure 1.1, the ADCs are element level ADCs, as a result, the digital signal will be available at an earlier stage, which will eliminate the drawbacks of an analog beamformer and provide more flexibility for the signal processing circuit. In addition, element level ADCs make RF data of the transducers available simultaneously without relying on multiplexing and reducing the functionality that has to be implemented in the periphery of the chip to a minimum. The latter feature helps to create very large transducer arrays, without being limited by the size and multiplexing speed of the ADCs placed outside of the core array. The element level ADC can also help reduce the cable count with the help of the digital multiplexing [15].



Figure 1.2: Block diagram of proposed TEE imaging system[4]

## **1.4** ADC requirements

In this ADC design, the area and power budget limited by the ultrasound application are the main challenge. The pitch size of the transducer is  $150\mu$ m. Consequently, the area of an element level ADC is limited by this pitch size. The area of an element level ADC should be less than the pitch size of the transducer:  $150\mu$ m×  $150\mu$ m. The power consumption of a TEE probe should be less than 1W. As there are on the order of 1024 transducers in TEE probe, the power budget of each element signal channel should be less than 1mW. Taking the power consumption of the other circuits in the signal receiving channel into consideration, the power budget for the ADC in each signal channel is  $600\mu$ W. The bandwidth of interest in receive mode is from 2.5MHz to 7.5MHz. According to the Nyquist criterion, the sampling frequency of the ADC needs to be higher than twice the signal frequency. The sampling frequency is set to 33MS/s, which is determined by the time resolution of the beamforming. The SNR of the output signal of the preceding LNA is around 50dB. According to the equation

$$ENOB = \frac{SINAD - 1.76}{6.02}$$
 (1.1)

where ENOB is the effective number of bits, SINAD is the signal-to-noise and distortion ratio, the ENOB of this ADC need to be larger than 8bits. According to these specifications, the figure of merit (FoM) of this ADC can be calculated by the equation

$$FoM = \frac{Power}{2^{ENOB} \cdot f_s} \tag{1.2}$$

where Power is the power consumption of the ADC, ENOB is effective number of bits,  $f_s$  is sampling frequency. The FoM of required ADC is around 70fJ/conversion-step.





Figure 1.3: State-of-the art ADCs(a)[5]



Figure 1.4: State-of-the art ADCs(b)[5]

frequency. From the comparison, the design chanenge is manny on power and area.				
	This work	[16]	[17]	[18]
Technology	$0.18 \mu m CMOS$	$0.13 \mu m CMOS$	$0.13 \mu m CMOS$	65nm CMOS
Resolution[Bit]	>8	12	14	12
Power[mW]	< 0.6	3.02	2.54	3.5
$Area[mm^2]$	< 0.0225	0.06	0.24	0.16
Fs[MS/s]	33	45	30	50
SNDR[dB]	>50	67.1	70.4	64.4
FoM[fJ/conversion-	<70	36.3	31.3	51.4

Figure 1.4 shows the FoM versus die area of state-of-the art ADCs. Table 1.1 shows a comparison of the desired specifications with respect to designs with similar sampling frequency. From the comparison, the design challenge is mainly on power and area.

Table 1.1: Performance comparison with respect to similar designs(a)

# **1.5** Organization of the Thesis

step

The thesis is organized as follows. Chapter 2 introduces the background of SAR ADCs and slope ADCs, including the working principle and main blocks. Chapter 3 describes the system level design, including the design choice of SAR ADC and slope ADC and the method of combining these two ADC. Chapter 4 explains the transistor level and layout design of the main building blocks of the system. Chapter 5 shows the system simulation results. Chapter 6 summarizes the contributions of the thesis. Suggestions for future work are also given.

The main challenge of this ADC design is the power consumption and area requirement. The SAR ADC is notable for its energy efficiency, as most of modern SAR ADCs present only dynamic power consumption from the use of CMOS logic and the absence of preamplifiers or static latch in the comparator. So, a SAR ADC is a good candidate ADC type. However, SAR ADCs tend to be not area efficient, because the C-DAC will cost large area. What's more, the area increases exponentially with ADC resolution. Single Slope ADCs are attractive for their simple implementation, and are widely used in imaging sensors. However, the counter in a single slope ADC needs a high speed clock, which makes it not power efficient. In addition, some building blocks in a single slope ADC have the potential to be shared by ADC array, which could be used to reduce both area and power consumption. Combining these 2 type ADCs together could be a good design solution to meet the power and area requirement. In this chapter, the background of SAR and slope ADCs are introduced followed by three related previous designs.

# 2.1 SAR ADC overview

The basic principle of successive approximation register (SAR) ADC is binary search algorithm. The approximation starts from MSB to LSB with the help of comparator. The following figure is an example of a 4-bit SAR ADC. Firstly, the voltage of the DAC is  $\frac{1}{2}V_{ref}$ . After the comparison of step 1, the B3 is set to 1. Then the DAC voltage increases by  $\frac{1}{4}V_{ref}$ , which is larger than the input signal during step 2. As a result, B2 is set to 0. B1 and B0 could be get in the same way. As shown in figure 2.1, the DAC voltage approaches to the input signal gradually.

Figure 2.2 shows the block diagram of SAR ADC. The main building blocks are clock controlled comparator, DAC, sample and hold circuit, and SAR logic.



Figure 2.1: SAR ADC principle



Figure 2.2: SAR ADC block diagram

The clock controlled comparator compares C-DAC voltage with the input signal. Then the comparison result will be sent to SAR logic, which controls the voltage change of C-DAC. The C-DAC could be used as the capacitor in sample and hold circuit.

### 2.1.1 Switching scheme

The voltage change on C-DAC is based on charge redistribution, which could be implemented by different switching schemes. The switching scheme is very important to a SAR ADC. Because it will affect power consumption and number of switches and voltage reference in a SAR ADC. In this section, three relevant switching schemes are introduced: conventional, monotonic,  $V_{cm}$ -based switching scheme.

#### 2.1.1.1 Conventional switching scheme

Figure 2.3 shows a 3-bit fully differential SAR ADC with conventional switching scheme. For simplicity, only the positive side of the ADC operation is described in below. During the sampling phase, the bottom plates voltage of the capacitors are charged to  $V_{ip}$ , and the top plates voltage are reset to the common-mode voltage  $V_{cm}$ . Next, the bottom plate of the largest capacitor is switched to  $V_{ref}$ , and that of the other capacitors are switched to ground. The comparator then performs the first comparison. If  $V_{ip}$  is higher than  $V_{in}$ , the most significant bit (MSB) B1 is 1. Otherwise, B1 is 0, and the bottom plate of the largest capacitor is reconnected to ground. Then, the bottom of the second largest capacitor 2C is switched to  $V_{ref}$ . The comparator does the comparison again. The ADC repeats this procedure until the least significant bit (LSB) is decided.



Figure 2.3: 3-bit differential Conventional SAR ADC

Figure 2.4 shows the waveform of the conventional switching scheme. The common mode voltage of two input signals remains at  $V_{cm}$  during the whole conversion.



Figure 2.4: Waveform of conventional switching scheme



Figure 2.5: Conventional switching scheme conversion procedure[6]

Figure 2.5 shows the energy consuming of each step. The average energy of B-bit switching algorithm, assuming all codes are equiprobable, may be derived as [6]

$$E = \sum_{i=1}^{B} 2^{B+1-2i} (2^{i}-1) CV ref^{2} = \left(\frac{2^{-B+1}+2^{B+2}}{3} - 2\right) CV ref^{2}$$
(2.1)

where B is the resolution of the ADC, C is the capacitance of a unite capacitor,  $V_{ref}$  is the reference voltage.

#### 2.1.1.2 Monotonic switching scheme

Figure 2.6 shows a 3-bit fully differential SAR ADC with monotonic switching scheme. During the sampling phase, the input signal is sampled on the top plates of the capacitive arrays, while the bottom plates are connected to the reference voltage. The MSB is directly obtained by the comparator. Depending on whether the MSB is 0 or 1, the MSB-capacitor of the bottom array or the top array is connected to ground, respectively. The ADC repeats the procedure until LSB is decided.



Figure 2.6: 3-bit differential monotonic switching scheme SAR ADC

Figure 2.7 shows the waveform of the monotonic switching scheme. During each bit cycling, the voltage on C-DAC just changes at one terminal. The common mode voltage will gradually decrease during the conversion.



Figure 2.7: Waveform of monotonic switching scheme

Figure 2.8 shows the energy consuming of each step. The average energy of B-bit switching algorithm, assuming all codes are equiprobable, may be derived as [6]

$$E = \sum_{i=1}^{B-1} (2^{B-2-i}) CVref^2 = (2^{B-2} - \frac{1}{2}) CVref^2$$
(2.2)

Where B is the resolution of the ADC, C is the capacitance of a unite capacitor,  $V_{ref}$  is the reference voltage.



Figure 2.8: Monotonic switching scheme conversion procedure[6]

#### 2.1.1.3 V<sub>cm</sub>-based switching scheme

Figure 2.9 shows a 3-bit fully differential SAR ADC with  $V_{cm}$ -based switching scheme. This switching scheme also employs top-plate sampling. In the first cycle, the inputs are connected to the top plates of the capacitor arrays and the bottom plates are connected to  $V_{cm}$ . The MSB is determined from a comparison immediately after the sampling. Depending on whether the comparison result is 0 or 1, the largest capacitor of the positive C-DAC array is discharged to ground or charged to  $V_{ref}$ , respectively. The opposite action is done in the negative C-DAC array. This procedure is adopted for all the remaining bits in the converter.



Figure 2.9: 3-bit differential Vcm-based switching scheme SAR ADC



Figure 2.10: Waveform of Vcm-based switching scheme

Figure 2.10 shows the waveform of the  $V_{cm}$ -based switching scheme. Like the conventional switching scheme, the common mode voltage of two input signals remains at  $V_{cm}$  during the whole conversion.

Figure 2.11 shows the energy consuming of each step. The average energy of B-bit

switching algorithm, assuming all codes are equiprobable, may be derived as [6]

$$E = \sum_{i=1}^{B-1} 2^{B-2-2i} (2^i - 1) CV ref^2 = \left(\frac{2^{-B} + 2^{B-2}}{3} - \frac{1}{2}\right) CV ref^2$$
(2.3)

Where B is the resolution of the ADC, C is the capacitance of a unite capacitor,  $V_{ref}$  is the reference voltage.



Figure 2.11:  $V_{cm}$ -based switching scheme conversion procedure[6]

#### 2.1.1.4 Summary

The advantage of the conventional switching scheme is that the input common mode voltage of the comparator will remain at  $V_{cm}$  during the conversion, so the common mode input is almost zero, which is good for comparator during the comparison. However, there is switch motion before the first comparison, thus causing more dynamic power consumption. In addition, there are lots of sampling switches at the bottom plate of the C-DAC capacitors, which will cost much area if using bootstrapped switches.

The advantage of the monotonic switching scheme is on area and power. Because of top plate sampling, the first comparison could be done directly after sampling. Consequently, the MSB capacitor value in C-DAC is half of its counterpart using conventional switching scheme. The number of switches and voltage reference are also less, which is easy to implement. Furthermore, there is just one switch motion in each bit cycling, thus saving power. The monotonic switching scheme consumes only 18.74% of the energy spent on the conventional switching scheme implementation when comparing 10-bit ADCs. The main disadvantage is that the input common mode voltage will gradually decrease from 0.5  $V_{ref}$  to Gnd, which may influence the comparator performance.

The advantage of  $V_{cm}$ -based switching scheme is that the input common mode voltage of the comparator will remain at  $V_{cm}$  during the conversion, which is good for comparator during comparison. Because of top plate sampling, its capacitance of C-DAC is same with that in monotonic switching scheme. In addition,  $V_{cm}$ -based switching scheme is also power efficient. It consumes only 12.48% of the energy spent on the conventional switching scheme implementation when comparing 10-bit ADCs. However, compared with monotonic switching scheme, it needs more voltage reference and switches.

## 2.1.2 Redundant weighing method

The SAR ADC which uses redundant weighing method adds extra redundant bit to tolerate a certain range of settling and decision error during bit-cycling. Therefore, it could alleviate the DAC and reference settling requirement. Figure 2.12(a) shows an example of binary search SAR ADC. This is a 4 bit case.  $V_i$  is input signal. For the first bit,  $V_i$  is smaller than the threshold voltage, so the MSB is 0. Then the quantization voltage level decreases by 4 LSBs. The ADC repeats this procedure until the least least significant bit (LSB) is decided. In this case, the digital output is 4. This is a correct conversion, the difference between the analog signal and the digital presentation is less than 1 LSB [7]. Figure 2.12(b) shows the same 4 bit case with wrong decision cycles. The wrong decision happens in the 2nd cycle, which results in mistakes in the remaining 2 cycles. In the end, the difference between the analog signal and the digital presentation is larger than 1 LSB.

Figure 2.13 shows concept of SAR ADC with redundant bit. This is also a 4 bit case, which uses 5 cycles to convert 4 bits. As a result, it will generate more decision levels than conventional one. The same input voltage could be represented by several digital codes. Hence, a certain range of error does not have influence on the conversion result. As shown in figure 2.13(b), although a decision error happens in the 2nd cycle, the conversion result is correct in the end.



Figure 2.12: Conventional binary search[7]



Figure 2.13: Redundant weighing search procedure<sup>[7]</sup>

# 2.2 Digital slope ADC overview

## 2.2.1 Conventional digital slope ADC

Figure 2.14 shows a diagram of a typical N-bit digital-slope ADC. The main building blocks are sample and hold circuit, counter, DAC and comparator. The input signal  $V_{in}$  is sampled on the  $V_a$  node. Then the N-bit counter starts working, which control the N-bit DAC to generate a digital ramp at node  $V_d$ . The comparator latches the counter as soon as the DAC output  $V_d$  exceeds the sampled voltage value, thus creating a digital output code proportional to the applied input voltage.



Figure 2.14: Block diagram of conventional digital slope ADC

Figure 2.15 shows the time-domain behaviour of digital-slope ADC. For this architecture, the sampling speed is severely limited due to the required high-speed over sampled clock fcnt, as the fcnt is  $2^n$  times of the sampling frequency, where n is the resolution of ADC [8]. Furthermore, the high speed clock is very power consuming. To solve such problem, asynchronous logic can be introduced.



Figure 2.15: Time domain behaviour of conventional digital slope ADC[8]

#### 2.2.2 Asynchronous digital slope ADC

Figure 2.16 shows the block diagram of asynchronous digital-slope ADC. Compared to the synchronous one, the N-DAC is controlled by delay line instead of N-bit counter, which eliminates the high speed counter clock from the system.



Figure 2.16: Block diagram of asynchronous digital slope ADC

The time domain behaviour is shown in figure 2.17. Firstly, the differential input signal is sampled on the capacitor array of the N-bit DAC. Then, the delay line is activated, the delay cell will switch one by one from 0 to 1, which controls the DAC to generate digital ramp. When the polarity of the comparator changes, the comparator will latch the delay line at its current position. The latched thermometer code, stored in the delay line, is proportional to the input voltage. Then with the help of thermometer code to binary code encoder, the digital output will be available.



Figure 2.17: Time domain behaviour of asynchronous digital slope ADC[8]

The main building blocks of such ADC are delay line and N-bit DAC, which could generate digital ramp signal. Figure 2.18 shows the delay line and N-bit DAC. The bottom node of the capacitors is controlled by delay line to connect to reference voltage or ground. Through each delay cell, The  $V_{rampp}$  will decrease by  $\frac{1}{2n}$  Vref. In contrast, The  $V_{rampn}$  will increase by  $\frac{1}{2n}$  Vref. Consequently, The step size of the differential ramp signal is  $\frac{1}{n}$  Vref.



Figure 2.18: Ramp generator

# 2.3 Method of combining SAR and Slope ADC

Figure 2.19 shows one way to combine a SAR and single slope [4].



Figure 2.19: Hybrid SAR and single slope ADC[4]

After the SAR conversion, the two switch S2 will close. The two current source
will charge the unit capacitor in the C-DAC. As a result, a voltage ramp is generated on C-DAC. When the comparator changes polarity, it will trigger the TDC (Time to digital converter). Then the conversion time will be converted into digital codes, which is shown as B6,B7,B8,B9.

The advantage of this architecture is that the current source and the delay line in TDC can be shared by several ADCs, which could reduce the power consumption and area of per ADC. The disadvantage is that the current source is not controlled by the delay line in TDC. The error will happen if the current source and the delay line do not start at the same time.

Another way to combine 2 ADCs is shown as figure 2.20.



Figure 2.20: Hybrid SAR and digital slope ADC[9]

The slope ADC in this one is digital slope ADC, which consists of a unary C-DAC. In this case, the C-DAC of SAR ADC and digital slope ADC are combined into one ADC array.

After the SAR conversion, the delay line starts to work, which will control the switch under the digital slope C-DAC to generate the digital ramp. The Delay line and the Encoder constitutes the TDC, which is also triggered by the comparator. The capacitors in SAR C-DAC are not binary, which is because the redundant weighing method is employed in this ADC.

The advantage of this architecture is that the digital ramp is controlled by the delay line in TDC, which makes these 2 time windows match with each other. Another advantage is the use of redundant weighing method, which could cover certain bit cycling error during SAR conversion. The main disadvantage of this ADC is on the area ,since the it uses additional C-DAC to generate the digital ramp.

Figure 2.21 shows an additional way. This ADC is a 12-bit ADC used in imaging

sensor. The SAR ADC does the first 6 bits coarse conversion. The single slope ADC does the 6 bits fine conversion. Similar to the ADC in figure 2.19, the ramp signal is connected to the bottom plate of the unit capacitor in C-DAC. While the ramp signal is digital ramp signal generated by a resistor string. To obtain the lower 6 bits, the counter counts the number of ramp steps when the comparator output becomes high.

The advantage of this ADC is that, the ramp generator can be shared by several ADCs. There is only one comparator used in both SAR and single phase, which can save area. The disadvantage is that the counter needs to be drove by a high speed clock, which is power consuming.



Figure 2.21: SAR-Assisted single slope ADC[10]

Table 2.1 shows the	performance of	prior	designs and	d the	target	specs	of t	his '	work.
			()		()				

	This work	[4]	[9]	[10]
Technology	$0.18 \mu m CMOS$	$0.18 \mu m CMOS$	28nm CMOS	90nm CMOS
Architecture	SAR-assisted	SAR-assisted	SAR-assisted	SAR-assisted
	Digital slope	single slope	Digital slope	single slope
Resolution[Bit]	>8	9	12	12
Power[mW]	< 0.6	0.8	0.35	0.056
$Area[mm^2]$	< 0.0225	0.015	0.0047	0.0023
Fs[MS/s]	33	33	100	0.37
SNDR[dB]	>50	55.7	64.43	62
FoM[fJ/conversion-	<70	48.7	2.2	36.9
step]				

Table 2.1: Performance comparison with respect to similar designs(b)

The low power consumption of [10] is because of the low sampling frequency, the small area is due to the single-ended input structure. The small area and low power consumption of [9] is related to its advanced 28nm technology. In this design, the technology is  $0.18\mu$ m, the sampling frequency is 33MS/s and the structure is differential input mode, which is challenging to meet the area and power targets.

In proposed hybrid ADC, SAR and digital slope ADC are combined to finish 9-bit conversion. The SAR ADC is chosen to do the 5 bits coarse conversion. The 4 bits fine conversion is finished by digital slope ADC. This split is based on conversion time and area consideration.



Figure 3.1: Building block diagram of proposed ADC

Figure 3.1 shows the system block diagram. The C-DAC of SAR ADC is also used as sampling capacitor. After the coarse SAR conversion, the residue voltage will remain on the C-DAC. Then the digital slope conversion starts. The Ramp DAC controlled by delay line will generate digital ramp voltage on the C-DAC, which will make the voltage of two C-DAC cross each other. With the help of comparator, the delay line and encoder will convert the conversion time into digital code. There are two comparators in the system, one is dynamic comparator used in SAR conversion, the other is time-continuous comparator used in digital slope conversion. In order to reduce power consumption and area, the ramp DAC and the delay line are shared by ADC array.

### 3.1 SAR ADC architecture

Figure 3.2 shows the architecture of proposed SAR ADC part with redundant weighted C-DAC. The switching scheme is monotonic switching scheme with top plate sampling. As a result, the C-DAC area could be half of that of conventional SAR ADC. However,

because of top plate sampling, the parasitic capacitance of the comparator will influence the C-DAC settling during conversion, which may cause gain error. In order to solve such problem, the value of reference voltage needs to be adjusted.



Figure 3.2: Proposed SAR ADC architecture



Figure 3.3: Wave form of proposed switching scheme

The redundant weighing method is used in the SAR conversion, which uses 6 cycles to convert 5 bits. The ratio of the capacitors in C-DAC is shown in figure 3.2. As a result, the voltage change on C-DAC of each cycle is  $\frac{12}{33}V_{ref}$ ,  $\frac{8}{33}V_{ref}$ ,  $\frac{5}{33}V_{ref}$ ,  $\frac{3}{33}V_{ref}$ ,  $\frac{2}{33}V_{ref}$ ,  $\frac{1}{33}V_{ref}$ . The wave form of SAR procedure is shown in figure 3.3.

There are 6 comparison results of 6 comparison cycles, which will be combined into 5 bits digital output. The ratio of C1 to C6 is C1:C2:C3:C4:C5:C6= $2^3+2^2:2^3:2^2:2^0:2^1:2^0:2^1:2^0$ . So, the comparison results B1 to B6 could be combined into 5-bit digital output D0-D4 in the way shown in figure 3.4. After the SAR conversion, the differential residue voltage of two C-DAC is within  $\left[-\frac{1}{33}, \frac{1}{33}\right]V_{ref}$ .

					B4	
		B6	B6	<b>B</b> 3	B3	
Digital	+	B5	B4	B2	B1	
Output	D4	D3	D2	D1	D0	

Figure 3.4: Combine comparison results into binary code

# 3.2 Unit capacitor value in C-DAC

The main consideration of the unit capacitor value is thermal noise and the mismatch of the capacitor. The thermal noise power during the sampling phase is

$$V n_{samp}^{2} = 2 \frac{kT}{C} \tag{3.1}$$

Where k is Boltzmann constant, T is the temperature, C is the total capacitance of one branch of the differential C-DAC.To get a quantization noise dominated design, the quantization noise needs to be larger than the thermal noise. The quantization noise power is

$$Vq^2 = \frac{V_{LSB}^2}{12}$$
(3.2)

Where  $V_{LSB}$  is the LSB voltage. Then C needs to be larger than 163.6fF, which is the lower limit of the C-DAC value. Mismatch of the unit capacitor can be described as

$$C = C_0 + \Delta C \tag{3.3}$$

where  $C_0$  is the nominal value of the capacitor,  $\Delta C$  obeys the normal distribution with zero mean. The relation between capacitor mismatch and maximum DNL is [11]:

$$DNL_{max} = \frac{\sqrt{2^N - 2\Delta C}}{2C} (LSB) \tag{3.4}$$

Where N is the resolution of the ADC,  $\Delta C$  is the mismatch value, C is the unit capacitance. Let  $3DNL_{max} < 0.5$ LSB. Then the maximum mismatch ratio of a unit capacitor can be derived:  $\frac{\Delta C}{C} < 0.38\%$ . The capacitor used in the system is MIM capacitor, the mismatch ratio can be obtained from Monte carlo simulation. Table 3.1 shows the result of Monte carlo simulation. The minimum size of unit capacitor which meets the mismatch requirement is  $5 \times 5 \ \mu m^2$ .

Area $(\mu m^2)$	Value(fF)	Mismatch	Mismatch ratio(%)
		value(aF)	
4×4	35.29	159.5	0.448
$5 \times 5$	54.27	194.6	0.359
6×6	76.85	229.6	0.297
7×7	103.3	264.6	0.256
8×8	133.7	299.7	0.224

Table 3.1: Mismatch ratio of MIM capacitor

# 3.3 Voltage level shift



Figure 3.5: Basic principle of of digital slope ADC

Figure 3.5 shows the basic principle of digital-slope ADC. After the SAR conversion, there will be residue voltage on the C-DAC. Then, the ramp generator will generate step ramp. The voltage on P-side C-DAC will decrease, while the voltage on N-side ramp will increase, which will make the voltage of two C-DAC cross each other. This time period T2 will be converted into digital code by time to digital converter (TDC). T1 is the total time period of digital-slope conversion.

However, after SAR conversion, the  $V_{ip}$  may be smaller than  $V_{in}$ . In such situation, if the voltage on p-side C-DAC decreases and the voltage on n-side C-DAC increases, these two voltages will not cross each other, which means the digital-slope ADC will

lose its function. In order to solve such problem, there is a voltage level shift after the SAR conversion. The voltage level shift will increase the voltage on p-C-DAC before the digital slope conversion starts, which makes sure that  $V_{ip}$  is always larger than  $V_{in}$ .

After the SAR conversion, the differential residue voltage will be within  $\left[-\frac{1}{33}, \frac{1}{33}\right] V_{ref}$ . While the level shift voltage value is  $\frac{4}{97}V_{ref}$ , which will be explained in next section. As a result, after voltage level shift, the differential residue voltage will be within  $\left[-\frac{1}{33}, \frac{1}{33} + \frac{4}{97}\right] V_{ref}$ . This voltage level shift value is a bit larger than the maximum absolute value of differential voltage. This is because there may be some settling error and decision error during the SAR conversion, which will make the differential residue voltage exceed  $\left[-\frac{1}{33}, \frac{1}{33}\right] V_{ref}$ . So, this voltage level shift value is designed for redundancy, although it will result in losing some resolution during digital-slope conversion.

### 3.4 Digital slope conversion

Figure 3.6 shows the circuit after SAR conversion. The bottom plates of capacitors in C-DAC of SAR ADC are connected to the low impedance node. The dynamic comparator and SAR logic are disabled after SAR conversion, which is not shown in this figure. The two switches S1 are connected to ground during the SAR conversion to make the bottom plate of C7 connect to low impendence node. After SAR conversion, S1 will switch off to make the ramp DAC floating.



Figure 3.6: Proposed digital slope ADC



Figure 3.7: Equivalent circuit of voltage level shift

The level shift is finished by the P-ramp DAC. After S1 switching off, the C01-C08 in P-ramp DAC will switch from ground to  $V_{ref}$ . To calculate the level shift voltage value, the circuit could be simplified as figure 3.7. C is the unit capacitance, 4C is the total capacitance of the P-ramp DAC, 2C is the capacitance of C7, 31C is the total capacitance of C1-C6 in P terminal C-DAC. These 3 capacitors can be considered as a voltage divider. C01-C08 in P-ramp DAC switching from ground to Vref means the voltage change  $\Delta V1$  is  $V_{ref}$ . Then, the voltage change  $\Delta V2$  can be calculated:  $\frac{4}{97}V_{ref}$ .



Figure 3.8: Working principle of proposed ADC

After voltage level shift, the differential residue voltage will be within  $\left[-\frac{1}{33}+\frac{4}{97},\frac{1}{33}+\frac{4}{97}\right]V_{ref}$ . Then, the delay line will be triggered, which will control C01-C08 in P-ramp DAC switch from  $V_{ref}$  to ground one by one, C01-C08 in N-ramp DAC switch from ground to  $V_{ref}$ . In this way, the 8 step digital ramp will be generated on the C-DAC. When the voltage on the N terminal C-DAC exceeds the voltage on the P terminal C-DAC, the TDC will convert the conversion time into digital code with the help of comparator. Figure 3.8 shows the working principle of proposed hybrid ADC. The red line and the green line shows the differential signal in the SAR conversion and the digital slope conversion. Figure 3.9 shows the diagram of the proposed hybrid ADC. Different from the circuit in figure 3.6, the ramp DAC and delay line are shared by N ADC subgroups, which could save area and power consumption. In order to keep the level shift voltage and ramp step voltage same with the case in figure 3.6, the capacitance ratio between ramp DAC and SAR ADC C-DAC should remain the same. As a result, the unary capacitance in ramp DAC should increase to N times, which is  $\frac{N}{4}C7$ .



Figure 3.9: Diagram of proposed hybrid ADC

#### 3.5 Time-domain interpolation

Figure 3.10 shows the relation between delay line and ramp DAC. The delay line is reset at sampling phase of the ADC. After the SAR conversion, the start signal will change from 0 to 1. Then the delay line controls the buffer to charge or discharge the ramp DAC. The D-flip flops are used to sample the delay line. Then the encoder will convert the 15-bit thermometer code into binary code. The capacitors in ramp DAC are triggered every 2 delay cells. There are 8 unary capacitors in each branch of ramp DAC, as a result, the step ramp signal is a 3-bit step ramp signal. While the D-flip



Figure 3.10: Delay line and ramp DAC

flops sample every delay cell, the 4 bit binary code is obtained from the encoder. Such time domain interpolation increases the resolution of digital slope ADC from 3 bits to 4 bits, with no extra capacitors in ramp DAC [9].

The time-domain interpolation is based on a low bandwidth comparator. As shown in figure 3.11, the high frequency step signal will be filtered by the comparator. After filtered, the signal will be more proportional to time.



Figure 3.11: Filtering function

### 3.6 Input signal range and resolution

After the SAR conversion, the differential residue voltage on C-DAC needs to be within  $\left[-\frac{1}{33}, \frac{1}{33}\right]V_{ref}$ , which means the differential input voltage need to be within  $\left[-\frac{32}{33}, \frac{32}{33}\right]V_{ref}$ . Since  $V_{ref}$  is 200mV, the differential input range is  $\left[-194, 194\right]$ mV, which still meets the input voltage range of design target.

After level shift the residue voltage is within within  $\left[-\frac{1}{33}+\frac{4}{97},\frac{1}{33}+\frac{4}{97}\right]V_{ref}$ , while the full scale of digital-slope ADC is  $\frac{8}{97}V_{ref}$ .

The resolution can be calculated:  $\log_2(2^5 \times 2^4 \times \frac{6}{99} \div \frac{8}{97}) = 8.56$  bits. The resolution is a bit smaller than 9 bits because of redundancy design. However,

The resolution is a bit smaller than 9 bits because of redundancy design. However, it is still high enough to meet the SNR requirement of the design target.

The main building blocks of the proposed hybrid ADC have been introduced in chapter 3. Their circuit implementation is discussed in this chapter.

# 4.1 Dynamic comparator

In order to reduce power consumption, the comparator in SAR conversion is a dynamic comparator. Figure 4.1 shows the dynamic comparator used in SAR conversion. The comparator consists of 2 stages. The first stage is voltage amplification stage, which will pre-amplify the input voltage. The second stage is a latch. M8, M10 and M9, M11 are two inverters connected in positive feedback, which are used to get rail-to-rail digital output outp and outn [19]. The output will be further buffered by the inverters.



Figure 4.1: Dynamic comparator

Figure 4.2 shows the time domain behaviour. The comparator is reset when CLK signal is low. During the reset phase, FN and FP nodes are pre-charged to VDD. outn and outp nodes are discharged to ground. When CLK signal becomes high, the comparison phase starts. As M4, M5 will switch off, FN and FP nodes will be

discharged. The discharging speed depends on the input voltage. When the commonmode voltage approximates the threshold voltage of M6 and M7, the second stage starts to work. The common mode output voltage will increase, while the differential output voltage will also increase. Finally, the rail-to-rail output will be obtained with the help of the positive feedback mechanism.

The power consumption of the dynamic comparator is speed limited, since the comparator needs to finish six comparisons within around 9ns. For this speed consideration, the average current during the working period of first stage and second stage is  $19.4\mu$ A and  $23.3\mu$ A. The supply voltage VDD is 1.8V.



Figure 4.2: Time domain behaviour of Dynamic comparator

#### 4.1.1 Kick back noise

Kick back noise is a common problem in dynamic comparators. The voltage change in nodes FN and FP is rail to rail, which will be coupled to the input nodes through the parasitic capacitance of the input transistor pair M1 and M2. Figure 4.3 is a simulation waveform, which shows the kickback noise. The blue wave is the C-DAC P terminal output, the red wave is the C-DAC N terminal output. There is some small voltage fluctuation during the bit cycling, which is kickback noise. However, in this structure, such kickback noise just influences common mode voltage. Figure 4.4 shows the differential voltage of two C-DAC nodes. The kickback noise has little influence on differential voltage.



Figure 4.3: Kick back noise



Figure 4.4: C-DAC differential voltage

#### 4.1.2 Dynamic comparator noise

The noise analysis of dynamic comparator is different from a common amplifier circuit, because it is not a linear circuit. The input-referred noise can be simulated in the time domain with transient noise simulation. Then the output results should be further processed to get the input referred noise. Figure 4.5 shows the test bench of the input referred noise simulation. V1 is the input common mode voltage, V2 is the input voltage added to the positive input terminal of the comparator. The Accumulator is

Verilog-A component. The 'total' node is used to count the total comparison number. The 'one' node is used to record times when the outp is high and the 'ratio' node will show the proportion of the times when outp is high.



Figure 4.5: Dynamic comparator noise simulation test bench

V2 is swept from -1.6 mV to 1.6 mV with 0.16 mV step size. For each input voltage value, the comparator will do 1000 times comparison. The Accumulator will output total, one and ratio signal for each signal value. The ratio should obey a normal distribution. So, after the simulation, function-fitting can be used to get the noise value. The function is [12]:



 $\Phi(x) = \frac{1}{2} [1 + erf(\frac{x}{\sqrt{2}})]$ (4.1)

Figure 4.6: Curve fitting of simulation results

Figure 4.6 shows the curve fitting result. The sigma is 0.455mV, which could be considered as the input referred noise of the dynamic comparator. The LSB voltage of

SAR conversion is 12.5mV. So, the input referred noise of the dynamic comprartor is much smaller than the LSB voltage.

# 4.2 Asynchronous timing sequence implementation



Figure 4.7: Timing sequence implementation



Figure 4.8: Timing sequence diagram

Figure 4.7 shows the asynchronous timing sequence implementation of the SAR conversion. CLK is the clock signal which is used as the sampling signal. The period of CLK signal is 30ns, which stays on high voltage level only at the beginning 2ns. As a result, the sampling duration is 2ns in every 30ns. The core of this asynchronous timing sequence is the dynamic comparator, which is enabled when Latch control signal is 1, disabled when latch control is 0. When the comparator is disabled, both the two outputs are 0. At reset phase, the Reset signal is reset, which disables the comparator. When SAR conversion starts, the Reset signal will become 1. Then, the latch control signal is only controlled by the "Latch\_finish\_delay" signal during the SAR conversion. Figure 4.8 shows the timing sequence diagram. The SAR conversion finishes at around 12ns, then digital slope conversion starts [13].

Figure 4.9 shows the SAR logic. The comparator outputs are directly used as the trigger clock. After each bit cycling, the corresponding D flip flops will be disabled. Consequently, only one D flip flop is triggered in each bit cycling, which could reduce the power consumption. CP9-CP4 are the output codes of the SAR conversion.



Figure 4.9: SAR logic

### 4.3 Level shift voltage value verification

As shown in chapter 3, the level shift value is designed to tolerate a certain range of settling error or decision error during SAR conversion. To verify whether this redundancy is effective or not, a simulation of the residue voltage is introduced in this section. Figure 4.10 shows the test bench used to record the residue voltage on the C-DAC after the SAR conversion. The voltage recorder is Verilog-A component, which records the differential residue voltage after every SAR conversion.



Figure 4.10: Test bench to record residue voltage



Figure 4.11: Differential input voltage



Figure 4.12: Residue voltage simulation

The differential input signal in this simulation is a linear ramp signal which covers the full scale range, which is shown in figure 4.11. The differential residue voltage is shown in figure 4.12. The maximum residue voltage is 6.906mV, the minimum residue voltage is -6.876mV. For this design, in ideal case, the residue voltage should be within [-6.06,6.06]mV. The residue voltage in simulation exceeds this range, which is because of the noise of the comparator. The level shift voltage value is 8.25mV. So this error could still be tolerated.

To take the mismatch of the capacitors in C-DAC into consideration, further analysis is needed. The unit capacitor in C-DAC is a  $5\mu m \times 5\mu m$  MIM capacitor, whose native mismatch is 0.359%. As a result, the maximum voltage settling error ratio on C-DAC caused by capacitor mismatch is  $\frac{1+0.359\%}{1-0.359\%}$ -1=0.7%, If such error happens in each bit-cycling, the maximum voltage error is 1.32mV. Although the maximum error will happen in each bit-cycling, this value could still be used as an upper limit value. Combining this value with the simulation result, After the SAR conversion, the residue voltage will be within[-8.20,8.23]mV, which still can be covered by the level shift voltage value. So, 8.25mV is a reasonable level shift voltage value.

#### 4.4 Time-continuous comparator



Figure 4.13: Time-continuous comparator

Figure 4.13 shows the time-continuous comparator used in the digital-slope conversion. This comparator consists of two stages. The bandwidth of the first stage needs to

be low, given the need of time domain interpolation. However, it cannot be too low, because it will cause a long propagation delay. The last delay cell is triggered at around 25ns in one conversion. To make sure the ADC can finish the conversion within 30ns, the propagation delay of the comparator can not exceed 3ns. As a result, the bandwidth of the first stage is designed at 90MHz, which is much smaller than the 700MHz step ramp signal and could meet the propagation delay requirement. The input common mode voltage of the first stage is around 600mV, so PMOS input transistors are used. The transistors under the input pair are cascode transistor, which reduce the voltage change at the drain nodes of the input pair. In this way, the voltage change coupled to the input node is reduced. The bandwidth of the second stage needs to be high to have a high response speed. The output is connected to an inverter to buffer the output signal to digital level. The tail current of first stage and second stage is  $100\mu A$  and  $40\mu$ A, respectively. The supply voltage is 1.8V. Figure 4.14 shows the bode diagram of time-continuous comparator. The DC gain is 62dB, bandwidth is 90MHz. The inputreferred rms noise of time-continuous comparator, simulated using small signal noise simulation, is 0.27mV. The LSB voltage of the digital slope conversion is 1.03mV. So, the input referred noise voltage is much smaller than LSB voltage.



Figure 4.14: Bode diagram of time-continuous comparator



Figure 4.15: Time-continuous comparator and switching logic

In order to reduce power consumption, power-down switches and the associated switch logic are applied to the time-continuous comparator. Transistors M7, M9, M10,

M15, M17, M18 are switch transistors in the circuit. SAR finish signal maintains 1 during the SAR conversion, which makes EN signal low. As a result, the tail current transistors M7, M15 switch off during the SAR conversion. M9, M10 discharge the drain nodes of M1, M2 to ground. M17, M18 pre-charge the drain nodes of M11, M12 to the supply voltage. As a result, the valid signal is 0. When the SAR conversion finishes, the SAR finish signal will change from 1 to 0, which makes EN change polarity. Then, the comparator is enabled. After the valid signal become 1, through a certain delay, the comparator will be disabled again.

### 4.5 Comparator delay compensation



Figure 4.16: Comparator delay compensation

The propagation of the time continuous comparator will result in a constant systematic offset in TDC. To eliminate this offset, the delay compensation is needed. Figure 4.16 shows the principle of the comparator delay compensation. Because of the delay time of the time continuous comparator, it will give a response after the crossing point, which will cause more delay cells be sampled by TDC. In order to solve this problem, three more delay cells are added to the delay line, based on the simulated delay time. Then, the TDC starts sampling the delay line from the third delay cell to compensate the comparator delay [9].

#### 4.6 Sampling switch

The peak to peak input voltage is around 400mV. The input mode is differential, which means the voltage swing on each input terminal is  $\pm 100$ mV. As the digital supply voltage is 1.5V, which can provide enough over drive voltage, it is preferable to use a single NMOS or PMOS transistor as sampling switch. The common mode voltage of the input is designed at 700mV. The sampling switch is NMOS transistor, which is shown in Figure 4.17.



Figure 4.17: Sampling switch



Figure 4.18: Sampling switch with dummy switch compensation

The main consideration of the sampling switch design is speed and accuracy. In conducting state, the output of the sampling switch needs to reach the input voltage within a certain time. To meet the speed requirement, a sufficiently high W/L device is usually used to reduce the on-resistance.

The sampling accuracy is influenced by charge injection and clock feed through. When the transistor switches off, the charge in its channel will be released through the source and drain node. This is called charge injection, which will cause a voltage change at the output node. In addition, the CLK signal which is used to control the switch will be coupled to output through parasitic capacitance. This is called clock feed through, which also causes a voltage change at output node. A dummy switch can be used to compensate these two effects, which is shown in figure 4.18. M2 is the dummy switch. The control signal of M1 and M2 are antiphase. M2 has two functions. One is to absorb the charge released by M1, the other is to compensate the clock feedthrough of M1 [14].

### 4.7 Encoder

The function of the encoder is to convert a thermometer into a straight binary code. In this application, the 15 inputs are counted from 0 to 15, which is converted into 0000 to 1111. In order to save area, the input signals are counted as a 2D matrix[4]. Figure 4.19 shows the circuit implementation of the encoder. The signals from inco1 to inco15 are 15 input signals, the Q1, Q2, Q3, Q4 are 4 bits output binary code.



Figure 4.19: Encoder

To illustrate the working principle of this encoder, figure 4.20 shows an example.

There are 10 ones in input signal, which means signal inco4 and inco8 are ones, inco12 is zero. As a result, the output MSB Q3,Q4 is 10. For the first non-full row, there are ones. So, the LSB Q1,Q2 is 10. As a result, the binary output code is 1010.

IN	x1	x2	<b>x</b> 3	x4	Y <sub>out</sub>	MSB	
1x	1	1	1	1	1		
2x	1	1	1	1	1	10	
Зx	1	1	0	0	0		
4x	0	0	0	Output			
X <sub>out</sub>	1	1	0				
LSB		10			1010	0	

Figure 4.20: An example of the proposed Encoder

# 4.8 Delay line



Figure 4.21: Delay line

As shown in figure 4.21, there are 17 cells in the delay line, each dealy cell consists of an AND gate and three delay units. The delay time of each delay cell is around 0.67ns. The

delay variation of the delay cell can be obtained from Monte carlo simulation. Figure 4.22 shows the simulation result. The average delay time is 0.673ns, the standard deviation is 34.18ps. The delay standard deviation is much smaller than the delay time of the delay cell, so it has little influence on the digital slope conversion.



Figure 4.22: Delay line time variation

# 4.9 Layout



Figure 4.23: Layout floor plan

Figure 4.23 shows the layout floor plan of the ADC array with 4 ADCs. The shared components are the TDC and the ramp generator, which are at the center of the layout floor plan. In order to save area, the ramp-DAC is on the top of the TDC. The capacitors in the ramp-DAC are MIM capacitors, which consist of metal5 and metal6 layer. In order to reduce cross talk between the TDC and the ramp generator, metal4 is used as a shield layer. Similarly, the SAR-DAC is also on the top of the circuit of each ADC. The length of the ADC array is  $300\mu$ m, the width is  $215\mu$ m. As a result, the area of each ADC is  $150\mu$ m×107 $\mu$ m, which is smaller than the design target.

As mentioned in previous chapters, the delay line and ramp generator can be shared by several ADCs. The simulated performance of an ADC array including 4 ADCs is shown in this chapter. Figure 5.1 shows the ADC array with 4 ADCs. The linearity, SNDR, power consumption and cross talk between different ADCs are discussed.



Figure 5.1: ADC array with 4 ADCs

## 5.1 Linearity

To simulate the INL(integral non-linearity) of the ADC, the differential input signal is a voltage ramp covering the full input range of the ADC from -194mV to 194mV. The ADC output is digital code. In order to analyse the ADC output in analog domain, a DAC is needed. In this work, this DAC is an ideal DAC implemented by Verilog-A. As shown in figure 5.2. The red line is the differential input signal, the blue line is the output of the ideal DAC. To obtain INL, the input voltage should be subtracted from the output of the ideal DAC, after which the result is divided by the LSB voltage of the ADC. The result is shown in figure 5.3, from -1.04LSB to 1.06LSB.



Figure 5.2: INL simulation



Figure 5.3: INL

There is a fixed gain error in the INL simulation. After the gain error calibration, the INL can be calibrated within[-1,1]LSB. Figure 5.4 shows the INL result after calibration.



Figure 5.4: INL after calibration

# 5.2 SNDR

To simulate the SNDR of the ADC, the differential input signal is a 5.11MHz sinusoidal signal with full scale input range of the ADC from 194mV to 194mV, which is shown in figure 5.5. Figure 5.6 shows the output of the ideal DAC.



Figure 5.5: Differential input signal of SNDR simulation



Figure 5.6: Ideal DAC output

After calculating the FFT, the output spectrum is obtained, which is shown in figure 5.7. The power density of harmonic and folded components are indicated in the figure. The SINAD (Signal-to-noise and distortion ratio) is 52.8dB. The effective number of bits (ENOB) is calculated by

$$ENOB = \frac{SINAD - 1.76}{6.02}$$
 (5.1)

which is 8.48 bits. So, the SNDR and ENOB meet the requirement of the ADC design target.



Figure 5.7: Simulated ADC output spectrum

#### 5.3 Cross talk

The delay line and ramp generator is shared by 4 ADCs. So, cross talk may happen among the 4 ADCs. To simulate the cross talk, the differential input of one ADC is a 5MHz sinusoidal signal with full scale input range of the ADC from 194mV to 194mV. The differential input signals of the other three ADCs are zero. Figure 5.8 shows the output of the ideal DAC of each ADC. The red line is the output of the ADC, whose input is sinusoidal signal, the other three lines are the output of the other ADC with zero input. As shown in figure 5.7, the output of the ADCs with zero signal input is not affected by cross talk.

In real situation, the cross talk may cased by the shared nodes of the ADC array. During the SAR conversion, the voltage of shared nodes are pulled down by switches. During the SAR bit cycling, different ADCs may cause different voltage fluctuations on the shared nodes. This is the main mechanism of the cross talk. The simulations above are based on the schematic simulation, some parasitic effects are ignored during the simulation. The more accurate simulation can be obtained from the post layout simulation.



Figure 5.8: Cross talk simulation

#### 5.3.1 Simulation with two frequency input

In real situation, the input signals of the ADC array may be at different frequencies. To further simulate the cross talk, in this part, the input signals are two sinusoidal signals at different frequencies. One is 5.11MHz, the other is 4.13MHz. Figure 5.9 and figure 5.10 show the FFT results of 2 ADCs, of which the input signal frequency is 4.13MHz and 5.11MHz respectively. The spectrum power density of the cross talk frequency is much smaller than that of the input signal frequency.



Figure 5.9: Spectrum of cross talk simulation(a)



Figure 5.10: Spectrum of cross talk simulation(b)

#### 5.3.2 Simulation with pulse signals

As discussed in chapter 1, this ADC will be used in the signal receiving channel of a TEE imaging system. During the working situation, different ADCs will receive the signal with different delay time. In this section, the input signals of 4 ADCs are pulse signals with different delay time as shown in figure 5.11. Figure 5.12 shows the output reconstructed by means of ideal DAC.



Figure 5.11: Input signals of pulse signal simulation



Figure 5.12: Reconstructed output signals

#### 5.4 Power consumption

In this design, the digital supply voltage is 1.5V, the analog supply voltage is 1.8V. Table 5.1 shows the power consumption of different sub blocks per ADC. The calculation is based on the average current during one conversion cycle. The power consumption of SAR and timing logic is the highest  $157.7\mu$ W, followed by that of the time-continuous comparator, which is  $121.5\mu$ W. The power consumption of dynamic comparator is less than time-continuous comparator, which is  $55.3\mu$ W. The delay line and ramp generator are shared by 4 ADCs, so their power consumption is relatively small per ADC. Figure 5.13 shows the power consumption breakdown.

The total power consumption of per ADC is  $419.3\mu$ W. As a result, the figure of merit(FoM) can be calculated, which is 36 fJ/conversion-step. Table 5.2 shows the

comparison between the design target and the simulated results.

TC-CMP	DY-CMP	SAR+Timing	Ramp	Delay	TDC	C-DAC	Total
		logic	generator	line			
$121.5\mu W$	$55.3\mu W$	$157.7 \mu W$	$12\mu W$	$20.05 \mu W$	$45.7\mu W$	$7\mu W$	$419.3\mu W$



Table 5.1: Power consumption of sub blocks

Figure 5.13: Power consumption breakdown

	Technology	ENOB	Sampling	Power	FoM
			frequency	consumption	
Design Target	$0.18 \mu m CMOS$	> 8 bits	33 MS/s	<0.6mW	<70fJ/conv-
					step
Simulation	$0.18 \mu m CMOS$	8.48bits	33 MS/s	$0.42 \mathrm{mW}$	$36 \mathrm{fJ/conv-step}$
Results					

Table 5.2: Performance comparison with design targets
## 6

## 6.1 Thesis contribution

A Low-Power Area-Efficient SAR-Assisted Hybrid ADC for ultrasound imaging system has been presented in this thesis. The number of unit capacitors of the proposed ADC is about 1/16th of that of a 9-bit SAR ADC. To further reduce the area and power consumption, the delay line and ramp generator are shared among the ADC array. The transistor level simulation results prove that the resolution, power and speed targets are met. Table 6.1 shows the performance comparison with prior works with similar circuit structure. Compared with [4], which used the  $0.18\mu$ m technology, the die area of this work is same with [4]. The power consumption of this work is about half of that of [4] with similar SNDR. The power consumption of [10], is much smaller than this work, which is because of the low sampling frequency. The FoM of [10] and that of this work are similar. Due to the advanced 28nm technology, the area and power consumption of [9] are both smaller than this work.

	This work	[4]	[9]	[10]
Technology	$0.18 \mu m CMOS$	$0.18 \mu m CMOS$	28nm CMOS	90nm CMOS
Architecture	SAR-assisted	SAR-assisted	SAR-assisted	SAR-assisted
	Digital slope	single slope	Digital slope	single slope
Resolution[Bit]	9	9	12	12
Power[mW]	0.42	0.8	0.35	0.056
$\operatorname{Area}[mm^2]$	0.015	0.015	0.0047	0.0023
Fs[MS/s]	33	33	100	0.37
SNDR[dB]	52.8	55.7	64.43	62
FoM[fJ/conversion-	36	48.7	2.2	36.9
step]				

Table 6.1: Performance comparison with prior works

## 6.2 Future work

The three main parts of the future work are improvement of the design, finishing the layout and measurement.

So far, the encoder in the TDC is not shared by the ADC array. However, it has the potential to be shared, which can further reduce the die area and the power consumption. The power consumption of the time-continuous comparator is the second highest among the sub blocks. The relation between the time-continuous comparator and the performance of the time-domain interpolation can be further analyzed to optimize the

power consumption of the time-continuous comparator. In addition, the layout area of the time-continuous has the potential to be reduced.

The layout of the SAR C-DAC and ramp C-DAC needs to be done in the future. For good matching, the routing should be symmetrical and dummy capacitors should be used.

To test the chip, the analog input, all the supply and reference voltages and a clock should be provided. The digital outputs need to be post processed. To realize these functions, a carrier PCB should be designed, which helps the ASIC connect to the test instruments. The input signals can be provided by a function generator. The input clock and digital outputs can be managed by an FPGA. These instruments can be controlled by computer via Matlab. Figure 6.1 shows a block diagram of the proposed measurement set-up.



Figure 6.1: Block diagram of the measurement set-up

- Yu, Z., Blaak, S., Chang, Z. Y., Yao, J., Bosch, J. G., Prins, C., ... Meijer, G. C. (2012). Front-end receiver electronics for a matrix transducer for 3-D transesophageal echocardiography. IEEE transactions on ultrasonics, ferroelectrics, and frequency control, 59(7).
- [2] Chen, C., Raghunathan, S. B., Yu, Z., Shabanimotlagh, M., Chen, Z., Chang, Z. Y., ... Vos, H. J. (2016). A prototype PZT matrix transducer with low-power integrated receive ASIC for 3-D transesophageal echocardiography. IEEE transactions on ultrasonics, ferroelectrics, and frequency control, 63(1), 47-59.
- [3] Savord, B., Solomon, R.(2003, October). Fully sampled matrix transducer for real time 3D ultrasonic imaging. In Ultrasonics, 2003 IEEE Symposium on (Vol. 1, pp. 945-953). IEEE.
- [4] W. Hu, "A 9-bit 33MHz Hybrid SAR Single-slope ADC," Delft University of Technology, 2015.
- [5] B. Murmann, "ADC Performance Survey 1997-2016," [Online]. Available: http://web.stanford.edu/ murmann/adcsurvey.html.
- [6] T. Rabuske, J. Fernandes, "Charge-Sharing SAR ADCs for low-Voltage Low-Power Applications", Springer Switzerland, 2017.
- [7] Liu, C. C., Kuo, C. H., Lin, Y. Z. (2015). A 10 bit 320 MS/s low-cost SAR ADC for IEEE 802.11 ac applications in 20 nm CMOS. IEEE Journal of Solid-State Circuits, 50(11), 2645-2654.
- [8] Harpe, P. J., Zhou, C., Philips, K., de Groot, H. (2011). A 0.8-mW 5-bit 250-MS/s time-interleaved asynchronous digital slope ADC. IEEE Journal of Solid-State Circuits, 46(11), 2450-2457.
- [9] Liu, C. C., Huang, M. C., Tu, Y. H. (2016). A 12 bit 100 MS/s SAR-Assisted Digital-Slope ADC. IEEE Journal of Solid-State Circuits, 51(12), 2941-2950.
- [10] Kim, M. K., Hong, S. K., Kwon, O. K. (2016). An area-efficient and low-power 12-b SAR/single-slope ADC without calibration method for CMOS image sensors. IEEE Transactions on Electron Devices, 63(9), 3599-3604.
- [11] Z. Wang, "A Low-power SAR ADC for implantable electronic medical device," University of Electronic Science and Technology of China, 2015.
- [12] Nuzzo, P., De Bernardinis, F., Terreni, P., Van der Plas, G. (2008). Noise analysis of regenerative comparators for reconfigurable ADC architectures. IEEE Transactions on Circuits and Systems I: Regular Papers, 55(6), 1441-1454.

- [13] Raheleh Hedayati, "A Study of Successive ApproximationRegisters and Implementation of an Ultra Low Power 10-bit SAR ADC in 65nm CMOS Technology," Linkping University, 2011.
- [14] Behzad Razavi, "Design of Analog CMOS Integrated Circuits", The McGraw-Hill Companies, 2001.
- [15] Michele D'Urbino, "An Element-level Sigma-Delta ADC for Ultrasound Imaging," Delft University of Technology, 2017.
- [16] Liu, W., Huang, P., Chiu, Y. (2010, February). A 12b 22.5/45MS/s 3.0mW 0.059mm<sup>2</sup> CMOS SAR ADC achieving over 90dB SFDR. In Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International (pp. 380-381). IEEE.
- [17] Lee, H. Y., Lee, B., Moon, U. K. (2012, February). A 31.3fJ/conversion-step 70.4dB SNDR 30MS/s 1.2V two-step pipelined ADC in 0.13µm CMOS. In Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International (pp. 474-476). IEEE.
- [18] Lee, C. C., Flynn, M. P. (2010, June). A 12b 50MS/s 3.5mW SAR assisted 2-stage pipeline ADC. In VLSI Circuits (VLSIC), 2010 IEEE Symposium on (pp. 239-240). IEEE.
- [19] Van Elzakker, M., van Tuijl, E., Geraedts, P., Schinkel, D., Klumperink, E. A., Nauta, B. (2010). A 10-bit Charge-Redistribution ADC Consuming  $1.9\mu$ W at 1MS/s. IEEE Journal of Solid-State Circuits, 45(5), 1007-1015.