Design of an Energy-Efficient Interface Circuit for a MEMS-based Capacitive Pressure Sensor

Lokesh Rajendran

Master of Science Thesis

TU Delft Delft University of Technology

Faculty of EEMCS

Design of an Energy-Efficient Interface Circuit for a MEMS-based Capacitive Pressure Sensor

Master of Science Thesis

For the degree of Master of Science in Electrical Engineering at Delft University of Technology

Lokesh Rajendran

September 27, 2013

Faculty of Electrical Engineering Mathematics and Computer Science (EEMCS) · Delft University of Technology

The work in this thesis was supported by NXP Semiconductors, Eindhoven. Their cooperation is hereby gratefully acknowledged.

Delft University of Technology
Department of
Electrical Engineering Mathematics and Computer Science (eemcs)

The undersigned hereby certify that they have read and recommend to the Faculty of Electrical Engineering Mathematics and Computer Science (EEMCS) for acceptance a thesis entitled

Design of an Energy-Efficient Interface Circuit for a MEMS-based Capacitive Pressure Sensor

by

Lokesh Rajendran

in partial fulfillment of the requirements for the degree of

Master of Science Electrical Engineering

Dated: September 27, 2013

Supervisor(s):

Dr.ir.Michiel Pertijs

Reader(s):

Prof.Dr.Kofi Makinwa

Dr.Leo de Vreede

Dr. Wim Besling

Mr. Mat Simons

Abstract

This thesis presents an incremental $\Delta\Sigma$ capacitance-to-digital converter (CDC) that serves as an interface circuit for a MEMS-based pressure sensor. The thesis presents a systematic analysis of the CDC and compares different CDC architectures. A novel non-linear CDC is also proposed and analysed. Energy-efficiency of the CDC is improved by implementation of various design techniques like double sampling, system-level chopping and a novel inverter-based OTA. The CDC has been designed in such a way that it can operate with either an on-chip or external pressure sensor. The CDC can be tuned to compensate for a wide range of baseline capacitance. The CDC operates over a pressure range of 0-1.3bar and achieves a pressure resolution of 10^{-5} bar (equivalent to a resolution of 16 bits).

The CDC is implemented in NXP 0.16μm 1P6M technology. The circuit design and layout of the CDC are presented. The CDC consumes 2.33μA from a 1.2V supply resulting in an energy consumption of only 2.01nJ, a significant improvement over the state-of-the-art.

Keywords: pressure-sensor interface, energy-efficiency, double sampling, incremental $\Delta\Sigma$ ADC, inverter-based OTA.

Table of Contents

Acknowledgements

I start by thanking my thesis advisor Dr. Michiel Pertijs who gave me the opportunity to work under him and helped me learn analog design. He was very patient with me throughout the entire course and gave me enough amount of freedom during my work. He was the best advisor one could ask for. In particular, he helped me develop an intuitive feel for the analytical equations.

I thank Prof. Kofi Makinwa and Prof. Marcel Pelgrom for their excellent classes on Electronic instrumentation and Nyquist data converters respectively.

I thank NXP Semiconductors, Eindhoven for funding this project. I gratefully acknowledge their monthly financial support. In particular, I wish to thank Frank Thus and Mat Simons of NXP for their administrative and technical help during the project. I wish to thank Wim Besling of NXP for the various extensive technical discussions we had on the pressure sensor and the circuit design. The discussion found in this thesis on the topic of pressure sensor characteristics and its physical construction was based on Wim's data. I formally thank NXP for allowing me to use their computer facility (for simulations).

I thank all the committee members for accepting my invitation for the defence and for their time in review of this thesis.

I thank Zhichao Tan for helping me throughout the design phase, even during the busy schedule of his thesis defence. This work reached its final stage due to his crucial help. I thank all the past and present members of our research group for their nice companionship and exchange of technical ideas. In particular, I wish to thank Ugur, Ruimin, Chao and Zili for the technical discussion. I sincerely thank Zu-Yao, Joyce and Karen for their administrative help.

I thank all the MSc students of my batch for their companionship. In particular, I wish to thank Yuxin, Siva, Sangan and many others who helped me in having fun and life outside the lab. And I wish to thank all the people who helped me during my time at Delft.

I wish to thank my parents, my sisters and their families for their love, affection and their huge amount of financial support for my studies.

Finally, I thank the Almighty God who has blessed me abundantly. His presence was with me throughout the ups and downs. I pray to you Lord and submit this work at your feet.

Guide me for the rest of my life as you have done in the past.

Delft University of Technology
September 27, 2013

Lokesh Rajendran

"The horse is made ready for the day of battle, but victory rests with the Lord."
— *Proverbs 21:31, New International Version*

Chapter 1

Introduction

The instrumentation applications of capacitive-based pressure sensors are numerous in the field of various scientific applications and day to day life. Some of these application areas are: biomedical applications like monitoring of inter-ocular eye pressure and inter-cranial pressure, measurement of altitude (Altimeter), and scientific applications where precise pressure monitoring is required.

In this research work, we will address the implementation of the interface circuitry that is required to obtain a digital output from a pressure sensor. There are various standard commercial products that are available for interfacing with a pressure sensor. In this work, our main focus is to design an energy-efficient interface circuit for the sensor. This is achieved by various design techniques that are discussed in detail throughout the thesis.

In the following sections of this chapter we will introduce the physical structure and characteristics of the pressure sensor used in this work, followed by specifications and the organization of the thesis.

1-1 Pressure Sensor Characteristics

The general principle of an capacitance sensor can be explained by the following formula (strictly speaking, a parallel plate capacitor). The capacitance, C (in Farads) is given by:

$$C = \frac{\epsilon \times A}{d} \tag{1-1}$$

where ϵ is the permittivity of the dielectric, A is the area of the plates and d is the distance between the plates. As we can see from Eq. (1-1), we have three parameters that influence the value of the capacitance. The physical quantity that has to be sensed influences one of these parameters and we get a change in the capacitance which is then measured by the interface circuit. In the case of a typical pressure sensor, the parameter d is varied and we get a corresponding change in the capacitance. Clearly as it could be seen from Eq. (1-1),

the relation between d and Capacitance, C is not a linear one. Thus the pressure versus capacitance characteristic will also be a non-linear curve, which will present constraints during the measurement of the capacitance. This is because the sensitivity of the pressure versus capacitance curve varies widely over the measurement range and it depends on the pressure that is to be measured. In fact, the pressure versus capacitance curve of the sensor (used in this project) is roughly a fourth order function.

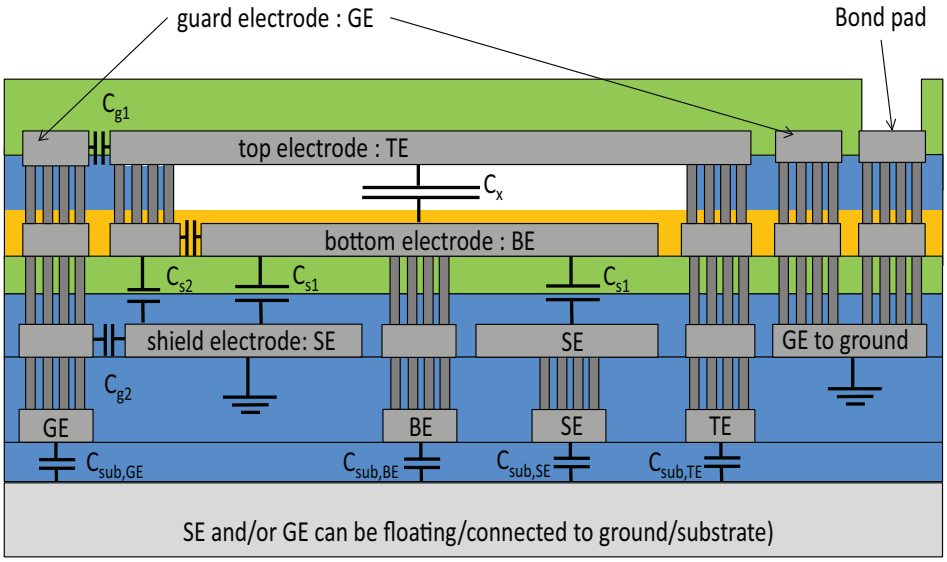


Figure 1-1: Physical construction of the sensor [1]

Now let's us have a look at the physical construction of the MEMS-based capacitive pressure sensor, given in Figure 1-1. This sensor was internally developed by NXP Semiconductors, Eindhoven. The sensor is square shaped and measures 400μm $\times$ 400μm. It is fabricated over the wafer (upon the passivation layer) in a special post processing step after the CMOS fabrication of the die. The top and bottom plates are made of Aluminium. The top plate is a flexible electrode and the bottom plate is a fixed electrode. The pressure acts on the top plate and causes a deflection of the plate which causes a change in the capacitance. The distance between the two plates is an air gap (no oxide exists between them). The shield electrode is implemented during the layout phase of the chip in METAL 5 and is connected to ground. The shield layer helps in preventing any interference from the circuit (present below the shield electrode) from reaching the sensor (present above the shield electrode). The top plate of the sensor will be the driving side (which ensures the electrical interference from external world will not affect the potential on the plate) and bottom plate will be the sensing side. The electrical equivalent of the sensor is shown in Figure 1-2. The C_x is the actual value of the sensor capacitance that has to be measured and C_{p1}, C_{p2} are the parasitic capacitances, whose value can be as high as $4 \times C_x$.

The measured pressure versus capacitance curve for the pressure sensor is given in Figure 1-3. The left side of the curve indicates the region in which the slope of the characteristic $(\frac{dC}{dP})$ is low. In other words, the sensitivity is low and a high resolution from the interface circuit is required to sense the change in pressure. The right side of the curve indicates the region in which $(\frac{dC}{dP})$ is high. In other words,the sensitivity is high and a lower resolution from the interface circuit is sufficient to sense the change in pressure. Table 1-1 gives the specification

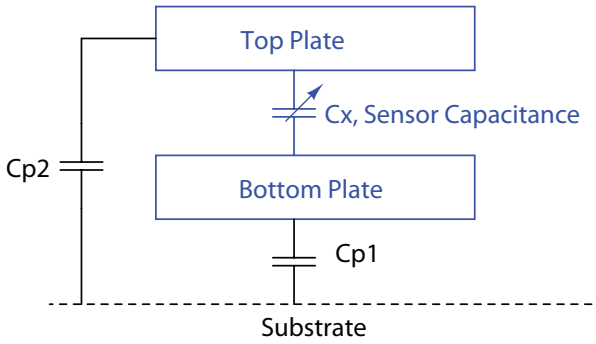


Figure 1-2: Electrical equivalent circuit of the sensor

Parameter	Value
Baseline Capacitance (0bar)	0.95 pF
Capacitance range (0.5 - 1.3bar)	0.45 pF
Sensor Cap variation (Variation in slope - 1σ)	$\pm$ 5%
Sensor Cap variation (Variation in baseline capacitance - 1σ)	$\pm$ 2.5%

Table 1-1: Specifications of the sensor

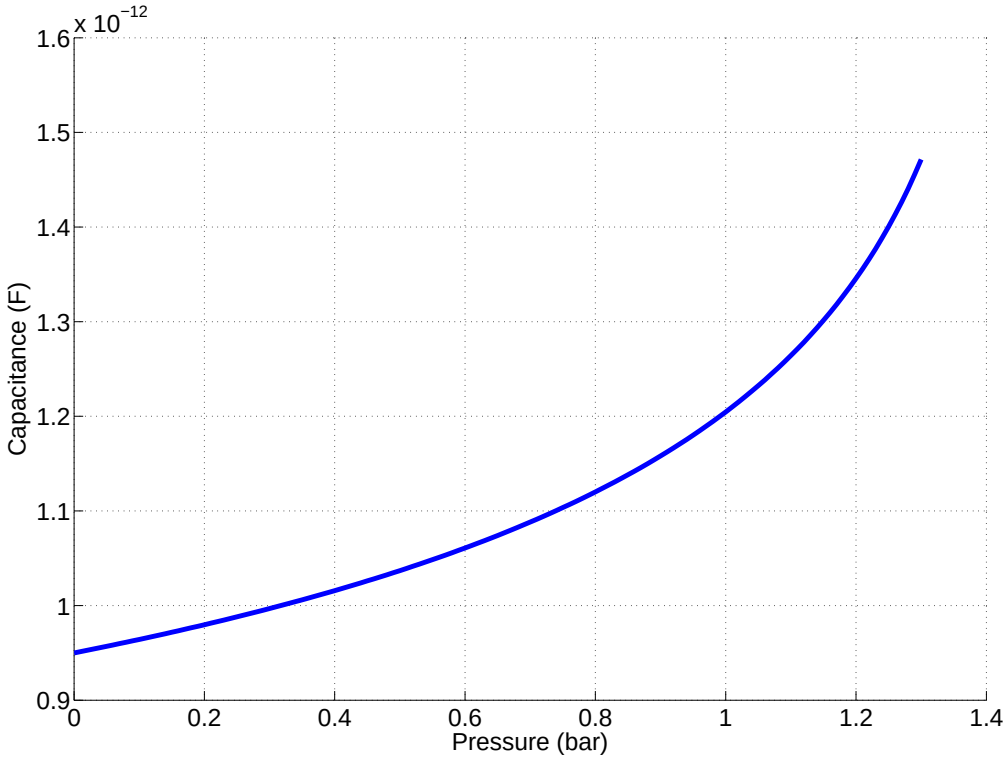


Figure 1-3: Pressure versus Capacitance characteristic [1]

of the sensor.

1-2 Target Specification

Table 1-2 tabulates the specification of the interface circuit. The prototype circuit will be designed in NXP 0.16μm CMOS process with 1 poly, 6 metal layers and 1.8V devices. The current state-of-the-art CDC achieves a FOM of about 1.4pJ/step [2]. The FOM is defined in Eq. (1-2) [3].

$$FOM = \frac{E_{meas}}{2^{ENOB}} \tag{1-2}$$

where E_{meas} is the energy consumption per measurement and ENOB is the effective number of bits. In our research work, we try to achieve a better performance than [2]. We attempt this by implementing several design techniques like *double sampling*, *system-level chopping* and a *novel inverter-based OTA*.

The circuit must be designed in such a way that the loading of the parasitic capacitance (C_{p1}, C_{p2}) should not affect the performance of the prototype. The prototype circuit should be designed in such a way that the performance has to be met regardless of whether the sensor is present off-chip or fabricated on the top of the die.

Target Parameter	**Requirement**
Pressure range	0 - 1.3 bar
Pressure resolution(at 1bar)	$<$ 0.01 mbar
Conversion time	$<$ 30 ms
Supply Voltage	1.2 - 1.8 V
FOM	$\leq$ 1.4pJ/step

Table 1-2: Target specifications of the prototype circuit

1-3 Organization of the Thesis

Chapter 2 deals with the system-level architecture of the prototype. The existing architecture called linear CDC [3] is shown and the operation of the CDC is explained. A novel architecture called non-linear CDC is proposed and analysed. The chapter then deals with a thorough noise and energy analysis of the existing CDC architecture and the proposed architecture.

Chapter 3 deals with the circuit implementation of the prototype. The design of various circuit blocks of the CDC are explained in detail. Several circuit techniques that are used to improve the energy-efficiency of the CDC are discussed.

Chapter 4 will discuss the simulation results of the prototype.

Chapter 5 concludes the thesis and summarizes the contributions of this research work.

Chapter 2

Architecture and Systematic Analysis of CDC

In this chapter we will introduce various technical terms that will be used throughout the thesis. Next, the existing CDC architecture is discussed in detail showing its pros and cons. Then we will propose a novel CDC architecture. The chapter presents various MATLAB algorithms wherever necessary and the corresponding results are shown.

2-1 CDC-Capacitance to Digital Converter

The prototype that we are implementing is used for measuring pressure as a digital output. The pressure sensor in which the transduction from mechanical domain (pressure) to electrical domain (capacitance) occurs is called the 'input transducer'. The digital output we get out of the prototype is a measure of the sensor capacitance (which in turn is influenced by the pressure), hence the prototype is aptly called as CDC or Capacitance to digital converter. The CDC is similar to the $\Delta\Sigma$ ADC. The comparison between the two is as follows [4]:

- The primary difference between $\Delta\Sigma$ ADC and the CDC are: In the case of a CDC, Capacitance is not known and a known voltage is applied to measure it. A reference quantity C_{ref} (reference capacitor) is used to measure the unknown capacitor. On the other hand, in a switched-capacitor $\Delta\Sigma$ ADC, the input voltage is not known and a known value of capacitance is applied. A reference quantity called V_{ref} is used to measure the unknown voltage.
- The similarity between the CDC and $\Delta\Sigma$ ADC is that they both work based on the principle of 'charge balancing'. In the context of CDC, it is explained as follows: the unknown capacitor C_x dumps an unknown charge Q_x in the negative feedback loop of the modulator. The reference capacitor C_{ref} dumps a known charge Q_{ref} in the feeback loop. Over time, the charge Q_x and Q_{ref} is made equal by the action of the

negative feedback loop. Hence the name Charge balancing. This concept is pictorially represented in Figure 2-1.

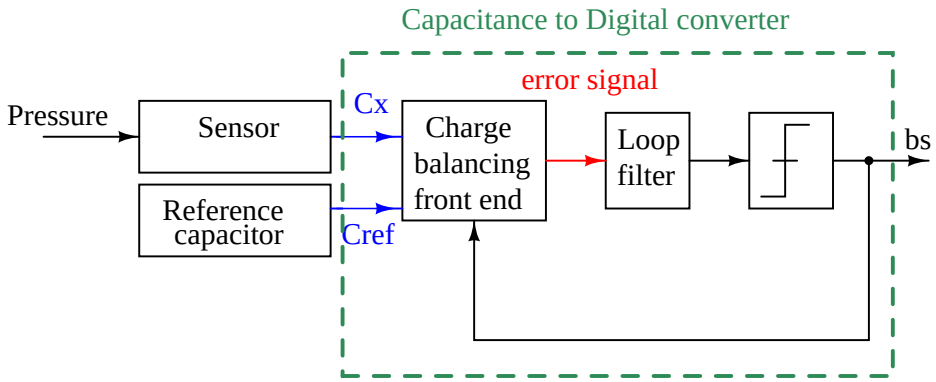


Figure 2-1: Conceptual Diagram of a CDC - illustrating the principle of charge balancing

The pressure versus sensor capacitance characteristics were discussed in Chapter 1. It shows that the capacitance corresponding to 0 bar is not 0 Farad but around 0.95pF. This value exists by default in the sensor and provides no useful information about the pressure. This capacitance is called as the 'baseline capacitance'. Thus any energy that is spent in transforming this capacitance into the digital output is futile and this capacitance has to be effectively cancelled. This is implemented in circuit level (in CDC) by another capacitor called as the Offset Capacitor referred to as C_{off}. The Offset capacitor is driven in anti-phase with respect to the sensor capacitor. Figure 2-2 shows a simple diagram of the implementation [5]. The equivalent capacitance present at the input of the OTA will then be (C_x-C_{off}).

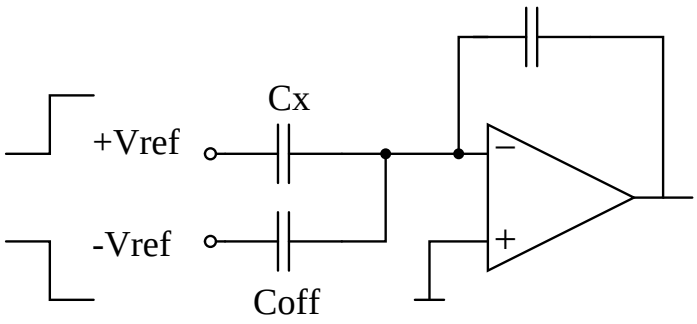


Figure 2-2: Electrical cancellation of Baseline Capacitance [5]

The use of C_{off} also helps us to effectively use the full output range of the CDC. This is shown using the MATLAB result that is shown in Figure 2-3. As we can see from the figure, the CDC without C_{off} doesn't use almost three-quarters of the dynamic range that is available. While the use of C_{off} has enabled the CDC to cover its entire output range.

2-2 Linear CDC - Existing Architecture

So far, we have seen the various terminologies that will be used throughout the thesis. We now come to the existing CDC architecture, which is called as linear CDC [3]. The conceptual

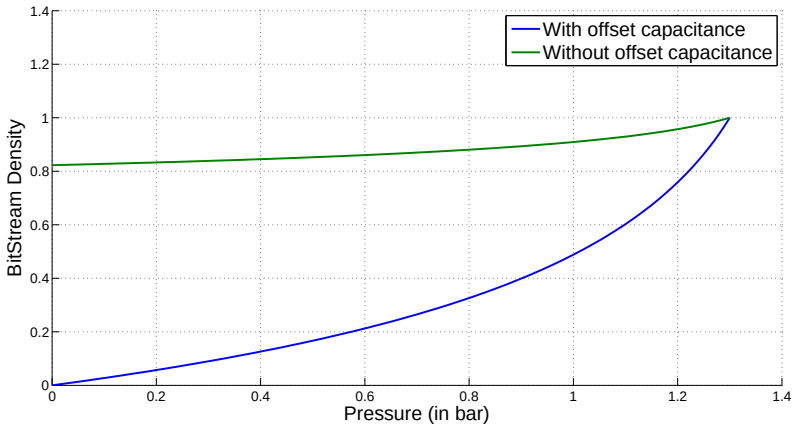


Figure 2-3: CDC output characteristics - with and without the use of Offset capacitance

block diagram of the linear CDC is shown in Figure 2-4. The expression that relates the bitstream density μ to the sensor capacitance C_x is given by (2-1). The principle of charge balancing implies that,

$$C_x - C_{off} - \mu.C_{ref} + (1-\mu).C_{ref} = 0$$
$$\mu = \frac{C_x - C_{off} + C_{ref}}{2C_{ref}} \tag{2-1}$$

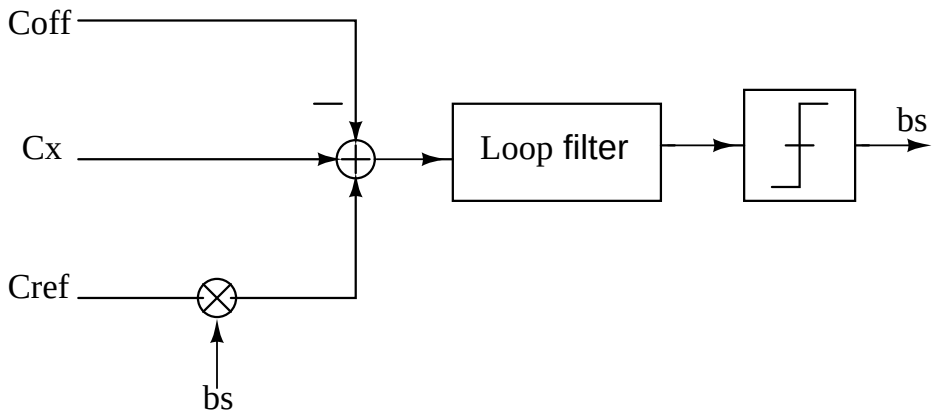


Figure 2-4: Conceptual diagram of a linear CDC

where the terms C_{off} and C_{ref} are the offset capacitor and reference capacitor respectively. Since the bitstream density and sensor capacitance are linearly related through (2-1), we will refer to this CDC as a linear CDC, in contrast with its non-linear counterpart that will be introduced in section 1-3. Depending on the range of μ, the CDC can be unipolar [μ =0 to 1] or bipolar CDC [μ = -1 to +1]. The output characteristic of the linear CDC as a function of pressure is shown in Figure 2-3 (the blue curve). A noticeable point is that the output characteristic is non-linear due to the non-linearity of the sensor. Thus to obtain a linear

one to one correspondence between pressure and digital output, a non-linear correction of the output of the CDC has to be done in the digital backend. Finally, the choice of Coff and Cref in a linear CDC can be understood by the following example. Suppose the capacitance range that has to be measured ranges from 1pF to 2pF. Then, we choose C_{off} to be at the midpoint of measurement range, that is 1.5pF (to cancel the baseline capacitance). The C_{ref} is chosen to be 0.5pF. Thus the whole measurement range from 1pF to 2pF is represented by $C_{off} \pm C_{ref}$.

The derivation shown in (2-1) is for a unipolar CDC. In case of a bipolar CDC, the (1-μ) term has to be neglected. The final equation will then be:

$$\mu = \frac{C_x - C_{off}}{C_{ref}}$$

2-3 Non-Linear CDC - A Novel Architecture

In this section we propose a novel CDC topology whose conceptual diagram is given in Figure 2-5. The corresponding expression for the non-linear CDC is given in (2-2). The derivation for this equation can be directly obtained from the charge balancing equation (similar to the derivation in Eq. (2-1)). This equation will also be derived while doing noise analysis (in later sections of the chapter), hence it is not mentioned here.

$$\mu = \frac{(\alpha + \beta)C_x + C_{ref}(\gamma + \delta)}{2(\beta C_x + \delta C_{ref})} \tag{2-2}$$

The output characteristics of the non-linear CDC is given in Figure 2-6. As seen in Figure 2-6, the output characteristics is an almost linear function of pressure. We can also clearly see from the graph that the sensitivity of the characteristics ($\frac{d\mu}{dP}$) is almost uniform throughout the entire measurement range of pressure for the non-linear CDC. Whereas for the linear CDC, ($\frac{d\mu}{dP}$) varies across pressure.

The qualitative discussion for the non-linear CDC is as follows:

- The expression for μ of linear CDC, has C_x in the numerator alone, hence the non-linearity of the C_x versus Pressure characteristics directly gets translated into non-linearity in the output characteristics of the CDC. Whereas in the non-linear CDC the C_x term is introduced in both numerator and denominator thus partially cancelling the non-linearity.
- Another way to look at the expression is that, the reference capacitor of the linear CDC given in the denominator of Eq. (2-1) is constant. In our non-linear CDC, the denominator term of Eq. (2-2) is dynamically changing as a function of pressure.
- The final difference can be clearly seen from the conceptual circuit diagram. The C_x of non-linear CDC is controlled by bitstream output whereas in the case of linear CDC, it is not true.

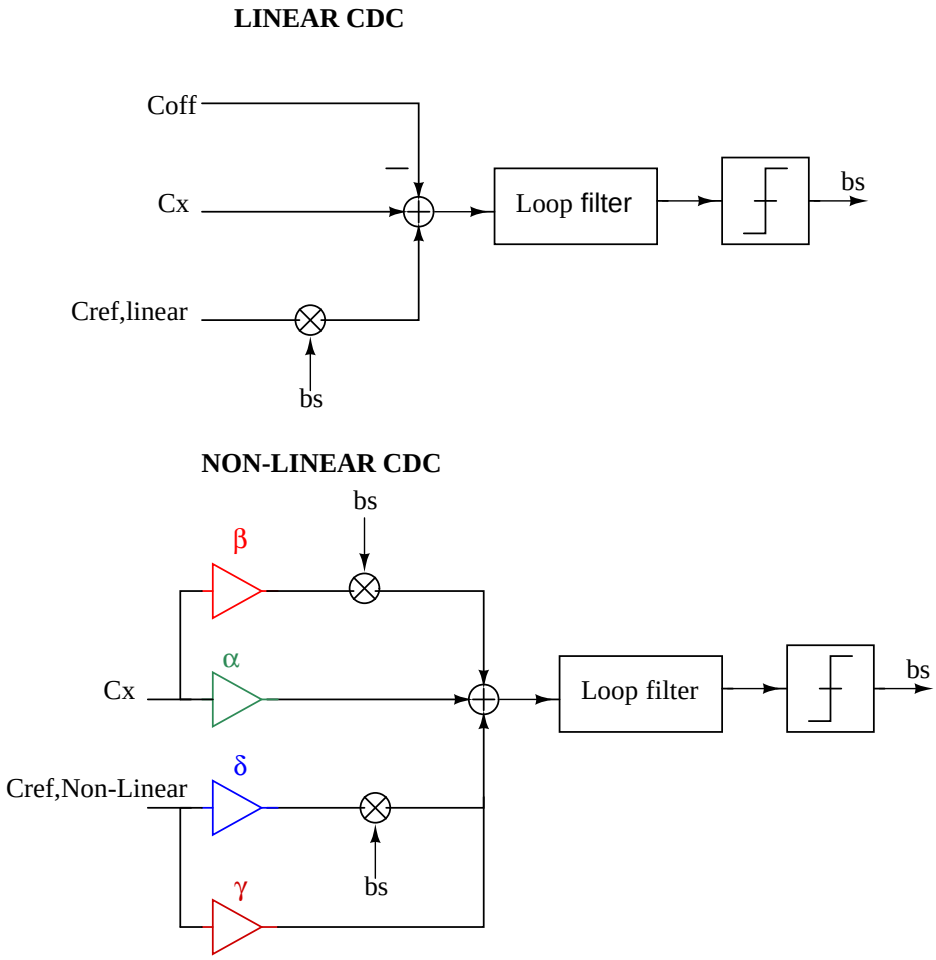


Figure 2-5: Conceptual diagram of non-linear CDC (along with linear CDC for comparison)

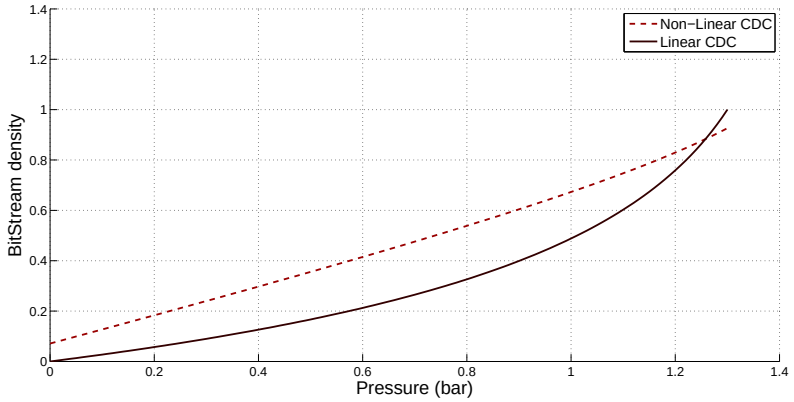


Figure 2-6: Comparison of output of linear CDC and non-linear CDC

- It can be clearly seen that the linear CDC is a special case of the non-linear CDC, when appropriate values are chosen for the co-efficients $\alpha, \beta, \delta, \gamma$.
- In the linear CDC, to obtain a linear relation between Pressure and digital output a non-linear correction has to be applied in the digital backend. Whereas, in the non-linear CDC, we do the non-linear correction in the analog frontend.

2-4 Non-Linear CDC - Determination of the Co-efficients

In this section we will try to determine the values of the co-efficient $\alpha, \beta, \delta, \gamma$. An algorithm to find out the coefficients was implemented in MATLAB. The algorithm is given as follows:

- The first step is to limit the search in the design space while choosing the value of a coefficient. There are some constraints that can be placed on the value of coefficients. The coefficients α, β (which are the coefficient of the sensor capacitance) should be integer numbers. This is because the value of sensor capacitance is a given design spec for the designer and cannot be sized like the capacitors available in the CMOS process. The physical meaning of the coefficient is as follows: Suppose the value of $\alpha = 2$, then the sensor capacitance should be integrated twice in a clock period.
- The rest of the coefficients δ, γ can be any decimal value, since they are on-chip capacitors in CMOS process. Their value is swept in the program between $[-5 \leq \delta, \gamma \leq 5]$ in steps of 0.1.
- Since this is a unipolar CDC, the value of μ should lie in the range of $[0 \leq \mu \leq 1]$. This constraint helps in validating the output of the CDC.
- The coefficients $\alpha, \beta, \delta, \gamma$ are varied in nested FOR loops. Thus for every iteration we get a value for μ and a set of four coefficients $(\alpha, \beta, \delta, \gamma)$ that were given as the input.
- Now to find out the optimal coefficients we define a Figure of Merit (FOM), which is given by Eq. (2-3). The terms that are present in the formula is clearly indicated in the Figure 2-7, which shows the expected pressure versus bitstream density(μ) curve. The black line shows a typical measurement curve and the red line indicates a first order fit line done in MATLAB for the curve. The FOM is similar to that of a typical INL measurement done in ADC's.

$$FOM = \frac{\text{peak INL}}{\text{bit-stream density range}} \tag{2-3}$$

- The smallest FOM corresponds to the best or optimal set of coefficients. The minimum FOM we obtained was 0.0625. For additional details refer to Appendix A.

The value of the coefficient obtained from MATLAB based on the algorithm above are as follows: $\alpha =$ **-2,** $\beta =$**-1,** $\delta =$ **0.6,** $\gamma =$**2.2**. The output characteristics of the non-linear CDC for the corresponding coefficients is shown in Figure 2-6.

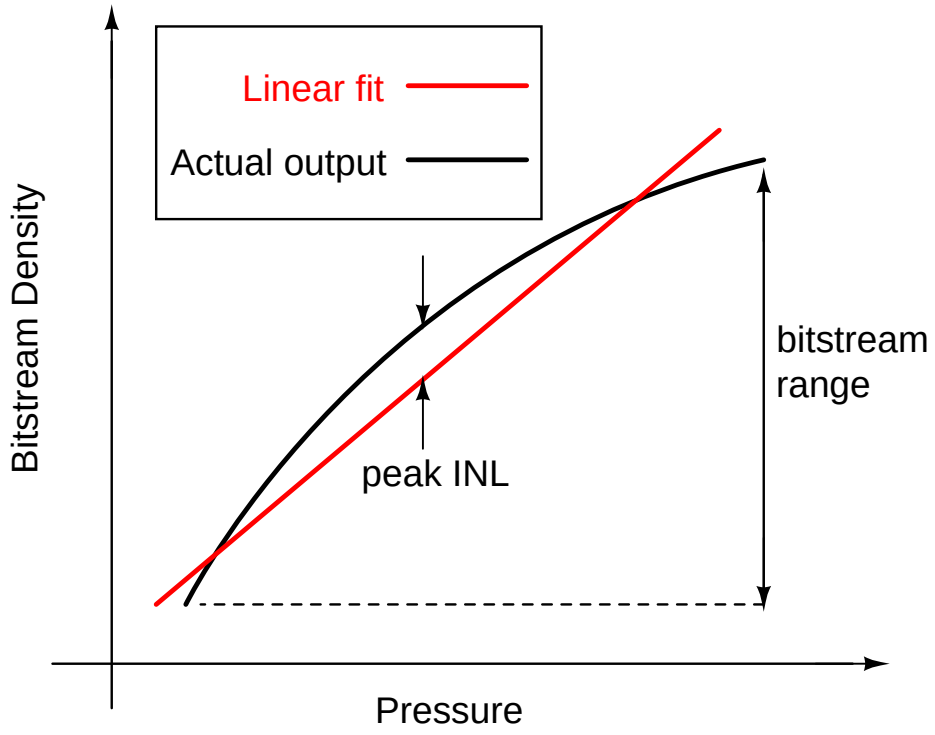


Figure 2-7: FOM used for determining the optimal coefficients for an non-linear CDC

2-5 Motivation for Noise and Energy-Efficiency Analysis

Until now, we have introduced the linear and non-linear CDC architectures. In this section, let's take a detour and perform the noise analysis of the linear CDC and the non-linear CDC. The motivation is as follows:

- In the following sections of the chapter, we will do noise analysis and compare the performance of the two CDCs. The reason is that noise (*thermal noise* - to be more specific) is the fundamental limiting factor in the performance of a CDC (or any physical system for that matter). We will then relate the noise parameters to the pressure resolution of the CDC and compare the performance of the two CDC. Another motivation for doing the noise analysis is that it lays the foundation for the *systematic design of CDC*. It is worth mentioning here that, this type of systematic noise analysis of a CDC is not found in the open literature.
- We will then compare the two CDC architectures in terms of their *quantization noise*. This will help us in choosing the Order of the modulator for the corresponding CDC architecture.
- Then we will derive equations that relate *energy consumption* of the CDC to the physical parameters of the CDC. The energy-efficient CDC architecture will then be chosen and then the CDC will be implemented in the further chapters. The main goal of this research is energy efficiency, hence we perform these analysis that are essential to understand pros, cons and fundamental limitations of the CDC.

In the following analyses, our approach is as follows:

- We will first make *quantitative discussion* about the topic, in form of mathematical derivations that link the physical parameters of the CDC to its performance.
- We will illustrate the important equation using graphs and make a *qualitative reasoning* of the equation. In other words, we will attempt to make the physical sense of the equation.
- Finally, we will *compare the performance* of the two CDCs and make the *conclusion* regarding which CDC is better in terms of energy-efficiency.

2-6 Comparison of Noise Performance of Linear and Non-Linear CDC

2-6-1 Linear CDC - Noise Analysis

Now let us perform the thermal noise analysis for the linear CDC architecture. The derivation follows similar noise analysis procedure given in Chapter 5 of [6] and uses the results from [7]. We assume that the charge balancing is implemented using a switched-capacitor integrator built using an OTA and that all the capacitors are charged using a reference voltage V_{ref}. Hence the charge is of the form '$C.V_{ref}$'.

The principle of charge balancing implies that the total charge accumulated ($q_{accumulated}$) at the input of the loop filter should be 0.

$$\begin{aligned} q_{accumulated} &= 0 \\ &= q_{S0} + q_{S1} + q_{noise} + q_{sig} \end{aligned} \tag{2-4}$$

where q_{S0} is the signal charge dumped by the capacitor C_{ref} when the bit stream is 0, q_{S1} is the signal charge dumped by the capacitor C_{ref} when the bit stream is 1, q_{noise} is the noise charge that is dumped into the input node of the loop filter due to thermal noise, q_{sig} is the signal charge dumped by the capacitor C_x.

Now let's calculate q_{noise} (from Eq. (2-4)), which is given as follows:

$$\overline{q_{noise}^2} = \overline{q_{n1}^2} + \overline{q_{n0}^2} + \overline{q_{n,sig}^2} \tag{2-5}$$

where q_{n1} is the (thermal) noise charge dumped by the capacitor C_{ref} when the bit stream is 1, q_{n0} is the noise charge dumped by the capacitor C_{ref} when the bit stream is 0, $q_{n,sig}$ is the noise charge dumped by the capacitor C_x. After 'N' clock cycles,

$$\overline{q_{n1}^2} = k.T(\mu.C_{ref})N.\xi \tag{2-6}$$

where T is the temperature, k is the Boltzmann constant, μ is the bit stream density and ξ is the design parameter that relates the g_m - the transconductance of the OTA and R_{on} - the switch resistance [7]. ξ is given by, $\xi = \frac{7/3+2x}{1+x}$, where x = $2g_m.R_{on}$.

$$\overline{q_{n0}^2} = k.T((1-\mu).C_{ref})N.\xi \tag{2-7}$$

$$\overline{q_{n,sig}^2} = k.T(C_x)N.\xi \tag{2-8}$$

Combining equations Eq. (2-6), Eq. (2-7) and Eq. (2-8), we get,

$$\begin{aligned} \overline{q_{noise}^2} &= k.T.N.\xi(\mu.C_{ref} + (1-\mu)C_{ref} + C_x) \\ \overline{q_{noise}^2} &= k.T.N.\xi(C_{ref} + C_x) \end{aligned} \tag{2-9}$$

From Eq. (2-4), we get

$$\begin{aligned} q_{S0} + q_{S1} + q_{sig} &= -q_{noise} \\ V_{ref}.((-N.\mu.C_{ref} + N.(1-\mu)Cref + N.C_x)) &= -q_{noise} \\ V_{ref}.(-2.\mu.C_{ref} + C_{ref} + C_x) &= \frac{-q_{noise}}{N} \\ V_{ref}.(C_{ref} + C_x) + \frac{q_{noise}}{N} &= \mu.(2C_{ref}).V_{ref} \\ \mu &= \frac{C_{ref} + C_x}{2C_{ref}} + \frac{q_{noise}}{N.(2C_{ref}).V_{ref}} \end{aligned} \tag{2-10}$$

The first term in the RHS of Eq. (2-10) is the expression which gives the relation between the mean value of μ and C_x. The second term is the uncertainty in μ that is denoted as σ_μ. The uncertainty σ_μ for a linear CDC is obtained by substituting Eq. (2-9) in Eq. (2-10).

$$\sigma_\mu = \frac{\sqrt{k.T.\xi(C_{ref} + C_x)}}{\sqrt{N}.2C_{ref}.V_{ref}} \tag{2-11}$$

Eq. (2-11) makes qualitative sense. The more the value of capacitance the more is the value of noise charge (in the form 'kTC') that is dumped into the loop filter, hence more uncertainty (It is to be noted that $C_x >> C_{ref}$ due to the baseline capacitance). And the term σ_μ is inversely proportional to N which also makes sense, the more the number of clock cycles N, the more is the number of samples, the lesser the thermal noise (better averaging). The uncertainty in μ (σ_μ) can be translated into uncertainty in Pressure($\sigma_{Pressure}$) using

$$\sigma_{Pressure} = \sigma_\mu(\frac{\partial Pressure}{\partial \mu}) \tag{2-12}$$

This is done simply because we are dealing with a Pressure sensor application and it makes more sense to tell the uncertainty (caused due to thermal noise in the circuit) in terms of Pressure - which is the only concern for the end user of the prototype. The term ($\frac{\partial Pressure}{\partial \mu}$) represents the slope of 'μ versus pressure' characteristic of the linear CDC.

2-6-2 Non-Linear CDC - Noise Analysis

The thermal noise analysis derivation of non-linear CDC follows exactly the same procedure that was done for linear CDC. The notations are the same, hence it is not repeated here.

The only difference is the presence of the Coefficients $\alpha, \beta, \delta, \gamma$ which are present only for the non-linear CDC.

$$\begin{aligned} q_{accumulated} &= 0 \\ &= q_{S0} + q_{S1} + q_{noise} + q_{sig} \end{aligned} \tag{2-13}$$

Now let's calculate q_{noise} (from Eq. (2-13)), which is given as follows:

$$\overline{q^2_{noise}} = \overline{q^2_{n1}} + \overline{q^2_{n0}} + \overline{q^2_{n,C_x}} + \overline{q^2_{n,C_{ref}}} \tag{2-14}$$

$$\overline{q^2_{n1}} = k.T(\mu.\beta C_x + \mu.\delta.C_{ref})N.\xi \tag{2-15}$$

$$\overline{q^2_{n0}} = k.T((1-\mu).\beta C_x + (1-\mu).\delta C_{ref})N.\xi \tag{2-16}$$

$$\overline{q^2_{n,Cx}} = k.T(\alpha.C_x)N.\xi \tag{2-17}$$

$$\overline{q^2_{n,C_{ref}}} = k.T(\gamma.C_{ref})N.\xi \tag{2-18}$$

Substituting Eq. (2-15), Eq. (2-16), Eq. (2-17), Eq. (2-18) in Eq. (2-14), we get

$$\begin{aligned} \overline{q^2_{noise}} &= k.T.N.\xi(\alpha.C_x + \delta.C_{ref} + \mu.(\beta.C_x + \delta.C_{ref}) \\ &\quad + (\beta.Cx + \delta.C_{ref}) - (\mu.\beta.C_x + \mu.\delta.C_{ref})) \\ \overline{q^2_{noise}} &= k.T.N.\xi(\alpha.C_x + \gamma.C_{ref} + \beta.C_x + \delta.C_{ref}) \end{aligned} \tag{2-19}$$

From Eq. (2-13), we get

$$\begin{aligned} q_{S0} + q_{S1} + q_{sig} &= -q_{noise} \\ -q_{noise} &= V_{ref}.(N((1-\mu)\beta.C_x + (1-\mu).\delta.C_{ref} + (-\mu.\beta.Cx) - \mu.\delta.C_{ref} + \alpha.C_x + \gamma.C_{ref})) \\ \frac{-q_{noise}}{N} &= V_{ref}.((\beta.C_x + \delta.C_{ref} + \alpha.C_x + \gamma.C_{ref}) - 2.\mu.\beta.C_x - 2.\mu.\delta.C_{ref}) \\ \mu &= \frac{(\alpha+\beta)C_x + C_{ref}(\gamma+\delta)}{2.(\beta.Cx + \delta.C_{ref})} + \frac{q_{noise}}{N.V_{ref}.(2.\beta.C_x + 2.\delta.C_{ref})} \end{aligned} \tag{2-20}$$

The first term in the RHS of Eq. (2-20) is the actual expression which gives the relation between μ and C_x. The second term is the uncertainty in μ, that is denoted as σ_μ. The uncertainty σ_μ for a non-linear CDC is obtained by substituting Eq. (2-19) in Eq. (2-20), as shown in Eq. (2-21). The uncertainty in μ can be referred back to the input as uncertainty in Pressure($\sigma_{Pressure}$) using Eq. (2-12).

$$\sigma_\mu = \frac{\sqrt{k.T.\xi.[(\alpha+\beta)C_x + (\gamma+\delta)C_{ref}]}}{|\sqrt{N}.V_{ref}(2\beta C_x + 2\delta C_{ref})|} \tag{2-21}$$

Figure 2-8 compares the σ_μ of both the linear and non-linear CDC. The graph is obtained from Eq. (2-11) and Eq. (2-21). In the MATLAB simulation, we assumed the following. For both linear and non-linear CDC, we set $V_{ref} = 1$V and N = 400. The value of C_{ref} for linear CDC was chosen such that the value $\pm C_{ref}$ can cover the measurement range of C_x. The

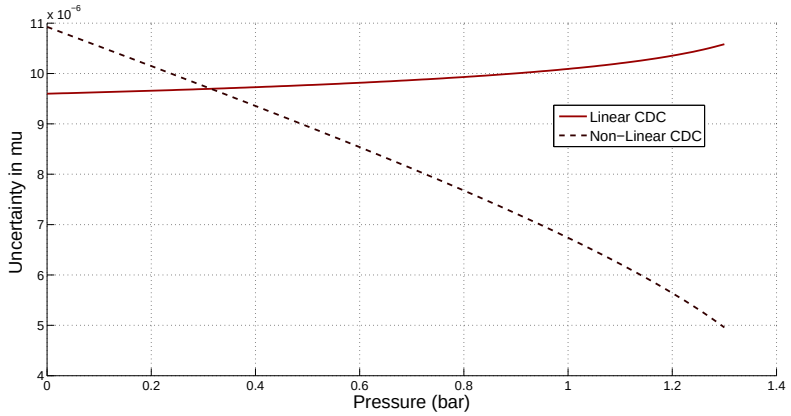


Figure 2-8: Uncertainty in μ

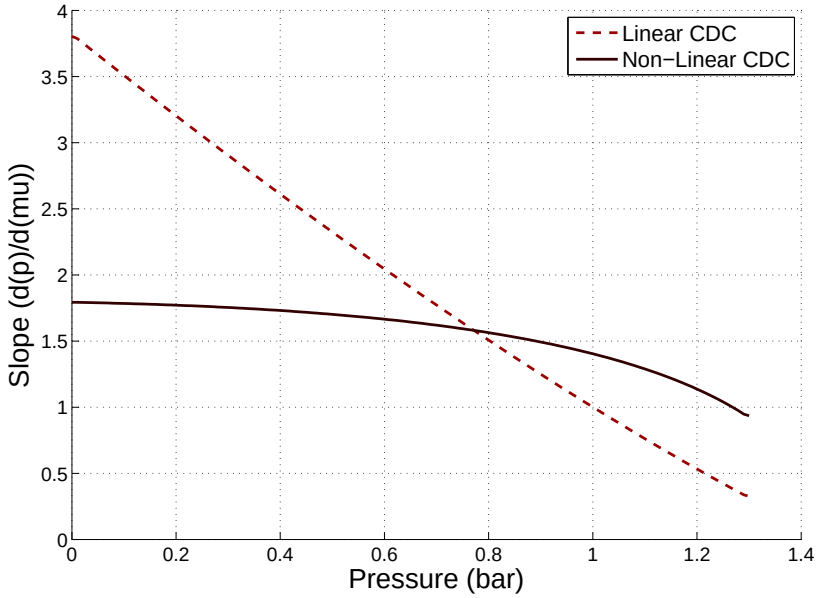


Figure 2-9: Pressure Slope

value of C_{ref} for non-linear CDC was chosen to be 1pF. Figure 2-9 shows the variation of $(\frac{\partial Pressure}{\partial \mu})$ versus Pressure. Since the non-linear CDC has a linear digital output we get an almost constant slope. Whereas the linear CDC has a non-linear digital output, hence its slope changes throughout the graph. For comparison, we calculate the fundamental limit of a given sensor capacitance C_x due to thermal noise assuming the capacitor is read out by an ideal, noise-free circuit :

$$\sigma_C = \frac{\sqrt{kT.C_x}}{V_{ref}.\sqrt{N}} \tag{2-22}$$

This uncertainty in capacitance (σ_C) can be referred back to the input as uncertainty in pressure ($\sigma_{Pressure,fundamental}$) using Eq. (2-23).

$$\sigma_{Pressure,fundamental} = \sigma_C(\frac{\partial Pressure}{\partial C}) \tag{2-23}$$

where the term $(\frac{\partial Pressure}{\partial C})$ can be obtained from the pressure versus capacitance characteristic. The results of the pressure uncertainty of linear, non-linear CDC and the pressure uncertainty due to a sensor capacitance C_x are shown in Figure 2-10. An interesting point to be noted in Figure 2-10, is that the performance of non-linear CDC exceeds the performance imposed by the fundamental limit (the area is highlighted using the circle). The reason for this behaviour is due to the fact that the coefficients α, β together add and contribute a factor of 3 to the value of sensor capacitance C_x. Thus the sensor capacitance of the non-linear CDC manifests itself as a bigger capacitance $(3.C_x)$ and leads to the better performance.

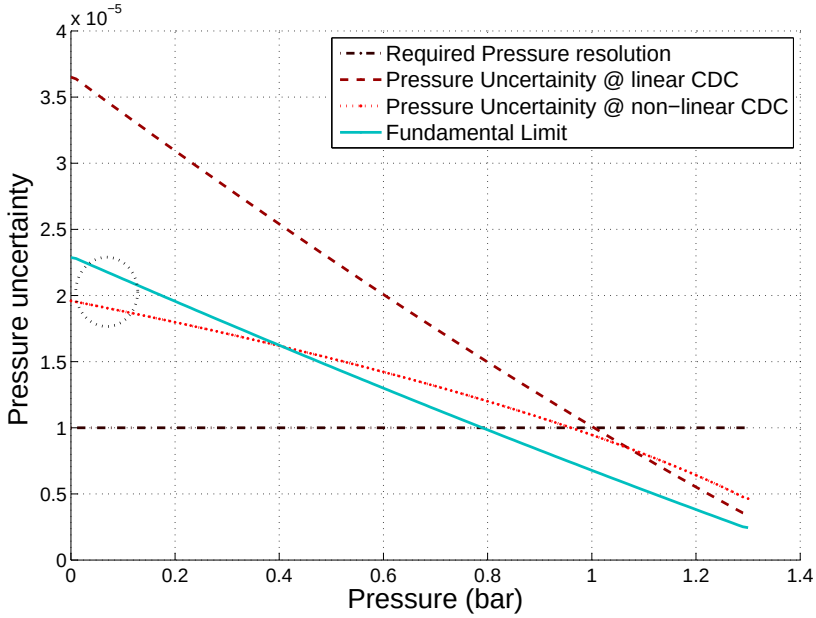


Figure 2-10: Uncertainty in pressure

2-7 Monte-Carlo Analysis

The results obtained from noise analysis will be used in the rest of the sections of this chapter. The first analysis that we do is the Monte-Carlo analysis. The motivation is as follows. The natural question that one asks after having a look at the values of the coefficients $(\alpha, \beta, \delta, \gamma)$ of the non-linear CDC is, "What happens to the output of the CDC if the coefficients change their values due to process variations ?". Similar concerns arise for the value of the capacitors C_{off} and C_{ref} present in Eq. (2-1) of the linear CDC. Hence we have done Monte-Carlo simulations in MATLAB to understand the effect of process variations. The following parameters shown in Table 2-1 are set for the Monte-Carlo simulation:

Parameter	Variation
Reference capacitor Variation	± 10%
Sensor cap - Slope variation	± 5%
Sensor cap - Baseline capacitance variation	± 2.5%
No. of Monte-Carlo runs	1000 runs

Table 2-1: Input parameters for the Monte-Carlo sim [1]

It is to be noted in all the following analysis the number of clock cycles was kept as 100, for both linear and non-linear CDC. In the Monte-Carlo simulation, we assumed a normal distribution with zero mean for the process parameters and the values provided in Table 2-1 represent the value of σ. The impact of process variation on the sensor capacitance is shown in Figure 2-11 and Figure 2-12.

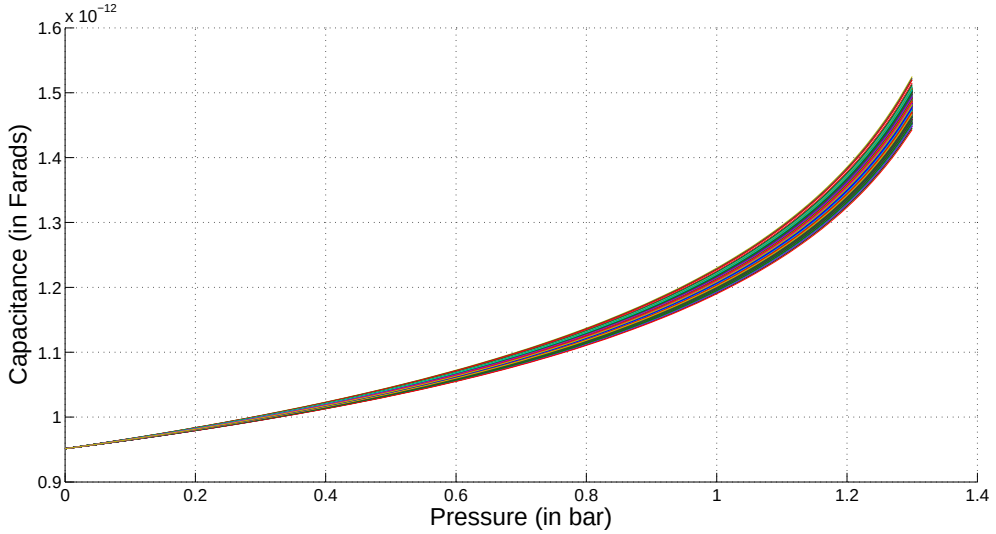


Figure 2-11: Process variation impact on sensor capacitance (only ± 5% slope variation)

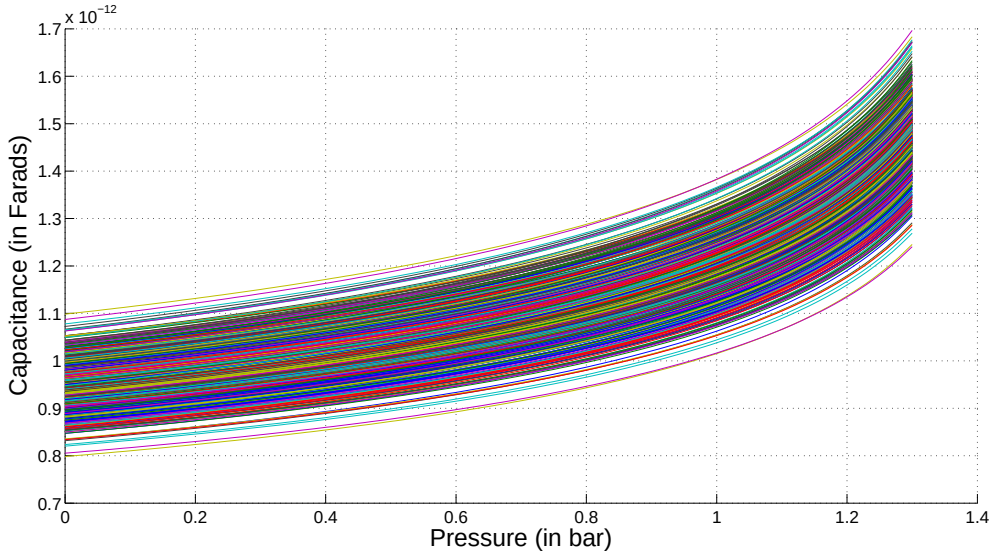


Figure 2-12: Process variation impact on sensor capacitance (both $\pm$ 5% slope & $\pm$ 2.5%baseline capacitance variation)

2-7-1 Monte-Carlo Analysis of Linear CDC

The bit stream density versus pressure characteristic for the linear CDC is shown in Figure 2-13. As it can be seen from the figure, the CDC output (μ) crosses the upper and lower bounds '1' and '0' respectively. Hence we introduce a calibration scheme to bring the CDC output in the allowed range ($0 \leq \mu \leq 1$).

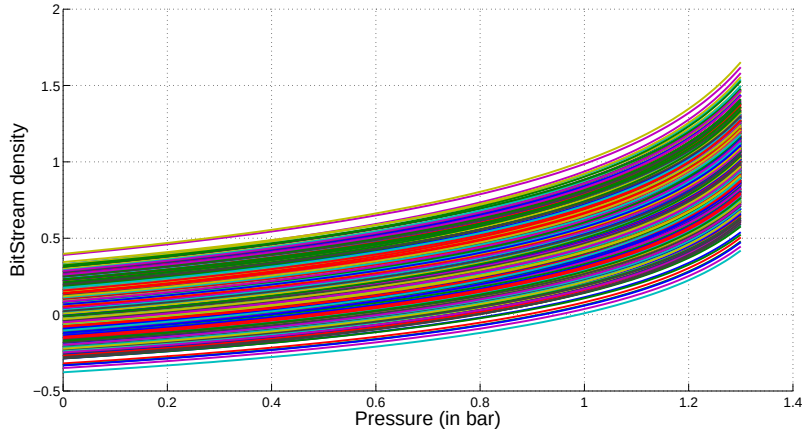


Figure 2-13: Output Characteristics of linear CDC (due to process variations - without calibration)

We apply the following 2-point calibration algorithm in MATLAB:

- **Step 1:** Let us take two pressure points 'P1' and 'P2' as our data points where we do the calibration. They are **0 bar** and **1.3 bar** respectively.

- **Step 2:** The formula for the calculation of the bitstream density μ for a linear CDC is given by:

$$\mu = \frac{C_x - C_{off} + C_{ref}}{2C_{ref}} \tag{2-24}$$

In the above formula, we will introduce two coefficient $[\theta, \eta]$ whose purpose is to compensate for the process variations. The Coefficient θ is for compensating the gain error. The Coefficient η is for compensating the offset error. The formula for μ including the tuning coefficients is given below.

$$\mu = \frac{C_x - \eta.C_{off} + \theta.C_{ref}}{2.\theta.C_{ref}} \tag{2-25}$$

- **Step 3:** The range of η is chosen to be $[0.85 \leq \eta \leq 1.2]$ (in steps of 0.05, with a total of 12 steps) and the range of θ is from $[0.85 \leq \theta \leq 1.4]$ (in steps of 0.05 with a total of 8 steps). For every tuning step in the MATLAB program, we get two value for bitstream density, μ_1 and μ_2 corresponding to the pressure points P1 and P2. Since, these two pressure points are the extreme pressure points for our application, we know that the value of μ_1 should be greater than 0 and the value of μ_2 should be less than 1(which is the maximum value of μ). The values of coefficients η , θ that satisfy the above condition are chosen for a particular monte-carlo(process variation) run. The bit-stream versus pressure characteristic for the linear CDC after the application of 2-point calibration is shown in Figure 2-14. Thus as seen from the figure we get an yield of almost 100%.

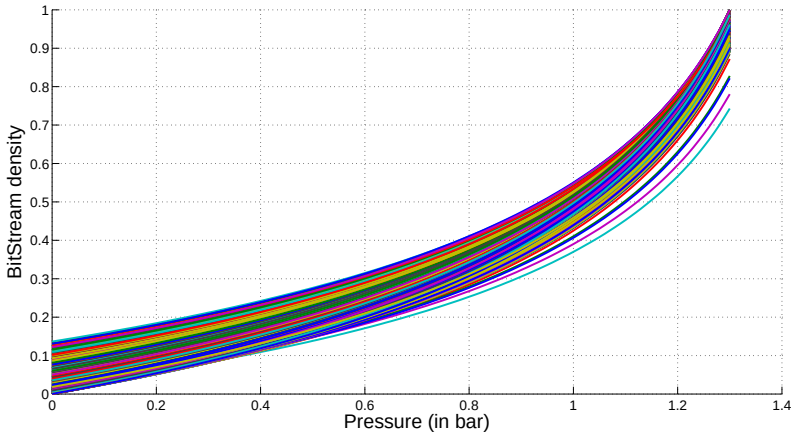


Figure 2-14: Output Characteristics of linear CDC (due to process variations - with calibration)

2-7-2 Summary of Monte-Carlo Simulation Results for Linear CDC

The process variations give rise to variation in the uncertainty in the measured pressure. The calibration helps to reduce this uncertainty in measured pressure. The summary of the Monte-Carlo simulation is as follows. From bitstream density(μ) versus pressure characteristics: (Figure 2-13 & Figure 2-14) the valid linear CDC output without tuning is 9 out of 1000

runs. The valid linear CDC output with tuning is 1000 out of 1000 runs.The histogram plot results in Figure 2-15, shows that the mean of pressure uncertainty($\sigma_{Pressure}$) at 1bar is 1.6267e-005 (The spec is to have a pressure resolution of 1e-5 at 1bar. We can achieve this by increasing number of cycles, which is currently set to 100. The main goal here was to demonstrate the effectiveness of the calibration, which was clearly achieved by making sure that the CDC output didn't saturate throughout the required pressure measurement range).

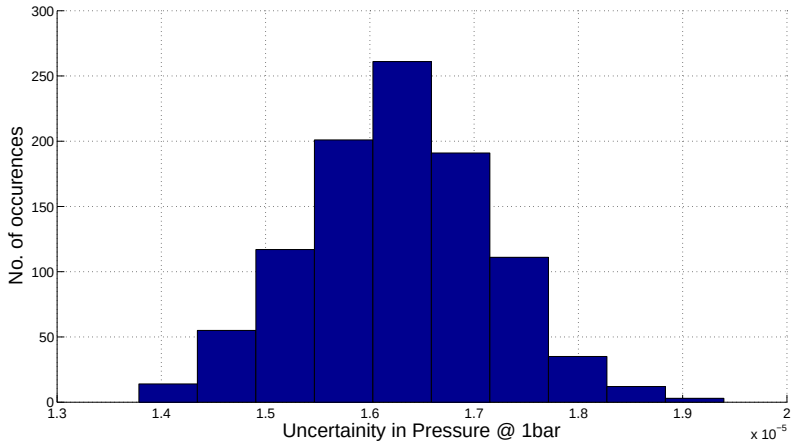


Figure 2-15: Histogram plot of the Uncertainty in Pressure (@ 1bar) - linear CDC

2-7-3 Monte-Carlo Analysis of Non-Linear CDC

The bit-stream denisty versus pressure characteristic for the non-linear CDC is shown in Figure 2-16 due to process variation. The values of $\alpha, \beta, \delta, \gamma$ were kept constant, while their capacitive coefficients are subjected to the process variation.

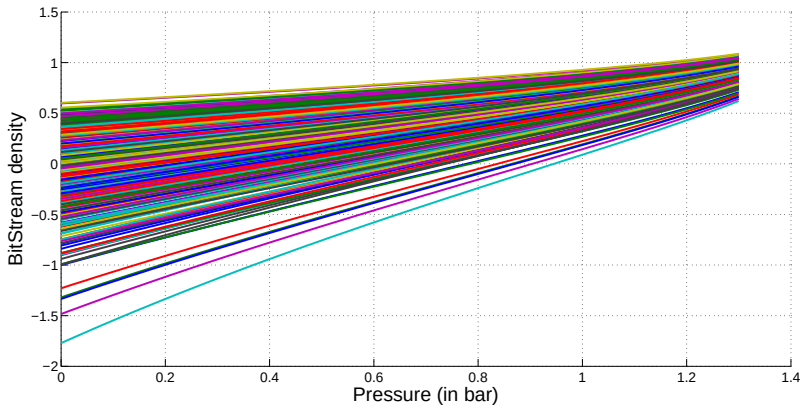


Figure 2-16: Output Characteristics of non-linear CDC (due to process variations - without calibration)

The algorithm of the 2-point calibration procedure for the non-linear CDC (to compensate for the process variation) is explained below:

- **Step 1:** Let us take two pressure points 'P1' and 'P2' as our data points where we do the calibration. They are **0 bar** and **1.3 bar** respectively.
- **Step 2:** The formula for the calculation of the bitstream density μ for a non-linear CDC is given by:

$$\mu = \frac{(\alpha + \beta)Cx + Cref(\gamma + \delta)}{2(\beta Cx + \delta Cref)} \tag{2-26}$$

  In the above formula, we will tune the coefficient $[\delta, \gamma]$ whose purpose is to compensate for the process variations. The Coefficient γ is for compensating the gain error. The Coefficient δ is for compensating the offset error.

- **Step 3:**The range of δ is $[0.5 \leq \delta \leq 0.7]$ (in steps of 0.05, with a total of 5 steps) and the range of γ is $[1.7 \leq \delta \leq 2.8]$(in steps of 0.1, with a total of 12 steps). For every tuning step in the MATLAB program, we get two value for μ_1 and μ_2 corresponding to the pressure points P1 and P2. Since, these two pressure points are the extreme pressure points for our application, we know that the value of μ_1 should be greater than 0 and the value of μ_2 should be less than 1(which is the maximum value of μ). The value of co-efficient δ,γ that satisfy the above condition is chosen for a particular monte-carlo(process variation) run. In addition to the above criterion we have chosen another parameter for filtering, which is (μ_1 - μ_2), which gives the range covered by the CDC output. This is to ensure that the CDC output uses the maximum dynamic range that is available. This is the only difference between co-efficient tuning of the linear and Non- linear CDC.

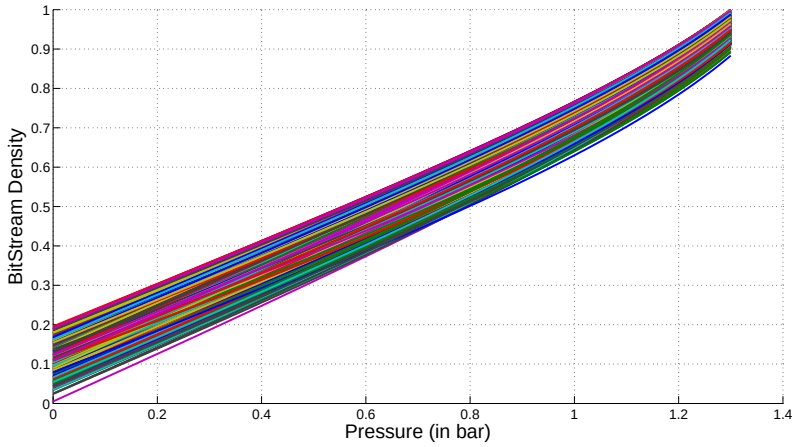


Figure 2-17: Output Characteristics of non-linear CDC (due to process variations - with calibration)

The bit-stream versus pressure characteristic for the non-linear CDC after the application of 2-point calibration is shown in Figure 2-17. Thus as seen from the figure we get an yield of almost 100% after tuning.

2-7-4 Summary of Monte-Carlo Simulation Results for Non-Linear CDC

From Bitstream density versus Pressure Characteristics: (Figure 2-16 & Figure 2-17) The valid non-linear CDC output without tuning is 477 out of 1000 runs. The valid non-linear CDC output with tuning is 1000 out of 1000 runs. The Histogram plot in result in Figure 2-18, shows that the mean of pressure uncertainty at 1bar is 1.94872e-005.

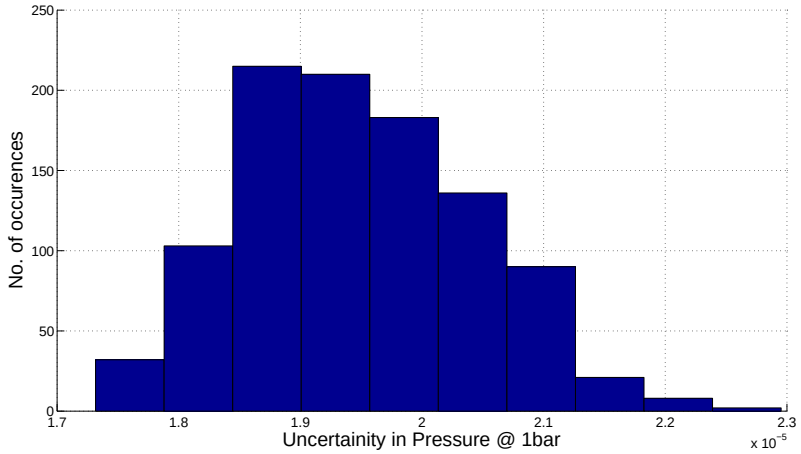


Figure 2-18: Histogram plot of the uncertainty in pressure (@ 1bar) - non-linear CDC

2-8 Energy Efficiency Calculations

2-8-1 Energy Consumption of Linear CDC

In this section, we will derive the theoretical predictions for the energy consumption of the two CDCs. The CDC that results in low energy consumption clearly will be the winner in terms of energy-efficiency. The derivation follows similar analysis procedure given in [8]. Consider the Figure 2-19, which shows a simplified capacitive sensor interface. This circuit is a simple representation of any switched-capacitor (capacitive) sensor interface circuit. During the clock phase Φ_1, the capacitor 'C_x' is charged to V_{ref}. Then during the clock phase Φ_2, the charge '$C_x.V_{ref}$' is transferred to the integration capacitor 'C_{int}'. The transconductance of the OTA is denoted as 'g_m'.

Assuming exponential settling, the minimum required 'g_m', to achieve the required accuracy (which is usually 0.5LSB), is calculated as follows.

$$g_m = \frac{C_x + Cref}{\tau} = \frac{(C_x + C_{ref})K}{T_2}$$

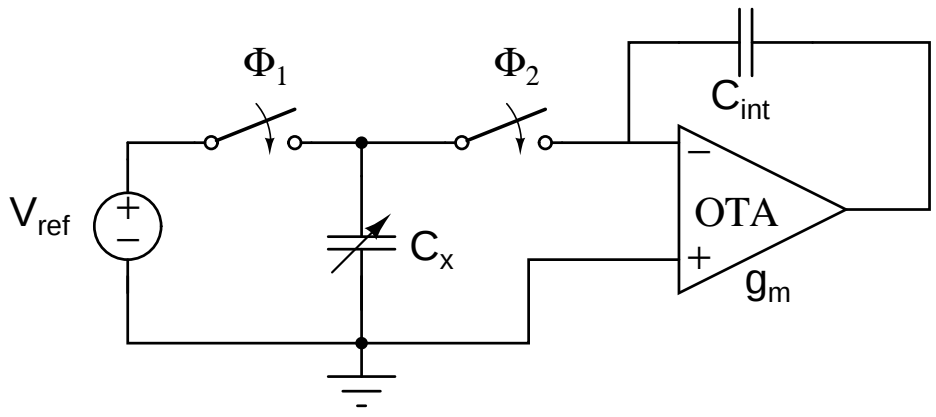


Figure 2-19: Simplified capacitive interface circuit [8]

Where $\tau = \frac{C_x}{g_m}$, K = $ln(2^{ENOB+1})$ and T_2 is the duration of the clock phase Φ_2. The energy consumption during Φ_2 is :

$$E_2 = T_2.V_{supply}.I_{OTA}$$
$$E_2 = T_2.V_{supply}.\frac{I_{OTA}}{g_m}.g_m$$
$$E_2 = (C_x + C_{ref}).K.V_{supply}.\frac{I_{OTA}}{g_m}$$

The energy consumption during Φ_1 is

$$E_1 = (C_x + C_{ref}).V_{ref}^2$$

The total energy consumption during a single clock phase is

$$E = E_1 + E_2$$

Assuming $V_{supply} = V_{ref}$, we get

$$E = (C_x + C_{ref}).V_{supply}^2 + (C_x + C_{ref}).K.\frac{I_{OTA}}{g_m}.\frac{1}{V_{supply}} \tag{2-27}$$

Eq. (2-27) gives the total energy consumption of the linear CDC.

2-8-2 Energy Consumption of Non-Linear CDC

The same notation and terms that were used for linear CDC are valid here also. Hence they are not repeated here. The additional terms $\alpha, \beta, \delta, \gamma$ are the coefficients of the non-linear CDC.

$$g_m = \frac{\alpha.C_x + \beta.C_x + \delta.C_{ref} + \gamma.C_{ref}}{\tau} = \frac{((\alpha + \beta)C_x + (\delta + \gamma)C_{ref}).K}{T_2}$$

The energy consumption during Φ_1 is

$$E_1 = ((\alpha+\beta)C_x + (\gamma+\delta)C_{ref})V_{ref}^2$$

The energy consumption during Φ_2 is

$$E_2 = T_2.V_{supply}.I_{OTA}$$
$$E_2 = T_2.V_{supply}.\frac{I_{OTA}}{g_m}.g_m$$
$$E_2 = ((\alpha+\beta)Cx + (\gamma+\delta)Cref).K.\frac{I_{OTA}}{g_m}.V_{supply}$$

The total energy consumption during a single clock phase is

$$E = E_1 + E_2$$
$$E = ((\alpha+\beta)C_x + (\gamma+\delta)C_{ref})V_{ref}^2 + ((\alpha+\beta)C_x + (\gamma+\delta)C_{ref}).K.\frac{I_{OTA}}{g_m}.V_{supply}$$
$$E = ((\alpha+\beta)C_x + (\gamma+\delta)C_{ref})V_{supply}^2(1 + K.\frac{I_{OTA}}{g_m}\frac{1}{V_{supply}}) \quad (2\text{-}28)$$

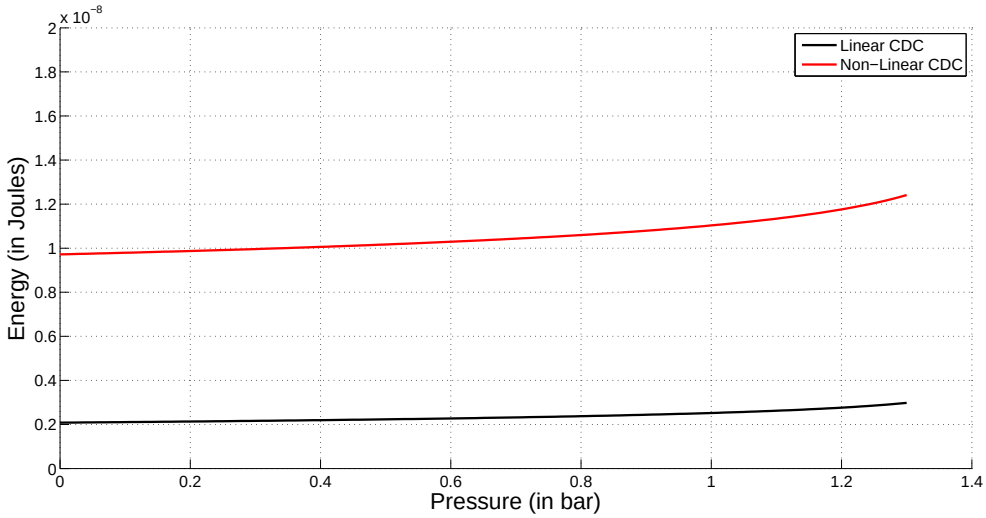


Figure 2-20: Energy Consumption of linear and non-linear CDC

Figure 2-20 compares the energy consumption of linear and non-linear CDC given by Eq. (2-27) and Eq. (2-28) respectively. As clearly seen from Figure 2-20, the energy consumption of the non-linear CDC is higher than the linear CDC.

We define a new FOM to compare different CDC architectures. Instead of just comparing the Energy of a given CDC, the FOM given in Eq. (2-29) takes into account of both Energy and the effect of thermal noise (by the term $\sigma_{Pressure}$). The FOM is given as follows.

$$FOM_{CDC} = energy.\sigma_{Pressure}^2 \quad (2\text{-}29)$$

The energy consumption of linear and non-linear CDC were given by Eq. (2-27) and Eq. (2-28) respectively. The uncertainty in Pressure ($\sigma_{Pressure}$) for both linear and non-linear CDC were given in Eq. (2-12). Thus from the equations above, the individual FOM of the CDC can be calculated. A given capacitor C will dissipate an energy of (E = C.V^2.N) over N clock cycles. We had defined the fundamental pressure uncertainty due to the effect of thermal noise on a capacitor C in Eq. (2-23). Then using Eq. (2-29), we can find the fundamental limit on FOM of a CDC. Figure 2-21 compares the FOM of linear, non-linear CDC and the fundamental limit for a CDC. It also concludes that the linear CDC is the most energy-efficient architecture. The fundamental limit is very low because it considers the energy consumption of a single capacitor alone, whereas for both the CDCs we have taken into account of the power consumption of the OTA also. This is the reason for the difference between the FOM of CDC and the fundamental limit. The following parameters were assumed in the MATLAB simulation. The supply voltage = 1.8V and the parameter $\frac{g_m}{I_d}$ was assumed to be around 20 (a reasonable assumption for transistor operation in weak-inversion).

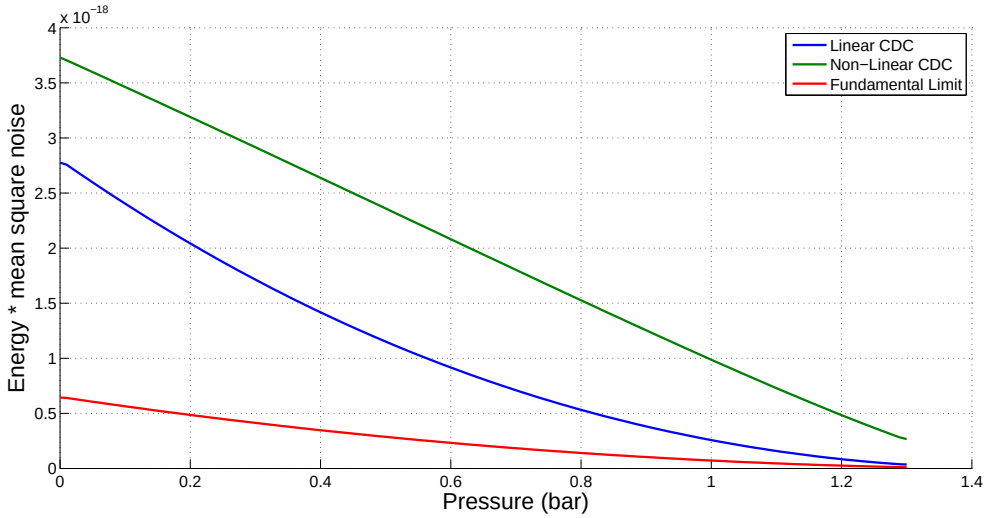


Figure 2-21: FOM for CDC

2-9 Choosing the Order of the Modulator - Quantization Noise

The analysis done until now illustrates the story of thermal noise and its impact on the CDC performance (energy consumption, pressure resolution etc.,). Now let's see the impact of quantization noise on the CDC performance. The motivation of the analysis is that, in case the non-linear CDC results in a lower order for the modulator compared to the linear CDC, then it will be a winner in terms of energy consumption (the modulator of the non-linear CDC will then require fewer OTAs).

2-9-1 Incremental ADC

The loop filter that we will implement will be representing an incremental $\Delta\Sigma$ ADC. The incremental ADC has a separate reset period to flush out the memory of the loop filter

between two measurements. The number of clock cycles that a ADC takes to achieve a particular resolution is denoted as N (Equivalent to OSR - Over Sampling Ratio in $\Delta\Sigma$ ADC). The Figure 2-22 shows the associated terminology of an incremental ADC. Detailed discussion of the incremental ADC can be found in [9], [6].

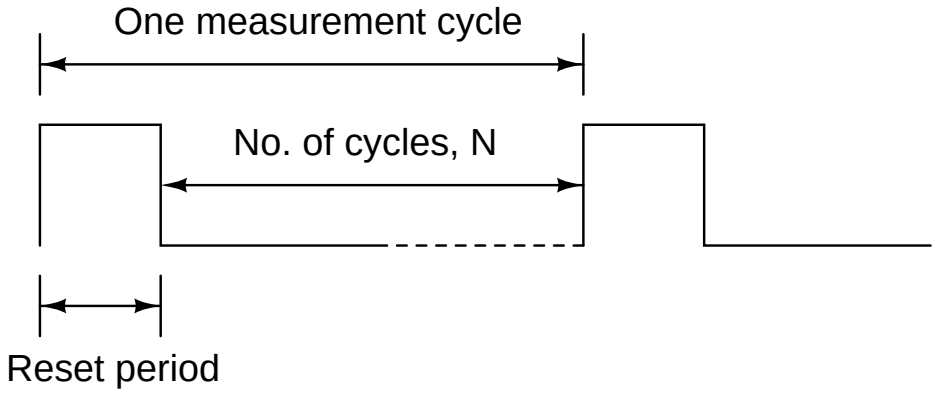


Figure 2-22: Basic terminology of an incremental ADC

From [9], the ENOB of an L^{th} order modulator can be given as follows

$$\begin{aligned} ENOB_{1^{st}orderModulator} &= log_2(N) \\ ENOB_{2^{nd}orderModulator} &= 2 * log_2(N) - 1.415 \\ ENOB_{3^{rd}orderModulator} &= 3 * log_2(N) - 6.601 \\ ENOB_{4^{th}orderModulator} &= 4 * log_2(N) - 14.102 \end{aligned}$$

The LSB of L^{th} order modulator can be written as

$$\Delta\mu = \frac{1}{2^{ENOB_{L^{th}orderModulator}}} \tag{2-30}$$

The quantization noise is then given as

$$\Delta P = \Delta\mu(\frac{\partial P}{\partial \mu}) \tag{2-31}$$

The term ΔP represents the input referred noise quantity. There are several degrees of freedom in ΔP like the number of Cycles 'N', order of the modulator etc., In the following comparison we will restrict ourselves to the pressure value of 1 bar and compare the performance of the linear and non-linear CDC across various order of the modulator. Thus in Eq. (2-31), the term $\Delta\mu$ is a function of the number of cycles. The slope value $(\frac{\partial P}{\partial \mu})$ corresponds to a pressure value of 1 bar.

In the Figure 2-23, we see the comparison of the noise performance of the two CDC as a function of the number of cycles 'N'. As we saw in the noise analysis in previous sections, the non-linear CDC has more thermal noise compared to that of the linear CDC. Usually, these kinds of curve are plotted as a function of N versus ENOB. In our case, since it is a pressure sensing application we plot the graph of Pressure resolution versus N. The optimum order for the modulator is chosen by the following method. The thermal noise should be lower than

the required pressure resolution and for the system to be energy-efficient the thermal noise of the system should be dominant compared to the quantization noise. Using these guidelines, we refer to Figure 2-24 and Figure 2-25, for choosing the order of the modulator. And we infer from these figures that the optimum order of the modulator for both linear CDC and non-linear CDC is 3. Thus in terms of both the thermal noise and quantization noise analysis, we can conclude that the CDC that is most energy-efficient is the linear CDC. Hence we will proceed on to implement the linear CDC in this research work.

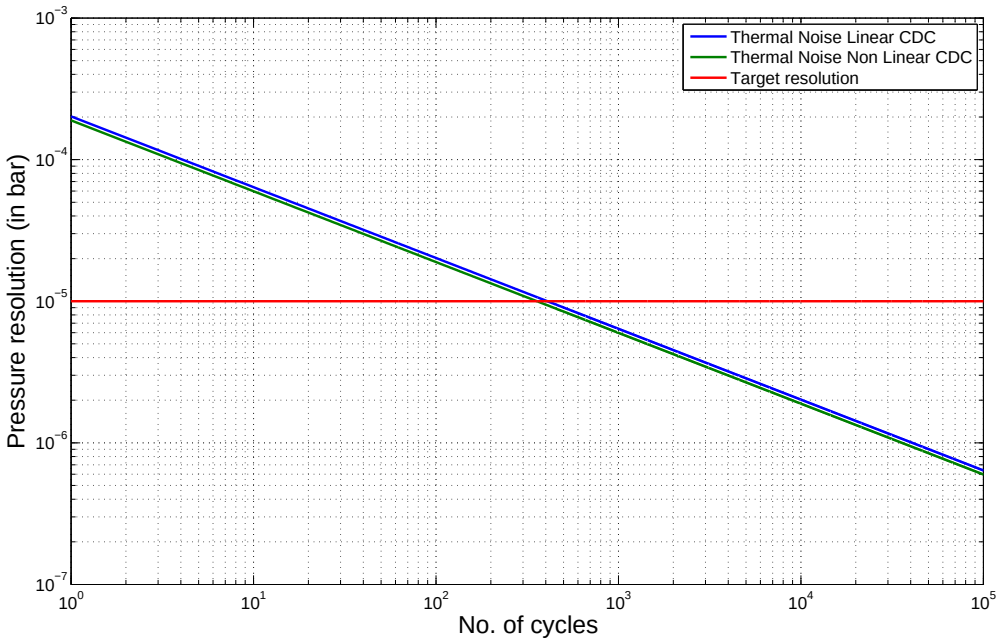


Figure 2-23: Thermal noise comparison of the two CDC

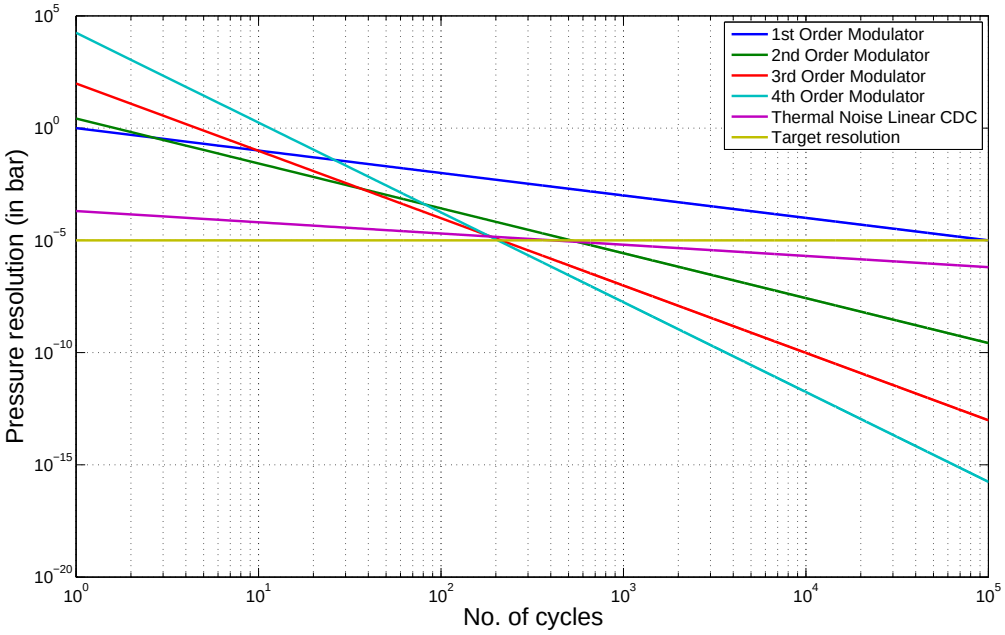


Figure 2-24: Performance of linear CDC

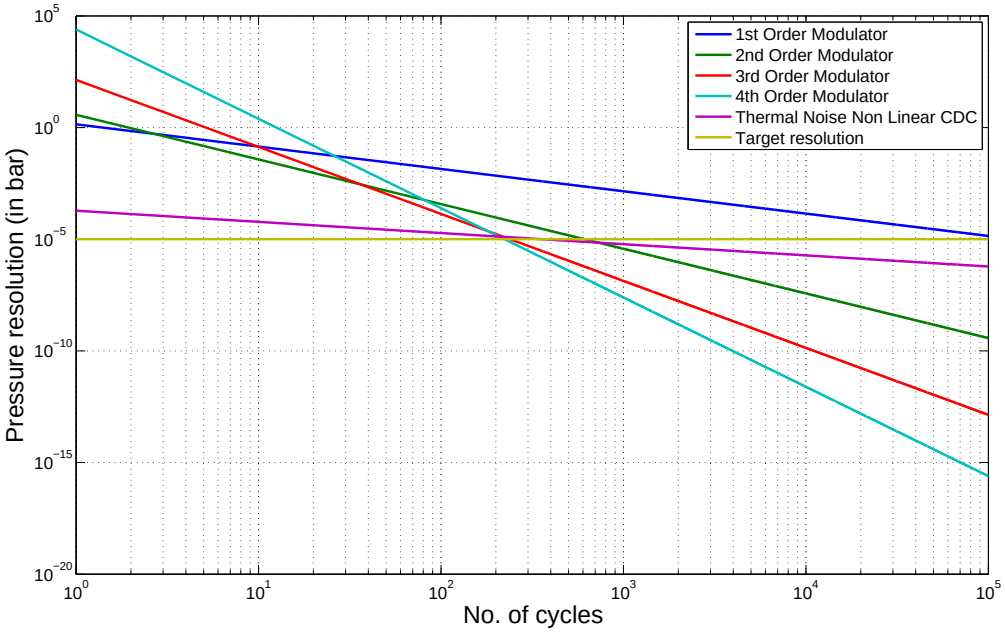


Figure 2-25: Performance of non-linear CDC

2-10 System Level Implementation

The system level implementation of the Loop filter is shown in Figure 2-26. The 3^{rd} order structure was chosen based on noise and energy-efficiency analysis. The CIFF (Cascade of Integrators with Feed-forward structure) architecture is chosen to reduce the swing at the output of the integrators [10]. The direct feed-forward path from input to the summing node is not present in our design because it would involve replicating the sensor capacitance for implementation of that feed-forward path [3]. The coefficients B, C1 and C2 represent the gain of the integrator and the coefficients A1, A2 and A3 represent the feed-forward coefficients.

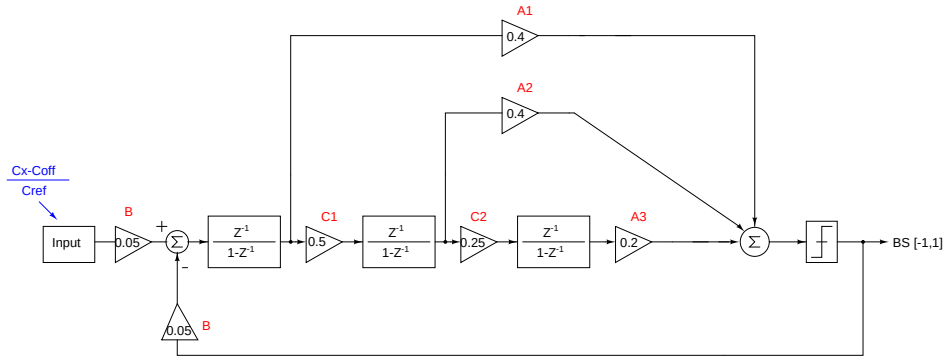


Figure 2-26: System level implementation of the Loop Filter

Figure 2-27 shows the quantization error plot in relation to a resolution 16 bits (The range of pressure that we require to measure is 0 - 1.3 bar and the pressure resolution is 1e-5 bar, from these input we obtain a resolution of around 16 bits). The maximum full-scale range for a 3^{rd} order modulator is $\pm 0.67 \times input$ [9]. For the chosen coefficients, the CDC achieves 16 bit accuracy in 130 clock cycles (N = 130). The Figure 2-27 shows clearly the quantization error to be limited between $\pm$ 0.5 LSB for the chosen value of 'N '. The CoI (Cascade of Integrators) structure was used as the decimation filter to obtain the digital output. The different type of decimation filter and their impact on performance of the ADC is discussed in detail in [6, 9]. The swing at the output of the integrators is shown in Figure 2-28. The output swing of the integrators is less than 200mV for the entire input range.

A simplified (single-ended) system-level implementation of the CDC is shown in Figure 2-29. The coefficients of the modulator along with their relation to the capacitor ratios is also given in the figure.

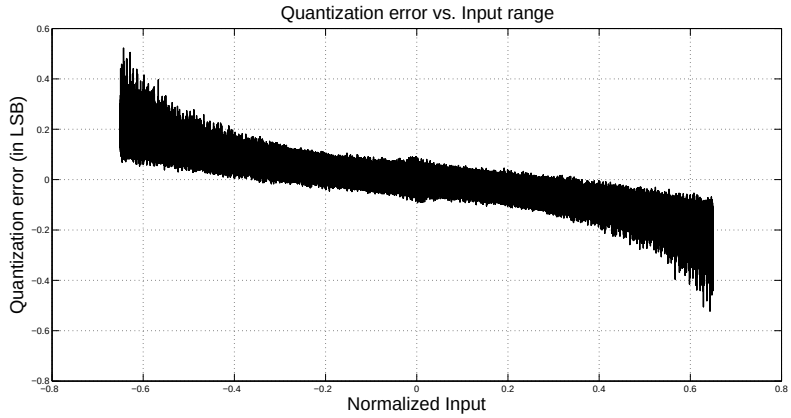


Figure 2-27: Quantization error versus normalized input range (16-bit, 130 cycles)

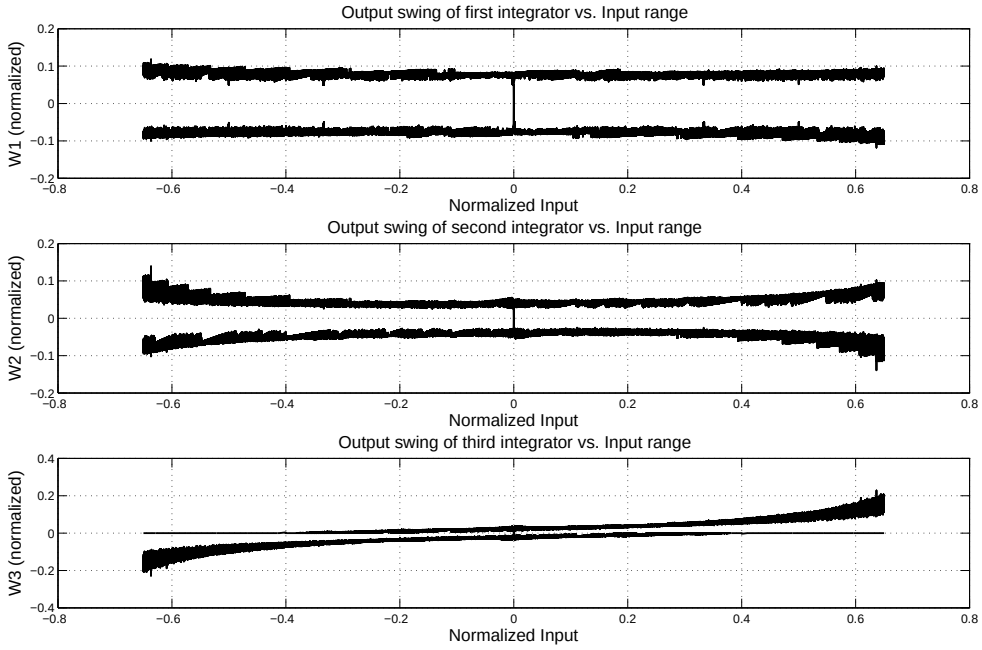
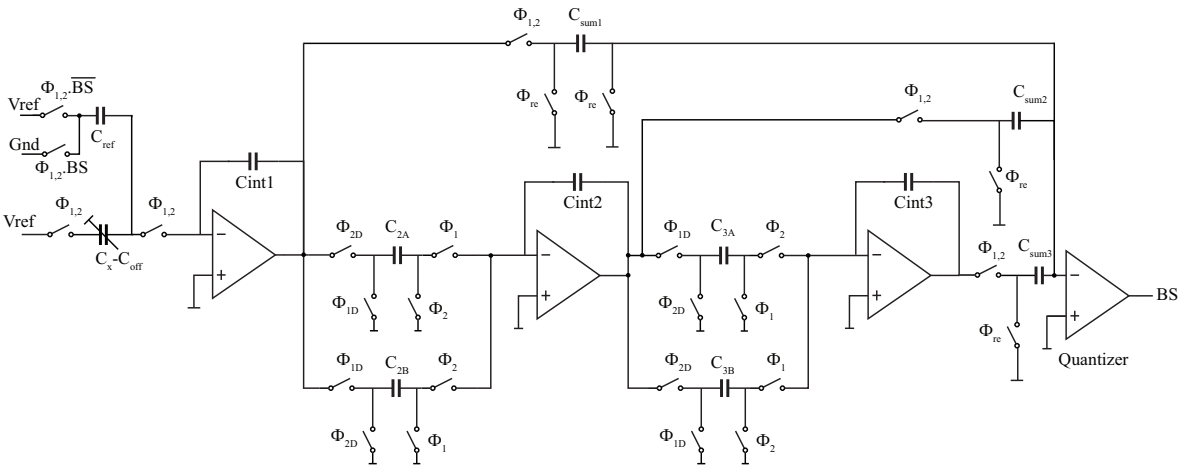


Figure 2-28: output swing of the integrators of Loop Filter versus normalized input



$$B = \frac{C_{ref}*V_{ref}}{C_{int1}} = \frac{200fF}{4pF} = 0.05$$

$$C1 = \frac{C_{2A,B}}{C_{int2}} = \frac{216fF}{2*216fF} = 0.5 \quad / \quad C2 = \frac{C_{3A,B}}{C_{int3}} = \frac{110fF}{4*110fF} = 0.25$$

$$A1 = \frac{C_{sum1}}{\Sigma C_{sum}} = \frac{2*110fF}{5*110fF} = 0.4 \Big/ A2 = \frac{C_{sum2}}{\Sigma C_{sum}} = \frac{2*110fF}{5*110fF} = 0.4 \Big/ A3 = \frac{C_{sum3}}{\Sigma C_{sum}} = \frac{1*110fF}{5*110fF} = 0.2$$

Figure 2-29: Simplified circuit implementation of the Loop Filter

Chapter 3

Implementation of the Linear CDC

In this chapter, we propose design techniques that are used improve the performance of the current design over the existing state-of-the-art CDC [3]. Then we will discuss the implementation of various circuit blocks.

3-1 Design Technique I - Inverter-Based OTA

The first design technique that is implemented is the novel inverter-based OTA. Before directly showing the structure, we briefly introduce inverter-based circuits and show their evolution over the years. Then we will discuss various inverter-based circuits from the open literature.

3-1-1 Motivation

The merits of inverter-based circuits are as follows:

- Figure 3-1 compares the different commonly used OTA structures versus an inverter-based OTA. The telescopic OTA, has two branches (2 × I) to provide $G_{m,eff}$ (the trans-conductance of the entire OTA) = g_m. The folded-cascode OTA, has four branches (4 × I) to provide the trans-conductance $G_{m,eff} = g_m$. The inverter-based OTA, has two branches (2 × $\frac{I}{2}$) to provide the transconductance $G_{m,eff} = g_{m,N} + g_{m,P} = 2 \times g_m$ (assuming the transconductance of PMOS and NMOS are equal) [3]. Thus we can clearly see that the inverter-based OTA achieves the highest possible transconductance for a given supply current. In other words, the $\frac{g_m}{I_d}$ of an inverter-based OTA is very high ($\frac{g_m}{I_d}$ is also a commonly used design metric to characterize a single transistor in a technology).

- The slew rate of an OTA structure is proportional to its GBW [11], hence the inverter-based OTA has better slew rate compared to other OTA structures.

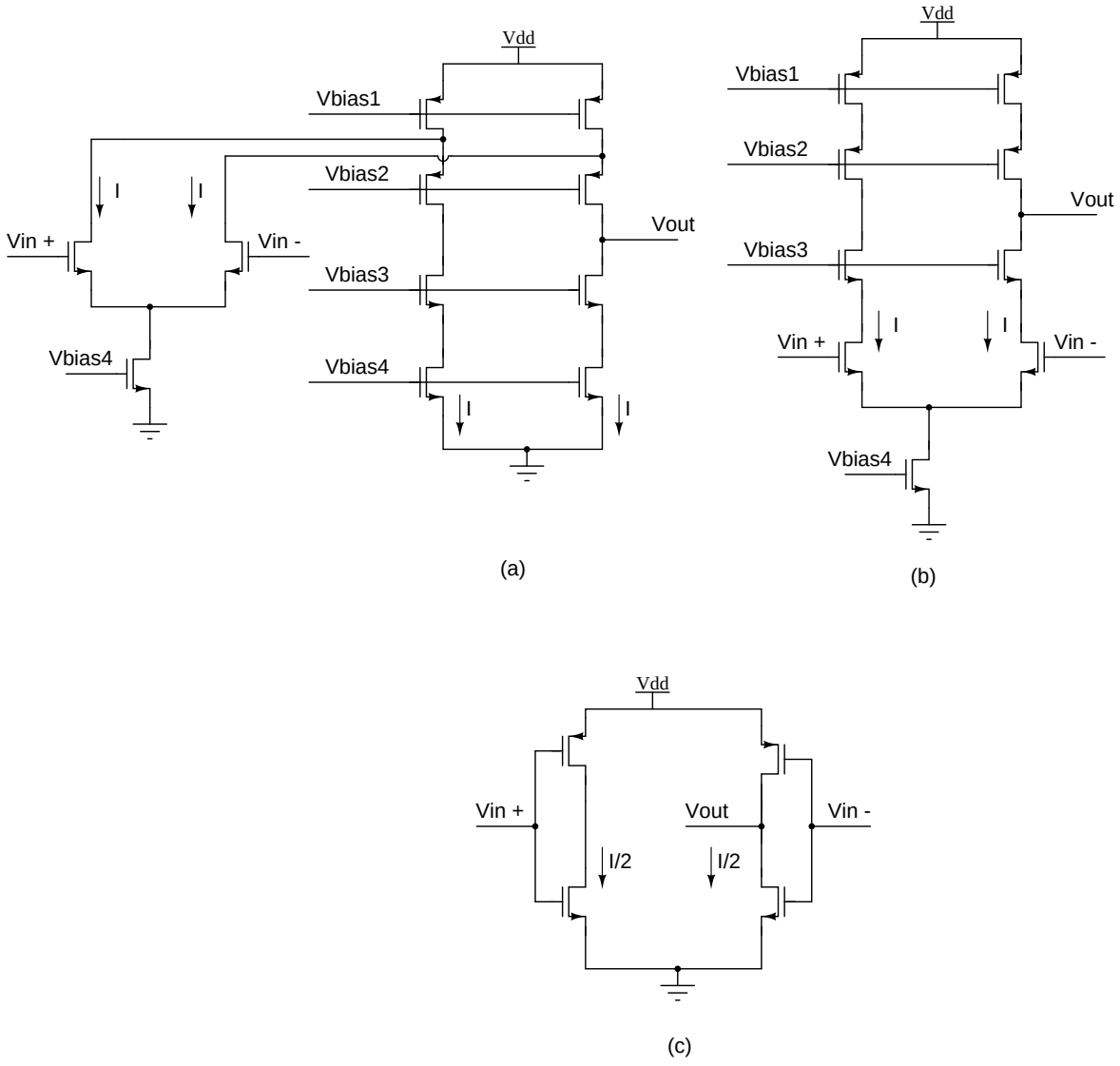


Figure 3-1: (a) Folded-Cascode OTA, (b) Telescopic OTA and (c) Inverter-based OTA

Based on the above discussion, we can say with confidence that inverter-based OTA structures are vital building blocks for an energy-efficient system. The earlier OTA designs concentrated mainly on normal cascoding or active-cascoding [12] of transistors to achieve the required DC gain. The inverter-based circuits have been investigated right from 1980's [13], but they have received great attention in recent years because of the very low supply voltage ($\leq 1.8V$) in today's technology. One of the first and most prominent work that used inverter-based structures to implement a system (analog filters) was [14]. In recent years, high resolution ADCs were implemented using inverter-based structures and achieved the state-of-the-art performance in terms of their FOM [15]. A brief discussion on different flavours of inverter-based OTA available in open literature is given below. The article [16] demonstrates an inverter-based self-biased OTA structure. This structure is relatively simple but is suited only for application in which single ended output is required. A nice OTA structure that retains the inverter-based circuit but provides a differential output was proposed in [17]. The highlight of this circuit is that it has Class AB biasing. Class A biasing of an inverter-based OTA structure with a switched-capacitor CMFB circuit and continous time CMFB circuit were demonstrated in recent publications [18, 19] respectively.

3-1-2 Evolution of Inverter-Based OTA Structure

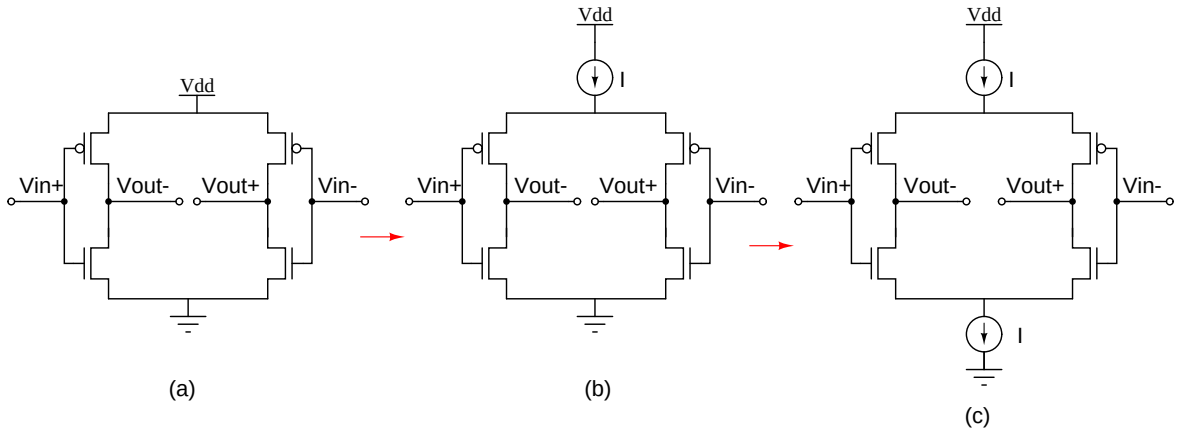


Figure 3-2: Evolution of inverter-based OTA (a) Simple Inverter-Based OTA, (b) Current-Starved Inverter-Based OTA and (c) Floating Inverter-Based OTA

The inverter-based OTAs have evolved over the time as illustrated in Figure 3-2. The simple inverter-based OTA [15] is shown in Figure 3-2 (a). The Transconductance of the OTA is highly influenced by the Process, Supply voltage and Temperature (PVT) variations. The OTA structure has also a very poor AC PSRR compared to other conventional OTA structures. The OTA structure shown in Figure 3-2 (b) is referred to as the 'current-starved inverter-based' OTA. The current source of the OTA helps in improving the AC PSRR and the DC operating point is more well-defined in this OTA compared to the OTA in Figure 3-2 (a). The OTA structure shown in Figure 3-2 (c) is the simplified OTA structure that is implemented in this research work. Since the two current sources are present at the top and bottom of the OTA, the OTA is isolated from the supply rails. The OTA is referred to as 'floating inverter-based' OTA structure. This OTA structure has better AC PSRR from both the supply rails and it doesn't require a capacitive level-shift (C_C in Figure 3-3) at its input,

which is typically used in the other inverter-based OTAs (in combination with auto-zeroing) to be able to freely define the input voltage.

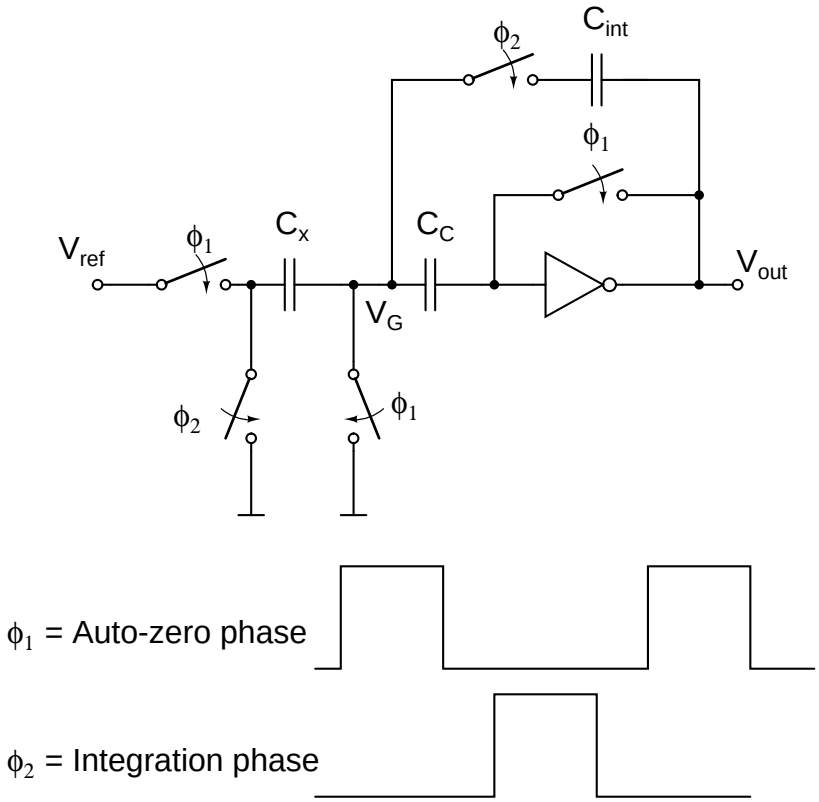


Figure 3-3: Schematic of the current-starved inverter-based OTA [3]

The floating inverter-based OTA is a significant design step. In case of the current-starved inverter-based OTA, the input signal is processed only during one half of the clock cycle the other half has to be dedicated for auto-zeroing. The schematic of the current-starved inverter-based switched-capacitor integrator is shown in Figure 3-3. The current-starved inverter-based OTA based architecture has more thermal noise voltage introduced due to the presence of the auto-zeroing capacitor C_C. Since this capacitor is removed in our architecture, it can be expected to be less noisy compared to the previous architecture [3]. The complete schematic of the 'floating inverter-based' OTA is shown in Figure 3-4. The cascoding devices are present to improve the DC gain of the OTA. The CMFB transistors operate in linear region and help in defining the DC potential at the output nodes of the OTA [20]. The rest of the transistors in the schematic operate in weak inversion. This OTA structure is similar to the OTA structure published independently in [19].

3-2 Design Technique II - Double Sampling

The second design technique that we have used in this work is double sampling. Figure 3-5 shows the comparison between a single sampling SC (Switched-Capacitor) integrator and a double sampling SC integrator. Let us briefly look at the operation of the single sampled

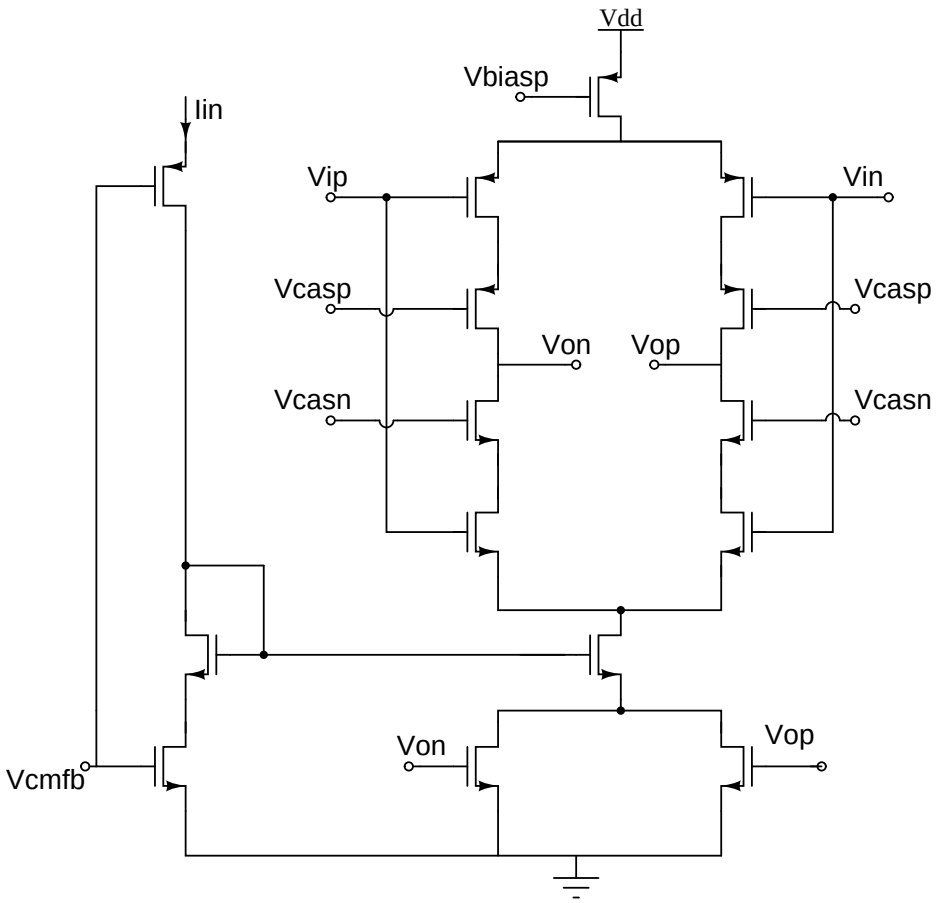


Figure 3-4: Floating inverter-based OTA

structure and understand its pros and cons. During the clock phase (ϕ_1) the input capacitor C_s stores the charge $C_s.V_{in}$ across it. During the clock phase (ϕ_2) C_s dumps the stored charge on the integration capacitor C_{int}. We can clearly observe that during the clock phase (ϕ_1), the integrator remains idle and burns static power. In case of a double sampling scheme, we introduce another SC branch as shown in Figure 3-5 (b). Thus when the capacitor C_{s1} samples the input signal during ϕ_1, the capacitor C_{s2} dumps the charge (that was stored from the previous half-cycle) upon the integration capacitor and vice-versa. By using double sampling, we have effectively doubled the sampling rate (in turn increasing the resolution of the ADC). This is an extremely useful property that can be exploited in energy-efficient circuits.

The beauty of the circuit is that it doesn't place any extra loading requirements on the OTA, thus the power and driving capability of the OTA in case of single-sampling and double-sampling remains the same.

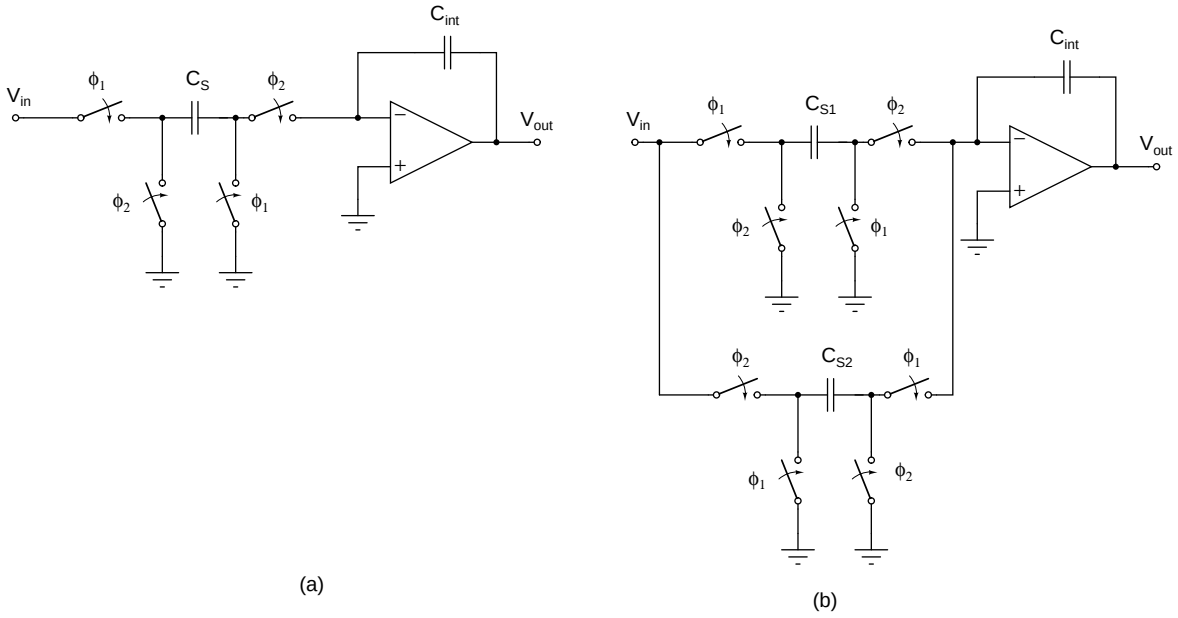


Figure 3-5: Comparison of (a) Single sampling integrator and (b) Double sampling integrator

The double sampling technique has a disadvantage. It is quite crucial for understanding this issue. The method used to alleviate the problem is explained later. The input-output relation of the double sampled OTA shown in Figure 3-5, is given by Eq. (3-1) [21].

$$V_{out}[n] = V_{out}[n-1] + \frac{C_S}{C_{int}}.V_{in}[n-1] + \frac{-1^n.\Delta C_S}{2.C_{int}}.V_{in}[n-1] \tag{3-1}$$

Where $C_S = \frac{C_{S1}+C_{S2}}{2}$ and $\Delta C_S = C_{S1} - C_{S2}$ is the term that arises due to the mismatch between C_{S1} and C_{S2} (ideally $C_{S1} = C_{S2}$). The problem is due to the -1^n term which can be represented mathematically as $-1^n = Cos(2\pi(\frac{f_s}{2})nT)$. This is a sampled cosine waveform with a frequency of $\frac{f_s}{2}$. Pictorially, -1^n is just a waveform that has positive peak (for even value of n) and negative peak (for odd value of n). This mismatch term is fed as an input

to the input of the loop filter along with the actual input. Now, the input to the loop filter also comes from the quantizer whose quantization noise peaks at $\frac{f_s}{2}$. The input from the quantizer and the mismatch term gets mixed and the resultant DC term gets aliased back into the baseband and it increases the noise floor. The SNR starts dropping down and the severity of the SNR loss depends on matching of the capacitors($\frac{\Delta C_S}{C_S}$).

There are several design techniques to avoid this aliasing back of the noise to the baseband [21, 22]. We have implemented the following technique [23]. In the frontend of the CDC instead of explicitly using two branches for every differential input arm, we run the SC circuit at twice the clock frequency. This is achieved by applying the input to the OTA using a single SC branch that is ON during both phase ϕ_1 and ϕ_2. The advantage of doing this is that we have only one capacitor instead of two and there is no matching requirement. For proper operation of the circuit, an additional clock pulse called ϕ_{re} is required [23]. The memory (state) of the input capacitor is cleared during the non-overlapping period called as ϕ_{re}, so that there is no correlation between the input during phase ϕ_1 and ϕ_2. The implementation of double sampling in the CDC is shown in Figure 3-6 and the corresponding timing diagram is shown in Figure 3-7.

Another advantage of running the SC branch at twice the clock frequency is saving significant chip area. In case the double sampling is implemented as shown in Figure 3-5, then there will be two SC branches per differential arm. Hence there will be a total of 4 capacitors that are required in the front-end of the CDC. The 4 capacitors are the sensor capacitors and unlike the CMOS capacitors, these MEMS structures occupy very huge area. Thus by running the front-end of the CDC at twice the clock frequency we manage to achieve the same functionality with just 2 sensor capacitors (which results in huge savings in the chip area). Apart from the SC branches in the front-end of the CDC, the rest of the SC branches can be implemented using the regular double-sampling structure, which is also illustrated in Figure 3-6. This is because: (1) in rest of the SC branches there will be no mixing of quantizer signal and (2) the rest of the capacitors in the CDC are ordinary fringe capacitors and do not occupy much area.

The reference voltage V_{ref} is equal to the supply voltage. In the previous designs, the voltage that was given to the node V_{ref} was less than the supply voltage [3]. We have connected it to the supply voltage to increase the signal charge that gets dumped into the loop filter. This will help in improving the FOM of our system. In Figure 3-6, the voltage V_{mid} sits in the middle of the supply voltage. If the V_{cm} (common-mode signal = 0.6V) is given over here, then it will result in injection of a common-mode signal when the supply is varied. Figure 3-8 shows the schematic of the Mid-supply voltage generator. It is basically a switched-capacitor attenuator/divider. The capacitors C1, C2 (both 100fF) is used for generating $\frac{Vdd}{2}$. The capacitors C3, C4 (both 1pF) act as charge reservoirs which supplies the transient load current.

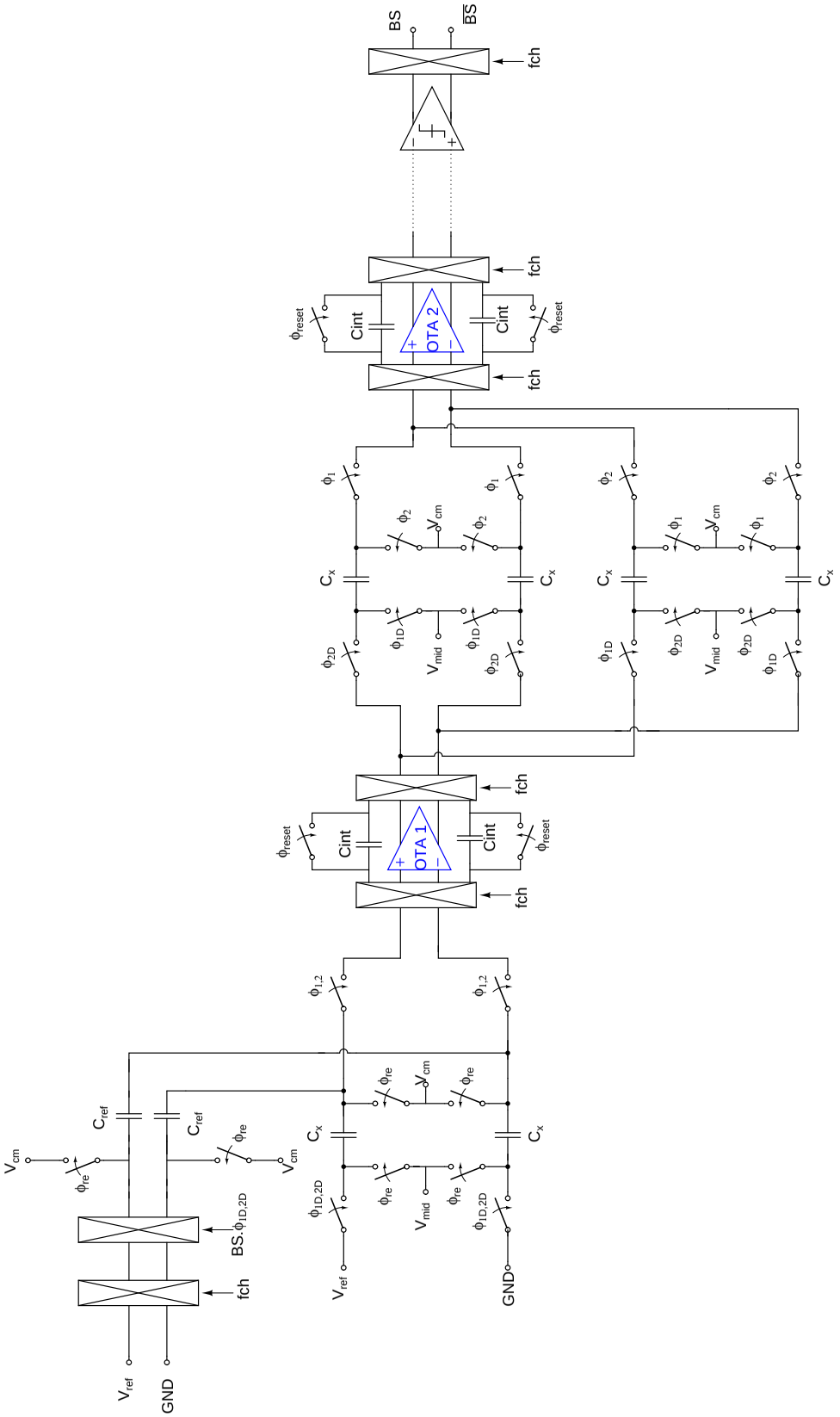


Figure 3-6: Implementation of double sampling and system Level chopping

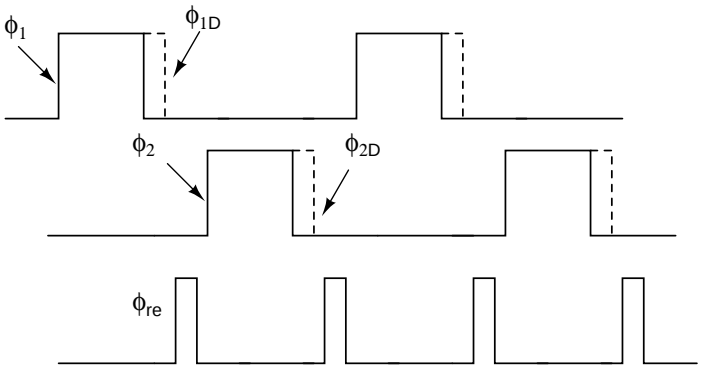


Figure 3-7: Timing diagram for double sampling

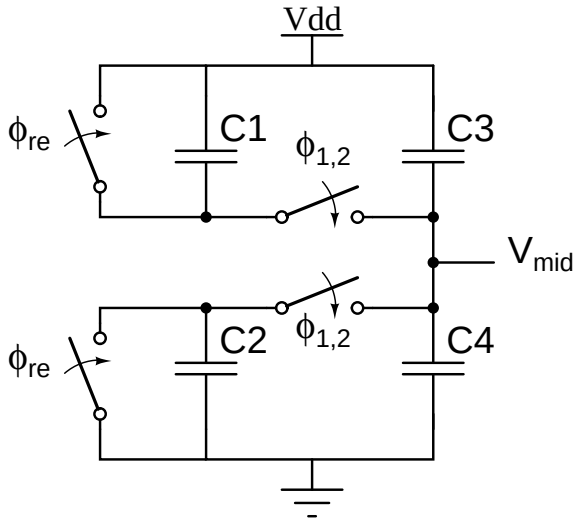


Figure 3-8: Mid-supply voltage generator

There are some interesting points to be noted due to the implementation of double-sampling.

- The floating inverter-based OTA structure is excellently suited for the implementation of double sampling. The other inverter-based OTA structures require auto-zeroing and it is less suitable to implement double-sampling using them.
- Due to the implementation of the double-sampling, we can obtain the required resolution in half the measurement time compared to [2]. Thus we have effectively increased the performance of our CDC 2X times better (in terms of the FOM) compared to the existing state-of-the-art CDC [2].

3-3 Design Technique III - System - Level Chopping

In the previous implementation of the CDC [2], the bottleneck for the performance was the phenomenon of charge-injection. The charge balancing architecture (through the presence of negative feedback), can eliminate multiplicative errors (like $\frac{1}{f}$ noise). However the charge-injection is an additive error and cannot be eliminated. The issue is represented in the input-output relation of CDC as shown in Eq. (3-2).

$$\mu = \frac{C_x - C_{off} + C_{ref} \pm \frac{Q_{inj}}{V_{ref}}}{2C_{ref}} \tag{3-2}$$

where Q_{inj} represents the charge-injection. To eliminate the charge-injection error, system-level auto-zeroing was previously implemented [2]. This involves taking two measurements (one with the sensor capacitance connected and the other without the sensor capacitance). The two measurements will have approximately the same error due to charge-injection and subtracting the two measurements will eliminate the error. The disadvantage is that for obtaining a single reading the conversion time is doubled. This is overcome in our CDC by implementing system-level chopping [6]. The implementation of the system-level chopping in the CDC is shown in Figure 3-6. To obtain the digital output, the decimation filter has to be a SINC filter to eliminate the chopper ripple.

The advantage of the system-level chopping in our system is as follows:

- Using system-level chopping we can obtain the digital output of the CDC in half the measurement time (when compared to system-level auto-zeroing). Thus, we have effectively increased the performance of our CDC 2X times better (in terms of the FOM) compared to the existing state-of-the-art CDC [2].
- In summary, by use of the proposed design techniques in our CDC, we can achieve 4X times (2X - due to double sampling, 2X- due to system-level chopping) better performance compared to the state-of-the-art [2].

3-4 Circuit Implementation

In this section, we will briefly discuss the implementation of various circuits blocks.

3-4-1 Bias Generator

Figure 3-9 shows the biasing circuit block. A constant- g_m bias circuit [24] was designed which provides the master bias, from which the required biasing currents are derived. Voltages V_{BIASP}, $V_{BIASN}$and V_{cm} represent the biasing voltages of PMOS, NMOS and the common-mode voltage respectively. Since our design has to work from 1.2V - 1.8V, all the bias voltages are referenced to ground (so that they remain constant irrespective of the supply voltage).

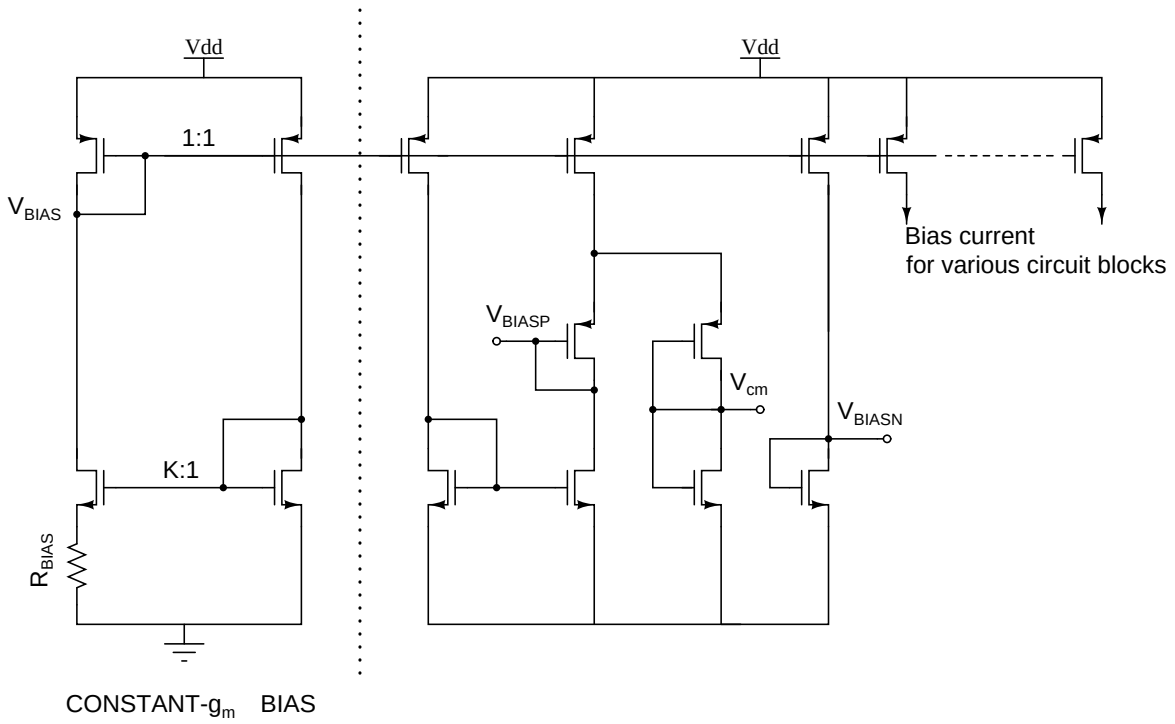


Figure 3-9: Schematic of Bias Generator

3-4-2 Clock Booster

The minimum supply voltage is around 1.2V and the common-mode voltage is 600mV (which is close to the threshold voltage of our technology). Thus the switches will have very high resistance (due to very low gate overdrive voltage), if the supply voltage is directly given. To reduce the switch resistance and to properly turn ON all the switches we use a clock booster. It is to be noted that all the switches in our design are normal NMOS transistors (no special technology layers are used). Figure 3-10 shows the implementation of the single ended input/output clock booster [25]. The capacitors C1,C2 are implemented using fringe capacitors. The two capacitors need not be equal. The sizing of capacitor C2 depends on the total gate capacitance present at the output node of the clock booster and the layout parasitic. Hence it is generally advisable to size C2 after an rough estimate of the layout parasitic. The size of C1 is relatively small because it drives the gate of only one NMOS transistor. In our design, C1 and C2 were chosen as 30fF and 210fF respectively. Figure 3-11

shows the double input clock booster. This block is used to boost the non-overlapping clocks like ϕ_1, ϕ_2. The capacitors C1 and C2 in this design were both chosen to be 100fF.

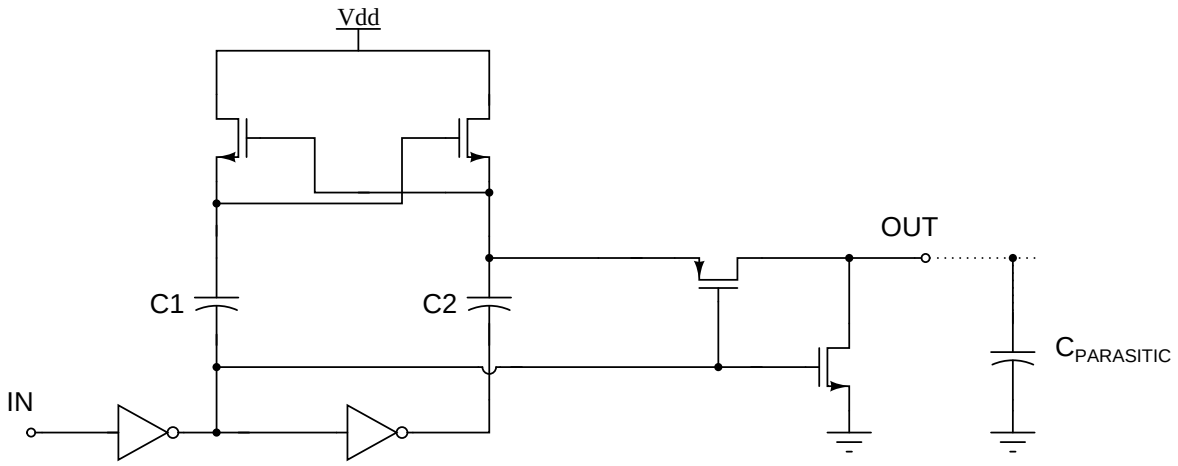


Figure 3-10: Schematic of single input Clock Booster [26]

3-4-3 Offset Capacitor

Figure 3-12 shows the schematic of the offset capacitor bank. It is a binary-weighted capacitor array whose unit capacitor value is 100fF. And it is tunable from 3.1pF to 100fF. This tunable property is extremely useful for compensating a wide range of baseline capacitance (that can vary due to process variation, due to fabrication of external or on-chip sensor capacitor). The required value of C_{off} is chosen by the serial in / parallel out shift register. The reference capacitor in our design is fixed to 200fF. Thus the CDC can measure a full-scale range of 400fF (Since a third order modulator is used the actual measurement range will be around 67% of 400fF).

3-4-4 Serial In / Parallel Out Shift Register

The serial in / parallel out shift register is used to provide the required control signals for various circuit blocks. The implementation of which is same as that of the standard IC available in market (example: IC 74AHC594 from NXP). It provides control signals for the offset capacitor bank, choosing an external or on-chip bias current and monitoring of the output of integrators.

3-4-5 Clock Generator

The generation of non-overlapping clock phases (ϕ_1, ϕ_2) and their delayed versions (ϕ_{1D}, ϕ_{2D}) for bottom plate sampling is well established [6, 3]. The signal ϕ_{re} is generated by making minor changes in the non-overlapping clock generator. The major task is to design the delay block that defines the pulse width of ϕ_{re}. The clock period for our design is 5μs. The width of the ϕ_{re} is designed to be around 300ns. This delay is generated using a programmable delay

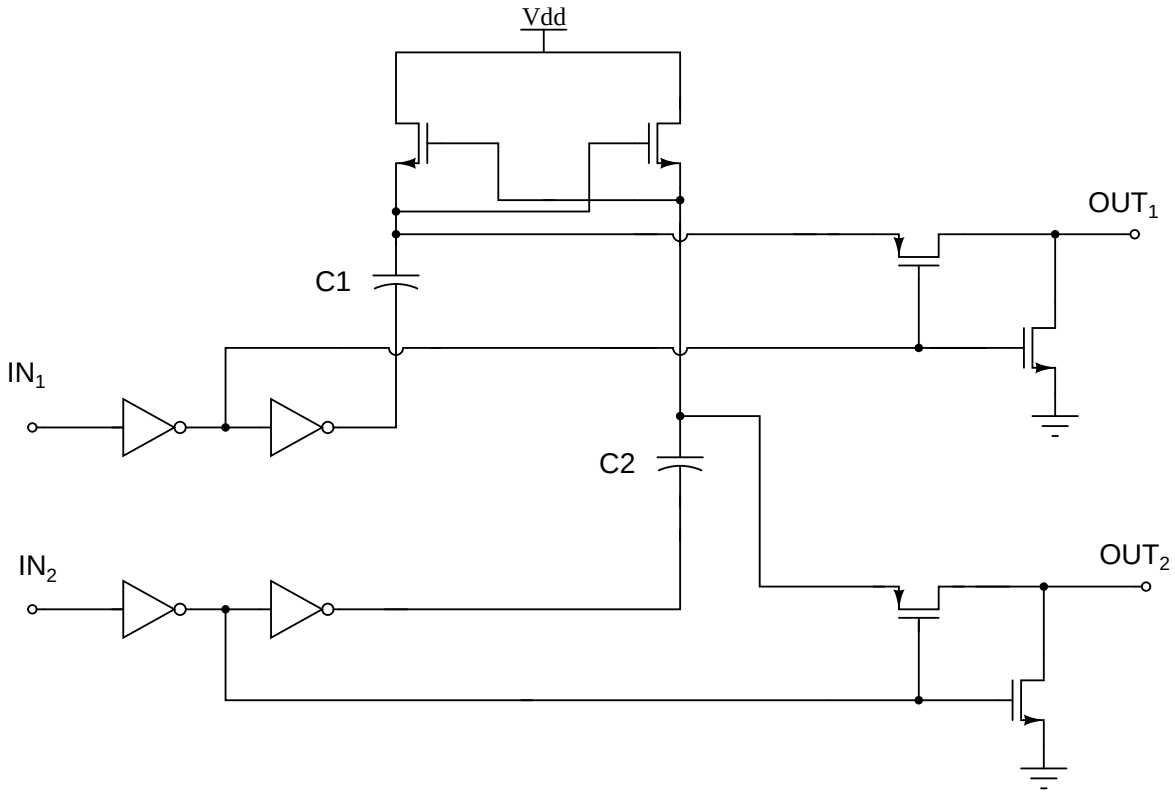


Figure 3-11: Schematic of double input Clock Booster [26]

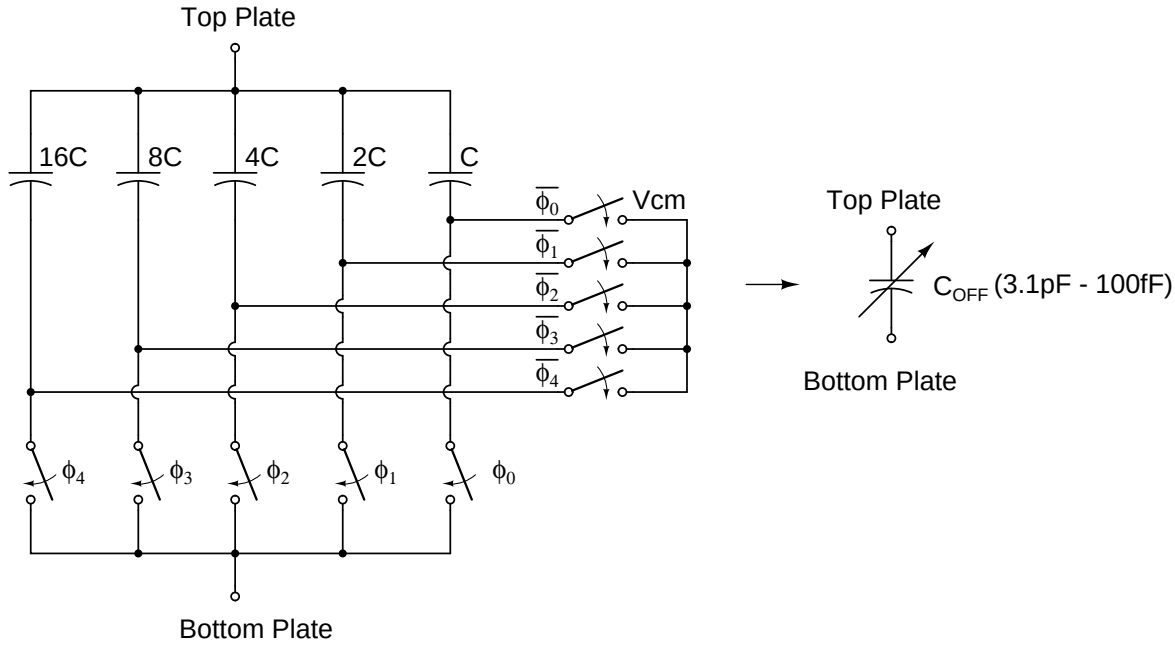


Figure 3-12: Schematic of the Offset capacitor bank

generator as shown in Figure 3-13. An external bias current is provided to the current starved inverters. By tuning the current we can control the rise and fall time of the inverter, when this signal is passed through the Schmitt trigger, we get a well-defined delay. The capacitors C1, C2 are just load capacitors whose presence helps in increasing the delay of the block (by loading the inverter). The schematic of the Schmitt trigger is also provided in Figure 3-13 [24].

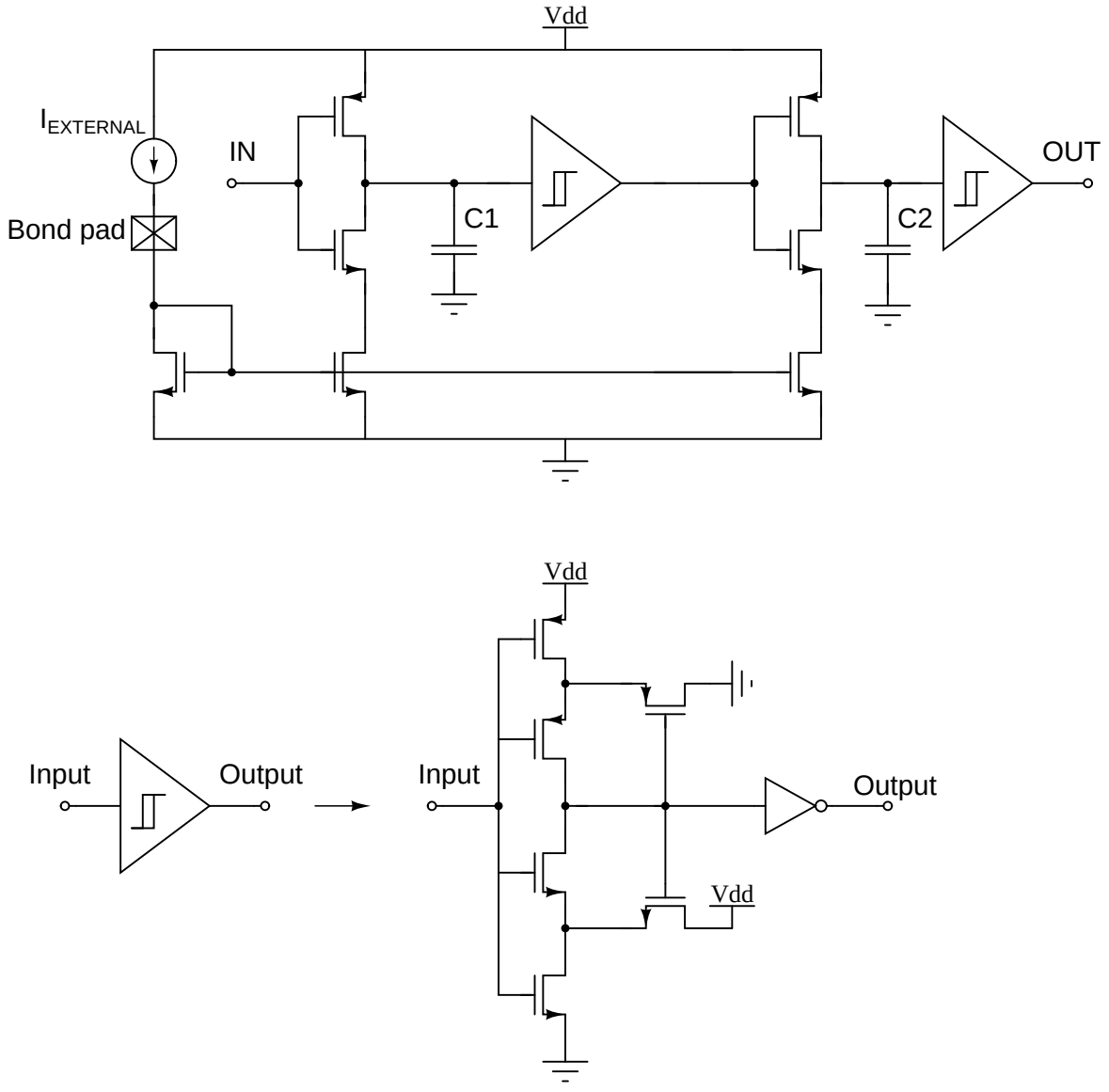


Figure 3-13: Programmable Delay generator

3-4-6 Comparator

Figure 3-14 shows the schematic of the comparator. This is a standard implementation of a comparator [3, 6]. The first stage of the comparator is the pre-amplifier. It is a low-gain

(diode-connected load), high-speed stage. It serves to provide sufficient amplification for the latch stage and it prevents any kick-back noise passing from latch stage to the passive summation node. The second stage is the track and latch stage. The decision of the comparator is taken when the signal ϕ_{EVAL} becomes low. The last stage is just a latch stage that is used for generating a rail-rail output. The delay of the comparator was measured to be around 65ns.

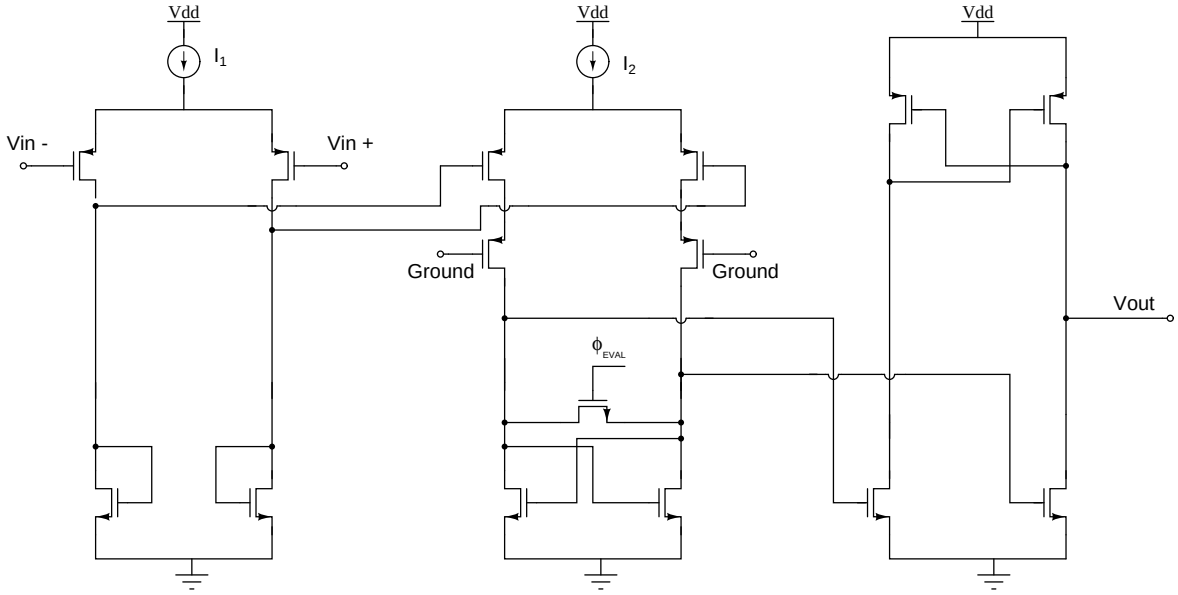


Figure 3-14: Schematic of Comparator

Chapter 4

Simulation Results

The architecture and systematic analysis of the CDC have been introduced in previous chapters, followed by the implementation details of various circuit blocks of the CDC. In this chapter, we will discuss the simulation results of the CDC in detail.

4-1 OTA Simulation Results

The floating inverter-based OTA was introduced in the previous chapter. Now we will discuss the simulation results of the OTA. A leaky integrator was modelled in MATLAB. The MATLAB simulation of the incremental $\Delta\Sigma$ ADC showed that to achieve the 16 bit accuracy, the OTA gain must be higher than 70dB. The output swing of the OTA in MATLAB simulation was shown to be less than $\pm$ 100mV.

Figure 4-1 shows the plot of DC gain of the OTA versus its output swing with VDD = 1.2V. The DC gain of the OTA was simulated to be around 77dB even when the supply voltage of the OTA was swept from 1.2V - 1.8V, thanks to the floating inverter-based OTA structure, which isolates the OTA from the supply rails by the current mirror.

Given a set of loading conditions, settling time etc., the transconductance (g_m) of the OTA can be calculated using the following equation [3], which can be derived from the model shown in Figure 4-2:

$$g_m = 2.ln(2.\frac{(m+1)}{T_{CLK}}(C_{in} + C_L + \frac{C_{in}C_L}{C_{int}})) \tag{4-1}$$

where m is the required accuracy in bits, T_{CLK} is the Clock period (m = 16bit, $T_{CLK} = 5\mu$s was given) and C_{in}, C_{int}, C_L are the input capacitor, integration capacitor and load capacitor respectively. The designed value of g_m of the OTA and their current consumption for VDD =1.2V is given in Table 4-1.

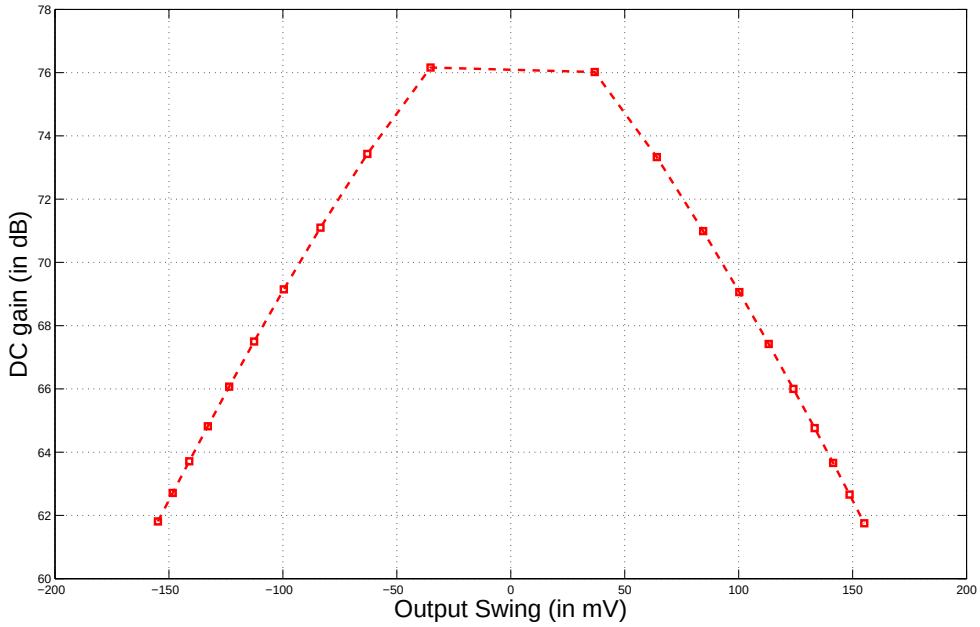


Figure 4-1: DC gain versus Output swing of the OTA

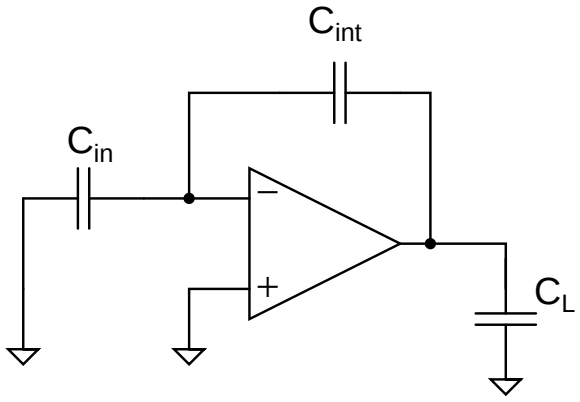


Figure 4-2: Circuit model of the integrator [3]

	Designed value of g_m	**Current consumption**
1^{st} integrator	19μS	0.653μA
2^{nd} integrator	5μS	0.186μA
3^{rd} integrator	2.3μS	93nA

Table 4-1: Simulation results of the OTA

4-2 Layout of the CDC

The layout of the complete CDC is shown in Figure 4-3. The chip occupies an area of about 892μm by 1196μm (including the bondpad and die-seal ring). The various numbers in Figure 4-3 indicates the location of a particular block. The whole chip is covered in Metal 5 (not shown in the figure) which acts as the shielding plate. It prevents the electrical interference generated by the circuit from reaching the sensor (which sits on top of the chip).

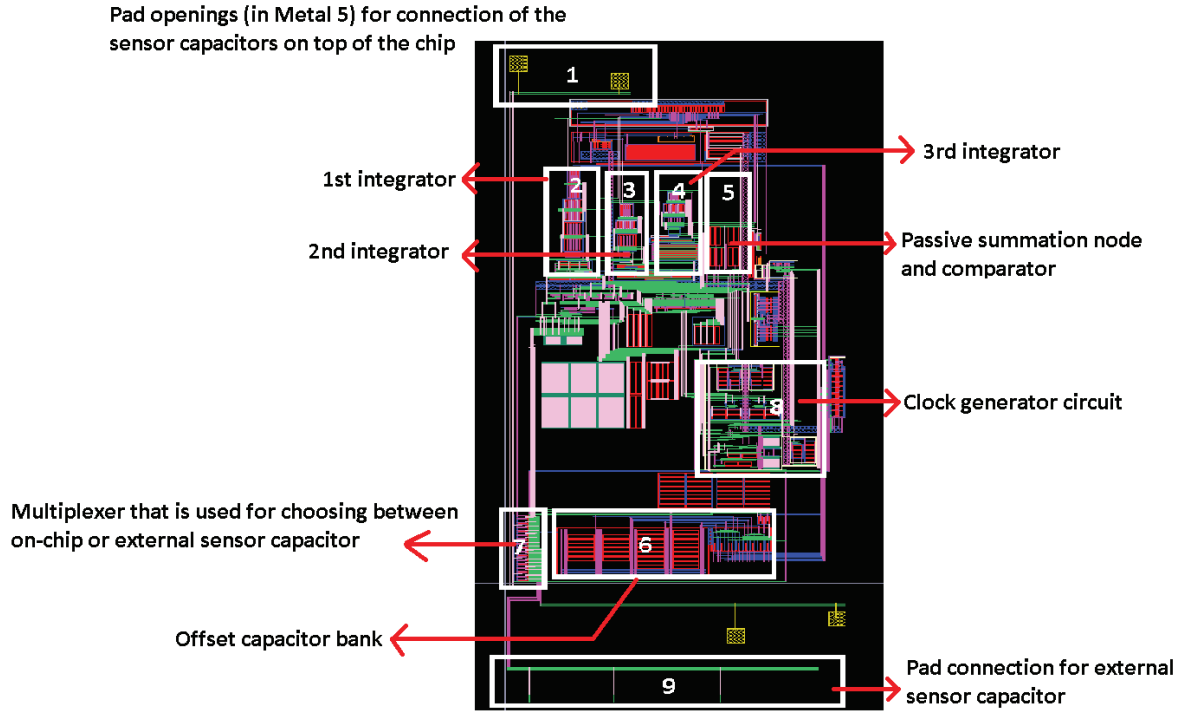


Figure 4-3: Layout of the CDC

4-3 Performance of the CDC

The simulated results of the CDC are summarized in Table 4-2. The state-of-the-art energy consumption for CDC is 8.3nJ [2]. Based on the simulation results, the current design achieves 2.01nJ which is roughly 4X times better than the state-of-the-art CDC while also achieving a substantially higher resolution. The use of double sampling, system level chopping techniques and the use of supply voltage as V_{ref} has resulted in the better performance of our CDC when compared to the state-of-the-art [2].

Specification	Performance
Technology	0.16μm
Supply	1.2V
Current consumption	2.33μA (Analog blocks)
Measurement time	0.72ms
Input range	0.87pF - 1.13pF
Full scale	0.26pF
ENOB	16 bits
Area	$0.34mm^2$
Energy	2.01nJ
FOM	0.03pJ/step

Table 4-2: Performance summary of the CDC

4-3-1 Bitstream FFT

The FFT of the bitstream of the incremental $\Delta\Sigma$ ADC is shown in Figure 4-4 and Figure 4-5 for the supply voltage, VDD = 1.2V and 1.8V respectively. The simulation was run for 10ms to obtain sufficient number of samples for the FFT and Hanning window was applied. As seen in both the figures, the 3rd order noise shaping is clearly seen.

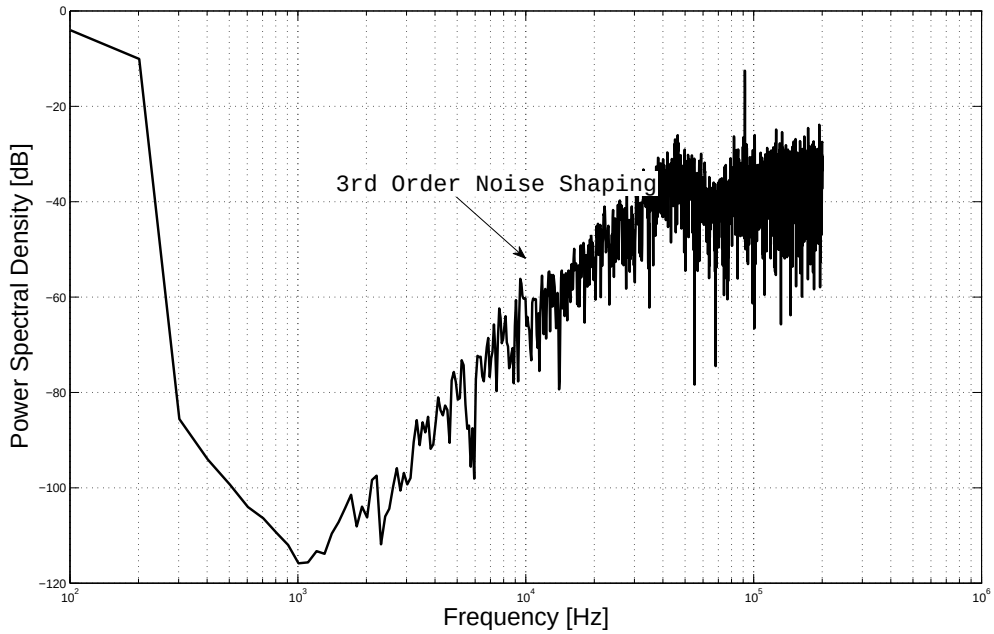


Figure 4-4: Simulated FFT of 3972 point bitstream with Hanning window (supply voltage = 1.2V)

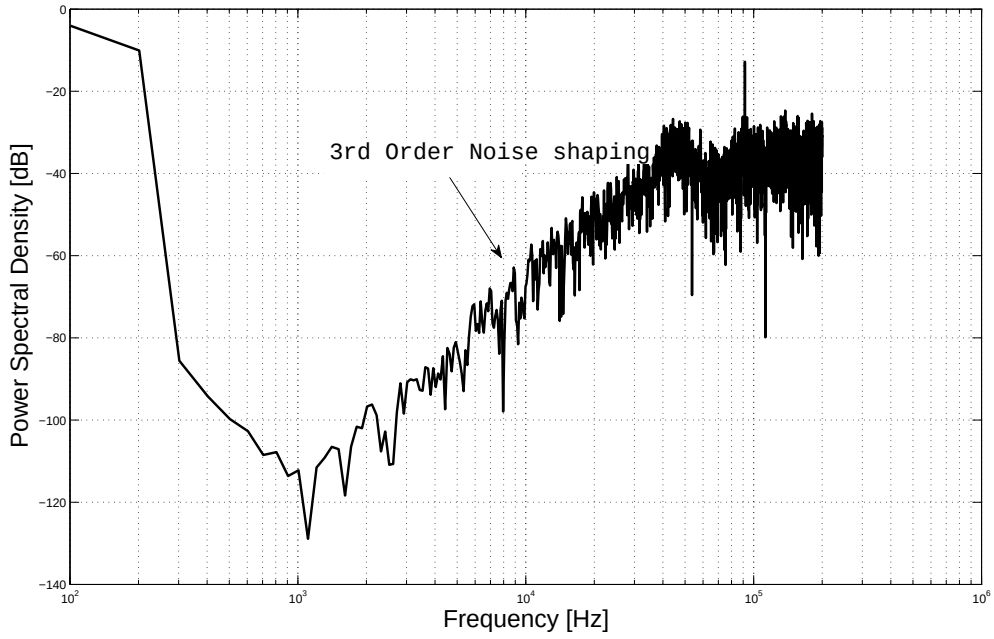


Figure 4-5: Simulated FFT of 3972 point bitstream with Hanning window (supply voltage = 1.8V)

4-3-2 Resolution

The performance of the CDC (at a supply voltage of 1.2V) when the input capacitance is swept is shown in Figure 4-6. The offset capacitance was set to 1pF and the reference capacitor (which is fixed) is 200fF. CoI (Cascade-of-Integrators) filter was implemented in Verilog-A and used for obtaining the digital output of the CDC. The simulation result shows that it achieves the required accuracy across the input range. The performance of the CDC was also checked with the following conditions: two capacitors were connected from either of the terminals of the sensor capacitance (C_x) to ground with a value of $4.C_x$. This mimics the parasitic loading effect of the sensor capacitance that is connected off-chip. The CDC achieved the required ENOB after the clock period was relaxed from 5μs to 10μs. Thus it proves that the CDC is functional with both on-chip and off-chip sensor capacitance.

4-4 Issues of the CDC at 1.8V Supply

The CDC when operated with 1.8V supply didn't give the required performance. The ENOB drops below 10 bits. Although we obtained the expected 3^{rd} order noise shaping (Figure 4-5), the output swing of the integrators were within desired range of ± 100mV and they showed proper settling, but still the required ENOB was not achieved. The issue has to be debugged in the future.

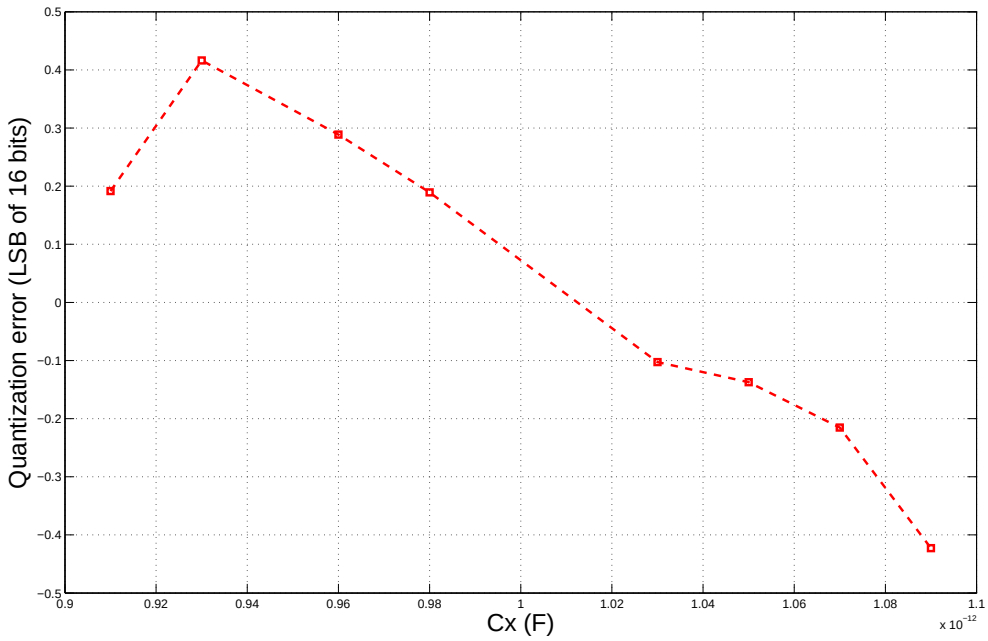


Figure 4-6: Quantization error plot of the CDC

Chapter 5

Conclusion

5-1 Thesis Contribution

A 3^{rd} order incremental $\Delta\Sigma$ ADC optimized for interfacing with a MEMS-based pressure sensor has been presented in this thesis. The system is implemented in NXP 0.16μm CMOS technology. The layout of the CDC has been completed and the post-layout simulations indicate proper operation of the circuit with 1.2V supply. The following are the contributions of this thesis:

- **Systematic analysis of CDC**. The thesis has clearly outlined a systematic analysis of thermal and quantization noise and energy-efficiency analysis procedures of a CDC. Using this analysis different CDC architectures can be compared, which has also been demonstrated in the thesis by comparing linear and non-linear CDC. The discussions are quantified with derivations and MATLAB simulations.
- **Novel CDC architecture**. In the thesis, a novel non-linear CDC architecture has been proposed and completely analysed at the system level.
- **Energy-Efficient CDC**. The thesis has demonstrated a CDC that achieves 4X better performance in terms of energy consumption when compared to the current state-of-the-art CDC [2] (based on simulation results alone) while also achieving a substantially higher resolution. This performance was achieved by various design techniques such as *double sampling*, *system-level chopping* and *a novel inverter-based OTA* which helped to achieve one of the best performing CDC in terms of energy-efficiency. These design techniques were for the first time demonstrated in a CDC.

5-2 Future Work

The operation of the CDC at 1.8V supply needs to be debugged and fixed. The Layout of the CDC has been completed and can be taped out. Some of the potential improvements or extensions of this work are provided below.

- The novel non-linear CDC can be implemented and compared with existing CDC architectures. The circuit implementation of this CDC would be quite interesting. The loop filter architecture will almost remain the same with modifications required in the frontend of the CDC.
- The floating inverter-based OTA can be implemented with Class AB biasing and its performance in CDC can be investigated.

Appendix A

Discussion of Linearization Approach

In section 2-4 of the thesis, a linearization routine in MATLAB was done for choosing of the coefficients $(\alpha, \beta, \delta, \gamma)$ of the non-linear CDC. Based on the MATLAB routine, we chose the following coefficients (α = -2, β =-1, δ = 0.6, γ =2.2). The output of the non-linear CDC and the linear fitting done in MATLAB is shown in Figure A-1. Figure A-2 shows the residual non-linearity in terms of pressure for the non-linear CDC. The maximum non-linearity is around 0.05 bar. Depending on the linearity requirements, further linearization in the back-end may be required.

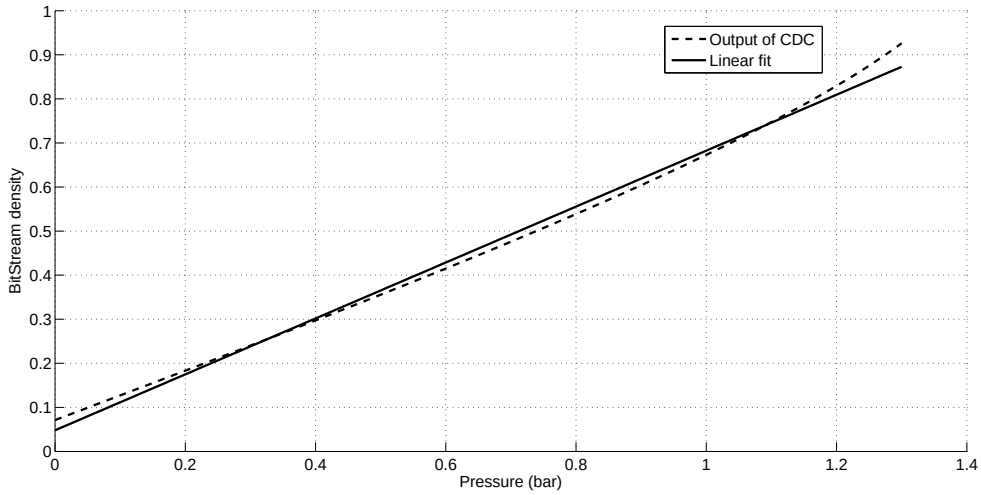


Figure A-1: Output of non-linear CDC and linear fitting in MATLAB

To have an appreciation of the linearization done by the non-linear CDC in the front-end, let's consider the case of the linear CDC. The output of the linear CDC and the linear fitting done in MATLAB is shown in Figure A-3. Figure A-4 shows the residual non-linearity in terms of pressure for the linear CDC. The maximum non-linearity is around 0.426 bar.

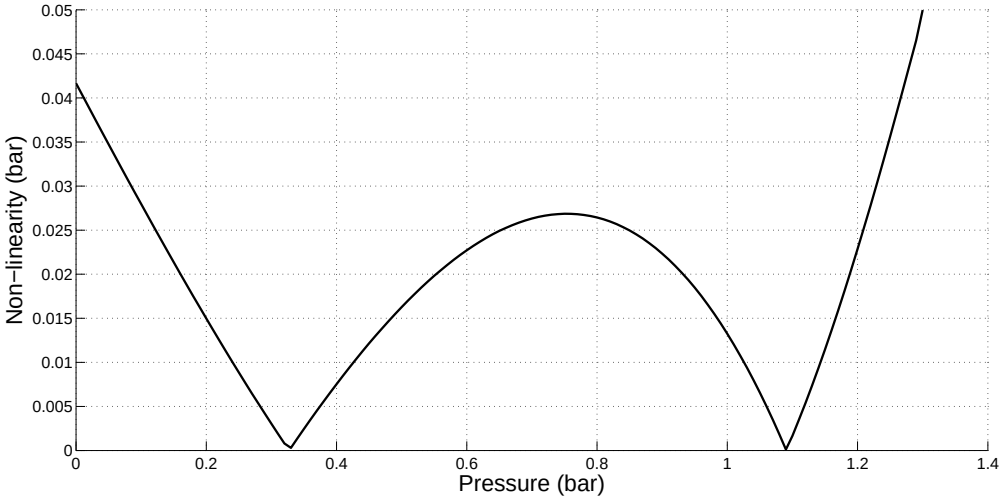


Figure A-2: The absolute non-linearity in CDC's output μ - non-linear CDC

We can clearly see the power of linearization obtained using the non-linear CDC which achieved a maximum non-linearity of around 0.05 bar compared to 0.426 bar obtained by the linear CDC.

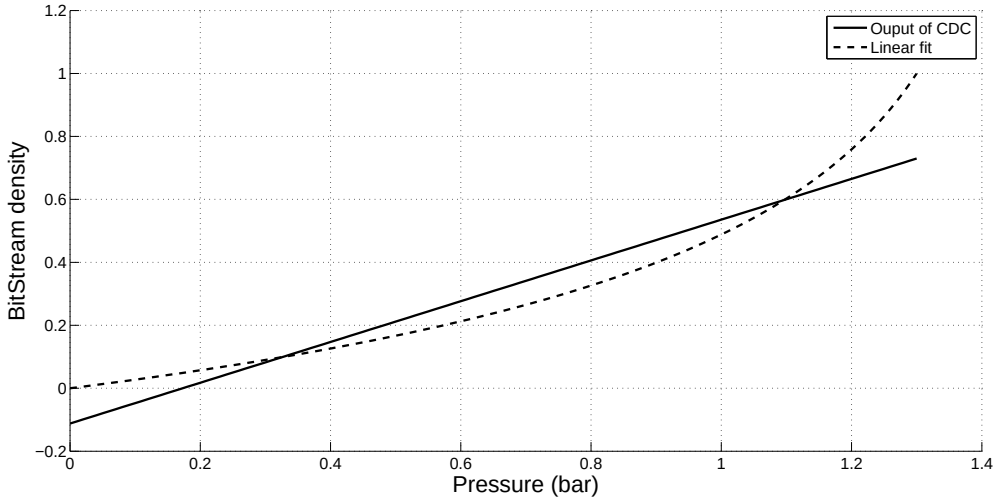


Figure A-3: Output of linear CDC and linear fitting in MATLAB

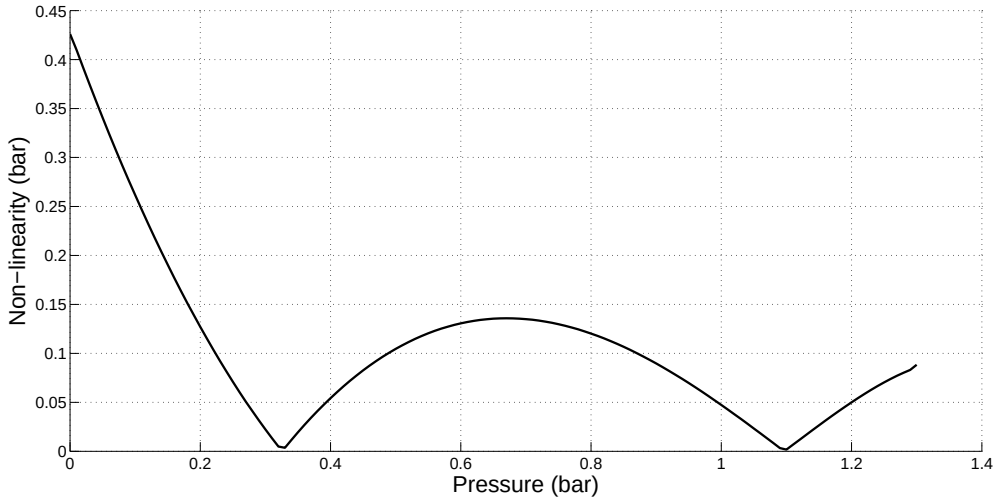


Figure A-4: The absolute non-linearity in CDC's output μ - linear CDC

Bibliography

[1] W. Besling. NXP Semiconductors, Eindhoven, private communication, 2013.

[2] Z. Tan, Y. Chae, R. Daamen, A. Humbert, Y. Ponomarev, and M. A. P. Pertijs, "A 1.2V 8.3nJ energy-efficient CMOS humidity sensor for RFID applications," in *VLSI Circuits (VLSIC), 2012 Symposium on*, pp. 24–25, 2012.

[3] Z. Tan, *Energy-Efficient Capacitive-Sensor Interfaces*. PhD thesis, TU Delft, June 2013.

[4] J. O'Dowd, A. Callanan, G. Banarie, and E. Company-Bosch, "Capacitive sensor interfacing using sigma-delta techniques," in *Sensors, 2005 IEEE*, 2005.

[5] S. Xia and S. Nihtianov, "Comparison of different methods to cancel offset capacitance in capacitive displacement sensors," in *Instrumentation and Measurement Technology Conference (I2MTC), 2012 IEEE International*, pp. 1838–1841, 2012.

[6] M. Pertijs and J. Huijsing, *Precision Temperature Sensors in CMOS Technology*. Analog Circuits and Signal Processing, Springer, 2006.

[7] R. Schreier, J. Silva, J. Steensgaard, and G. Temes, "Design-oriented estimation of thermal noise in switched-capacitor circuits," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 52, no. 11, pp. 2358–2368, 2005.

[8] M. Pertijs and Z. Tan, "Energy-efficient capacitive sensor interfaces," in *Nyquist AD Converters, Sensor Interfaces, and Robustness* (A. H. van Roermund, A. Baschirotto, and M. Steyaert, eds.), pp. 129–147, Springer New York, 2013.

[9] J. Markus, *Higher-order incremental delta-sigma analog-to-digital converters*. PhD thesis, Budapest Univ. Technology and Economics, March 2005.

[10] R. Schreier and G.C.Temes, *Understanding Delta-Sigma Data Converters*. IEEE Press/Wiley, 2004.

[11] X. Peng and W. Sansen, "AC boosting compensation scheme for low-power multistage amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 11, pp. 2074–2079, 2004.

[12] K. Bult and G. Geelen, "A fast-settling CMOS op amp for SC circuits with 90-dB DC gain," *IEEE Journal of Solid-State Circuits*, vol. 25, no. 6, pp. 1379–1384, 1990.

[13] B. J. Hosticka, "Dynamic CMOS amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 15, no. 5, pp. 881–886, 1980.

[14] B. Nauta, "A CMOS transconductance-C filter technique for very high frequencies," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 2, pp. 142–153, 1992.

[15] Y. Chae and G. Han, "Low Voltage, Low Power, Inverter-Based Switched-Capacitor Delta-Sigma Modulator," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 2, pp. 458–472, 2009.

[16] M. Bazes, "Two novel fully complementary self-biased CMOS differential amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 26, no. 2, pp. 165–168, 1991.

[17] A. Grasso and S. Pennisi, "High-performance CMOS pseudo-differential amplifier," in *Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on*, pp. 1569–1572 Vol. 2, 2005.

[18] J. Custodio, J. Goes, N. Paulino, J. Oliveira, and E. Bruun, "A 1.2-V 165- μW 0.29-mm^2 Multibit Sigma-Delta ADC for Hearing Aids Using Nonlinear DACs and With Over 91 dB Dynamic-Range," *Biomedical Circuits and Systems, IEEE Transactions on*, vol. 7, no. 3, pp. 376–385, 2013.

[19] S. Gambini, K. Skucha, P. Liu, J. Kim, and R. Krigel, "A 10 kPixel CMOS Hall Sensor Array With Baseline Suppression and Parallel Readout for Immunoassays," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 1, pp. 302–317, 2013.

[20] B.Razavi, *Design of Analog CMOS Integrated Circuits*. Tata McGraw-Hill, 2002.

[21] T. Burmas, K. Dyer, P. Hurst, and S. Lewis, "A second-order double-sampled delta-sigma modulator using additive-error switching," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 3, pp. 284–293, 1996.

[22] Z. Yang, L. Yao, and Y. Lian, "A 0.5-V 35- μW 85-dB DR Double-Sampled $\Delta\Sigma$ Modulator for Audio Applications," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 3, pp. 722–735, 2012.

[23] W. Shen, *Low-Power Double-Sampled Delta-Sigma Modulator for Broadband Applications*. PhD thesis, Oregon State University, July 2010.

[24] R. J. Baker, *CMOS Circuit Design, Layout, and Simulation, Third Edition*. Wiley-IEEE Press, 2010.

[25] T. Cho and P. Gray, "A 10 b, 20 Msample/s, 35 mW pipeline A/D converter," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 3, pp. 166–172, 1995.

[26] S. Rabii and B. Wooley, *The design of Low-Voltage Low-Power Sigma-Delta Modulators*. Kluwer Academic Publishers, 1999.