OLED Display with SG-TFT

Master's Thesis

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OLED Display with SG-TFT

THESIS

submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE

in

ELECTRICAL ENGINEERING

by

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Abstract

OLED is a current based device, which emitted amount of light depends on the current supplied to the device so steady current flow is needed. In Active Matrix Organic Light Emitting Diode (AMOLED) Display. TFTs are used as driving transistors for OLED. Because of the non uniformity of the TFTs, variation in threshold voltage and mobility has a negative effect in performance of the OLED. During this thesis we investigated two types of driving scheme, Voltage and current programmable pixels, with Single grain Si TFT. New structure of pixel is purposed with array of photodiodes beneath Cathode/Anode layer of OLED which is used for giving optical feedback to the driving TFT. With this structure, possibility of compensation for the threshold voltage variation is investigated.

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Acknowledgement

I express my gratitude to my promotor Prof. dr. C. I. M. Beenakker for giving me a chance to commence this thesis. I thank dr. Ryoichi Ishihara for his daily supervision during this research work. I especially thank dr. Jaber Derakhshandeh for his help in process steps and sharing his valuable knowledge regarding SG-TFT. I also thankfull to Michiel van der Zwan for accompanying me in cleanrooms and LABs and helping me with the OLED process and fabrication. I thank Daniel Tajari Mofrad for his daily help during this thesis. I especially thank Martijn Tijssen, Dong Zhang, Olindo Isabella from Photovoltaic group for helping me with ITO deposition and metal evaporation.

I would like to thank all process technologists of the ICP group who have helped me to complete my thesis successfully.

Amir Naeimi
Delft, the Netherlands
April 18, 2011

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1.1 Display Technology

Display technology is evolved from cathode ray tube (CRT) in 1922 to nowadays matured technologies such as LCD and Plasma display. Because of bulky size and heavy weight of CRT, always there was a need for thinner displays. nowadays flat panel displays are everywhere in our daily lives: mobile phones, notebooks, monitors and TVs are a few examples.

There are several types of flat panel display technologies, namely: liquid crystal displays (LCDs), plasma display panels (PDPs), light emitting diodes (LEDs) and organic light emitting devices (OLEDs). They are radically different due to thier applications and unique properties.[1]

Light emitting diodes (LEDs) and organic light emitting devices (OLEDs) are electroluminescent devices with semiconductor (crystalline) and organic materials (amorphous) structures, respectively. Electrons and holes recombine within the emissive materials, where the bandgap of the materials determines the emission wavelength.[2]

Amorphous organic material has a much lower mobility than crystalline semiconductors, which results in a higher driving voltage of OLEDs. Due to the amorphous characteristics of OLED, it is possible to fabricate OLED displays in large sizes (>40 inches). Since the conductivity of amorphous organic materials is very low, very thin organic films (40– 150 nm) are required to reduce the driving voltage (<10 V). This is quite a challenge in thin film formation, especially for large size substrates. There are several fabrication technologies proposed, such as physical vapor deposition, spin coating, ink jet printing and laser assisted patterning. Prototypes of OLED panels of 40 inches have been demonstrated, and OLEDs of 11 inches (or less) are also commercially available.[3] Another challenge for large displays is the reliability. A large display (Tv, Monitor) must have a longer lifetime than a mobile phone. Recently, commercial OLED products for mobile displays and monitors have emerged, shown in Fig.1.1. However, for TV applications, OLED panel lifetime still falls short. The main advantages of OLEDs are:

1. Low process temperature

Figure 1.1: Sony's latest 19" monitor.

2. Nonselective to the substrate material, which is suitable for flexible displays.

3. Very thin structure.

A lot of research is going on field of OLED which mainly focused to improve device performance especially driving voltage and lifetime . Also, due to the possibility of large size fabrication, the potential manufacture cost of OLEDs is lower than that of LEDs. Because OLEDs have some advantages in performance and fabrication cost over LEDs, they have a chance to replace LEDs in some applications since they are both electroluminescent devices with similar operation principles. Besides, in comparison with LEDs, OLEDs have two unique advantages: larger panel size and higher resolution.

1.2 Research objectives

This report mainly focused on driving circuit of the OLED. OLED is a current based device, which emitted amount of light depends on the current supplied to the device so steady current flow is needed. In Active Matrix Organic Light Emitting Diode (AMOLED) Display. TFTs are used as driving transistors for OLED. Because of the non uniformity of the TFTs, variation in threshold voltage and mobility has a negative effect in performance of the OLED. During this thesis work, first I will discuss the Single Grain TFT and its characteristic and explain why it is good for OLED backplane (Chapter 2). Then OLED operation and characteristics will be discussed (Chapter 2). In chapter 3 we will examine different types of pixel structures and create a module of OLED for simulation and new purposed pixel structure will be discussed. In chapter 4 we will discuss the measurement results and last Chapter will be the conclusion and contribution of this thesis.

The Technology 2

The OLED Display that we are developing at the TU Delft is based on two technologies. The first is the μ-Czochralski Single Grain Thin-Film Transistor technology. This is used for the integrated electronics. The second is the Organic LED material from Ossila Ltd, the Active layer for our OLED Display.

This chapter is organized in two sections, explaining the SG-TFT Technology (Section 2.1) and the Organic material (Section 2.2).

2.1 μ-Czochralski Single Grain Thin-Film Transistor

Transistors can be made out of different materials. Looking only at silicon transistors, it is possible to make them out of amorphous silicon (a-Si), poly-crystalline silicon (poly-Si) and single-crystalline silicon (c-Si) [4]. The difference is in the way silicon atoms are organized and are characterized by size of the ordered regions within the material. An ordered region is where the silicon atoms have regular geometric arrangement or periodicity. a-Si lacks such ordered regions, while poly-Si have ordered regions, but vary in size and orientation with respect to one another. These ordered regions are called grains and are separated from each other by grain boundaries. c-Si has a regular geometric periodicity throughout the entire material, all with the same grain (single grain). The c-Si electrical properties are superior compared to a-Si and poly-Si, since c-Si lacks the grain boundaries that degrade the electrical characteristics, making it a suitable material for high performance transistors.[5]

The Thin-Film Transistor (TFT) is a type of MOS transistor where the active semiconductor material (silicon) is deposited as a thin-film over a supporting substrate. The substrate can be a large panel, for example glass, for making large LCD screens. Since the silicon is deposited, the type of silicon is limited to a-Si or poly-Si type. In contrast, regular type MOS transistors are made from c-Si wafers. These wafers are grown from a single seed, and have regular geometric periodicity throughout the entire wafer.

The μ-Czochralski Single Grain Thin-Film Transistor (SG-TFT) technology is a method to produce high performance transistors out of amorphous silicon by Excimer-laser crystallization. These SG-TFTs out-perform the a-Si and poly-Si TFTs, and yet

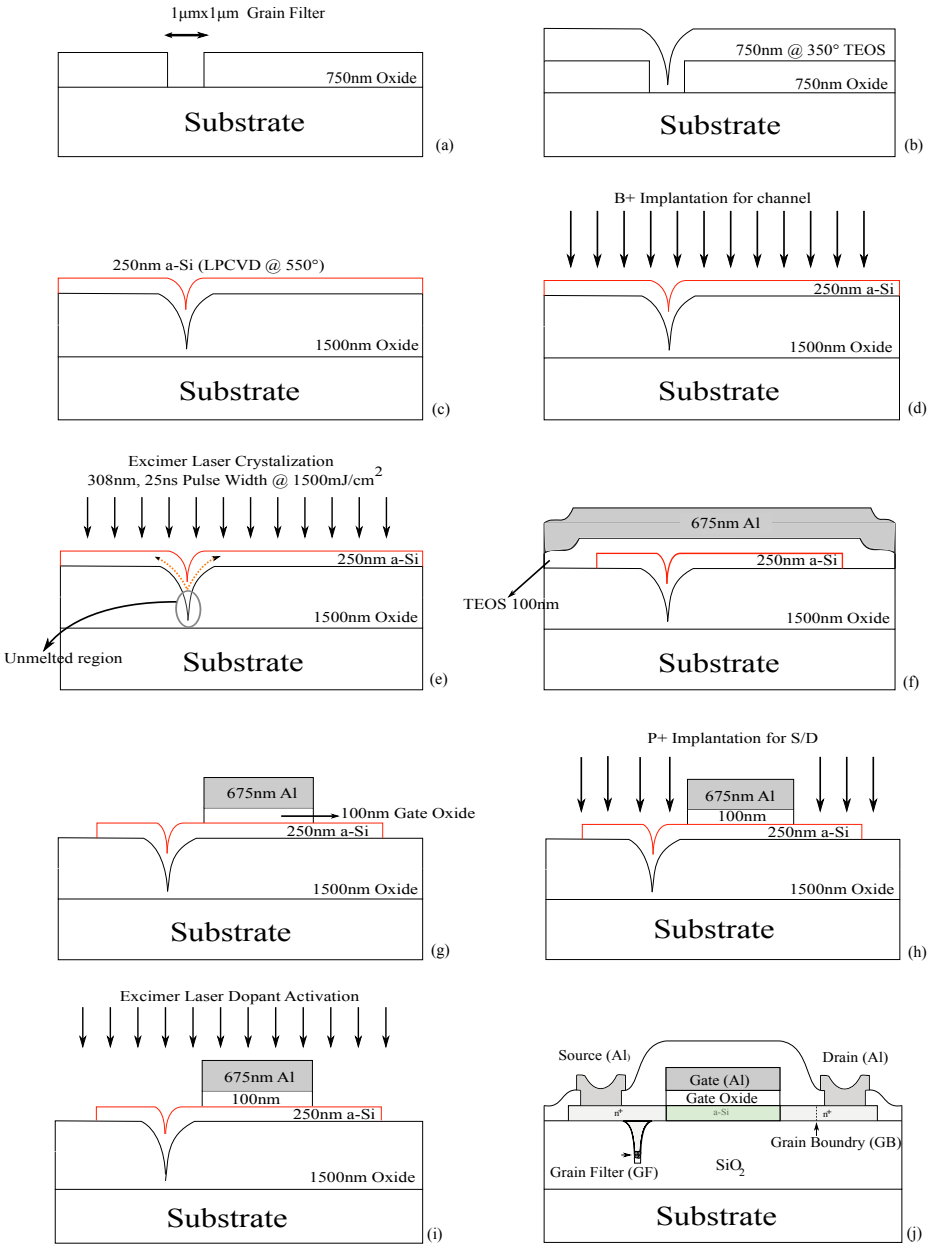


Figure 2.1: The SG-TFT process steps.

the electrical performance is comparable to c-Si transistors [6]. SG-TFT technology has the advantage of high performance SG transistors that can be fabricated on a panel substrate, for example glass or Polyethylene terephthalate (PET), with the possibility to use these transistors in analog, digital and RF circuits. Advantages of the SG-TFT when used with OLED are as following: stability, integration with other devices, uniformity, and being able to realize photodiodes with same technology. Table 2.1 compares various type of TFT technologies.

Table 2.1: Comparison of Various type of TFTs.

[7, 8]

	a-Si TFT	poly-Si TFT	SG-TFT
Field effect mobility ($cm^2/V.sec$)	0.1-1	50-300	500-600
Off Current (pA)	<1	~ 0.1	~ 0.1
Type of TFT	NMOS	P/N.MOS	P/N. MOS
Uniformity	Good	Poor	Good
Stability	Bad	Good	Very good

2.1.1 SG TFT Process Steps

As shown in Figure 2.1, we start of with a substrate (Si, Glass or PET), where SiO_2 is deposited on top. Small cavities are patterned in the SiO_2, these cavities are called the *grain filters*. A layer of a-Si is deposited on top, covering everything and filling up the cavities. An Excimer laser is used to crystallize the silicon: the laser partially melts the a-Si, the bottom of the cavities stays unmelted and forms the seed for the crystallization of the upper silicon. The *grain filter* ensures that the crystallization is grown from a single grain. The result can be seen in Figure 2.3a, where the *single grains* form a grid and the *grain filters* can be found in the middle of each square shaped *single grain*. Inside these grains, source and drains are made by implanting with phosphorus and boron for NMOS SG-TFT and PMOS SG-TFT respectively. Ideally, these islands are of a single grain. Although planar defects are present inside the *single grain*, it has been reported that these defects are less active than random grain boundaries [9] [10]. These planar defects often grown out the grain filter radially [11]. It is possible to place the transistor channel parallel to these planar defects so that the current flow does not cross these defects, resulting in a higher mobility for better transistors. In Figure 2.3b, the transistor placed in position X has the highest field effect mobility.

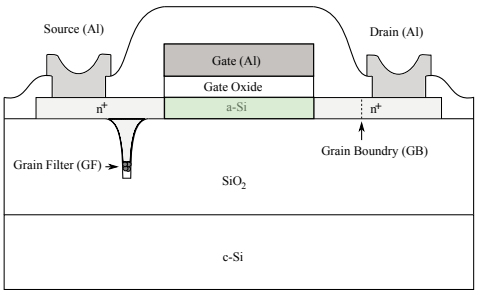
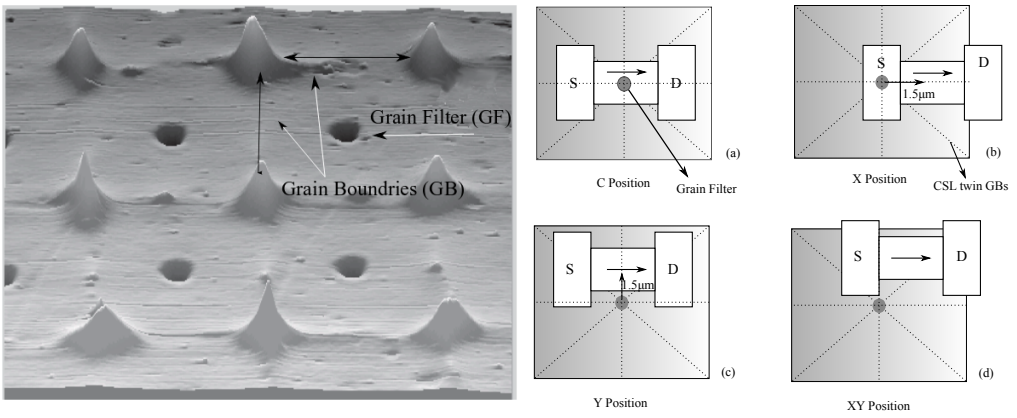


Figure 2.2: Cross section of an n-channel SG-TFT inside a location controlled grain.

All the fabrication steps can be done at relatively low temperatures (<350°). This makes it possible to fabricate SG-TFT on cost-effective plastic substrate (PET) for flexible electronics. In our case a flexible OLED display (FOLED) drivers.



(a) (b)

Figure 2.3: AFM image of a grid of grains formed by the μ-Czochralski process. Different TFT channel orientation with respect to the grain filter with positions C, X, Y, XY.

2.1.2 SG Thin-Film Transistor performance

The SG Thin-Film Transistor have better electrical characteristics compared to the a-Si and poly-Si transistors. Near SOI[1] performance have been reported [7], with high field effect mobility (μ_{FE}) of average 600 cm^2/Vs and 270 cm^2/Vs for n-channel and p-channel respectively in X positioned grain Control. In Table 2.2 the performance parameters the mobility (μ_{FE}), subthreshold swing (V/dec), threshold voltage (V) and off-current (A) are seen for both NMOS and PMOS SG-TFTs [6].

Field Effect Mobility (μ_{FE})
One of the most important parameters to characterize TFTs is the Field Effect Mobility (μ_{FE}). The mobility relates the carrier (electron or hole) velocity to the electric field (expressed in μ_{FE}).

Subthreshold Swing (S)
The subthreshold swing slope factor S describes the quality of the turn-on characteristics. The slope factor S defines the amount of gate voltage needed to change the drain current by a factor of 10 (expressed in V/dec). For digital applications, an ideal switch-like behavior is desired. An ideal transistor has a S parameter of 60 mV/dec.

Threshold Voltage (V_{th})
The gate-source voltage at which conduction appears in the channel is called the

[1] Silicon On Insulator technology, used to reduce parasitic device capacitance and thereby improve transistor performance.

threshold voltages. A low threshold voltage is desired, so that the TFT operational regime is within a reasonable voltage range.

Off-Current (I_{off})
The off-current is the minimum current in the transfer characteristics of the TFT. It is the current that still is present when the TFT is off.

Table 2.2: SG-TFT Performance Parameters.

SG-TFT Device	$\mu_{FE,e}[cm^2/Vs]$	S[V/dec.]	$V_{th}[V]$	I_{off}(A)
NMOS	600	0.2	0.5	$1.3 \cdot 10^{-13}$
PMOS	270	0.13	-2.3	$1 \cdot 10^{-14}$

2.1.3 Location controlled single grain TFT Performance

As it shown in Figure. 2.3b, there are four locations for grain to be positioned in or around the channel. The Table. 2.3 shows the electrical properties of NMOS and PMOS devices fabricated in mentioned locations. As it is shown in Table. 2.3 , X position has the highest mobility, lowest subthreshold slope (S) and lowest leakage current (I_{OFF}) meanwhile C position has the better uniformity for mobility. The highest mobility for SG-TFT at X position is due to the fact that the carriers do not feel the coincidence site lattice (CSL) twin boundaries, which are parallel to the direction of current flow. [11]

Table 2.3: Electrical properties of NMOS and PMOS SG-TFTs with different grain position.

TFTs	Position	$\mu_{FE,e}[cm^2/Vs](\sigma\%)$	S[V/dec.](σ%)	$V_{TH}[V](\sigma\%)$
SG	X	597±101(17%)	0.21±0.03(13%)	1.7±0.2(11%)
	Y	528±57(10%)	0.25±0.04(14%)	1.8±0.3(15%)
	XY	505±55(7%)	0.22±0.01(6%)	1.9±0.1(6%)
	C	471±32(7%)	1.1±0.13(12%)	0.86±0.3(32%)
SOI		727±18(2.4%)	0.18±0.006(3.6%)	1.1±0.09(8%)

(a) NMOS

TFTs	Position	$\mu_{FE,e}[cm^2/Vs](\sigma\%)$	S[V/dec.](σ%)	$V_{TH}[V](\sigma\%)$
SG	X	273±27(11%)	0.14±0.04(24%)	-2.2±0.38(17%)
	Y	202±26(13%)	0.15±0.02(21%)	-2.3±0.52(24%)
	XY	219±44(20%)	0.18±0.02(8%)	-3.36±0.58(23%)
	C	228±22(10%)	0.16±0.03(16%)	-3.3±0.64(25%)

(b) PMOS

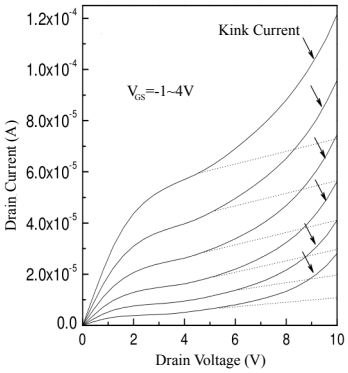


Figure 2.4: Kink effect at IV characteristic of n-channel SG-TFT.

2.1.4 Reliability of SG-TFT

During this project mainly NMOS transistor were used for designing the pixels. There are few reliability issues with SG-TFT transistor which are described as following:

The Kink Effect

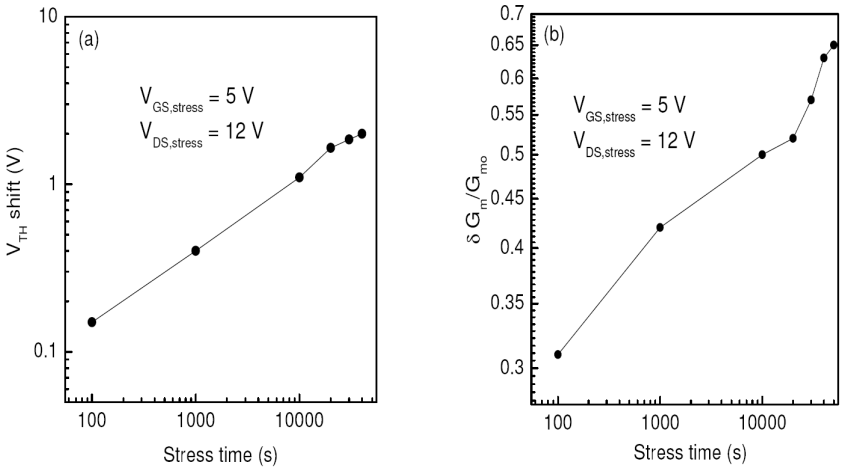
Build up of positive charge due to accumulation of holes in the substrate is one of major parasitic effects in TFTs. The accumulation of holes in substrate is generated by impact of ionization at high lateral electric fields, which is called *Floating body effect,* one of the consequence of floating body effect is the Kink Effect. Figure.2.4 shows the I-V characteristic of n-channel SG-TFT. Similar to SOI devices, the high kink current causes a premature breakdown of such TFTs.[12]

Threshold Voltage variation

The threshold voltage V_{th} is an important parameter for the operation of a circuit. It is very sensitive to the injection of carriers in the gate oxide as well as the creation of traps by high supply voltages. Changes in V_{th} are a measure of device stability. The degradation of TFTs (Fig.2.5), resulting from drain hot carrier injection, causes a change in V_{th} and the transconductance (g_m).[5]

2.2 Organic Light Emitting Diode

A schematic of a conventional three layer OLED is shown in Fig.2.6. Three organic layers are sandwiched between a Cathode and a transparent Anode. Energy states in organic materials can be described by molecular orbitals, which are combinations of all the atomic orbitals. The electrons fill the molecular orbitals from the lowest energy states so that the Highest Occupied Molecular Orbital (HOMO) can be defined. Once



(a) (b)

Figure 2.5: Degradation of V_{th} and G_m during stress time.

the system is excited, the electrons can be promoted to higher molecular orbitals. The first excited state is called the Lowest Unoccupied Molecular Orbital (LUMO). The HOMO and LUMO in organic materials are similar to the valence and conduction band in semiconductor materials.

Electron transport layer (ETL) and hole transport layer (HTL) are somehow similar to the n-type and p-type in semiconductor materials, with relatively high electron and hole mobilities, which recombine near the organic–organic interface.

Carrier injection from the electrode to organic layer can be improved by adjusting the work function of the metal electrodes. A high work function anode, indium tin oxide (ITO), and low work function cathode, Mg:Ag alloy or Ca, are hence chosen for better carrier injection. Also, since ITO is transparent, the emitted photons radiate through the anode and glass substrate, to the far field.

To reduce the driving voltage, improve the quantum efficiency and extend the operation lifetime, a multilayer structure was proposed, such as a Hole Injection Layer (HIL), Hole Blocking Layer (HBL) and Electron Injection Layer (EIL). Emission wavelength from an OLED can be adjusted by the emitting layer (EML) material and device structures.

During this project Organic material and components were provided by *Ossila Ltd.* In the following subsection we will investigate the characteristics and the process steps of the Ossila F8TB (Green color Polymer based organic fluid) and PEDOT:PSS.

2.2.1 Operation Principle

As shown in Fig.2.6, by applying positive voltage to Anode and negative to Cathode, holes and electrons will be injected from the anode and cathode respectively (step ❶),

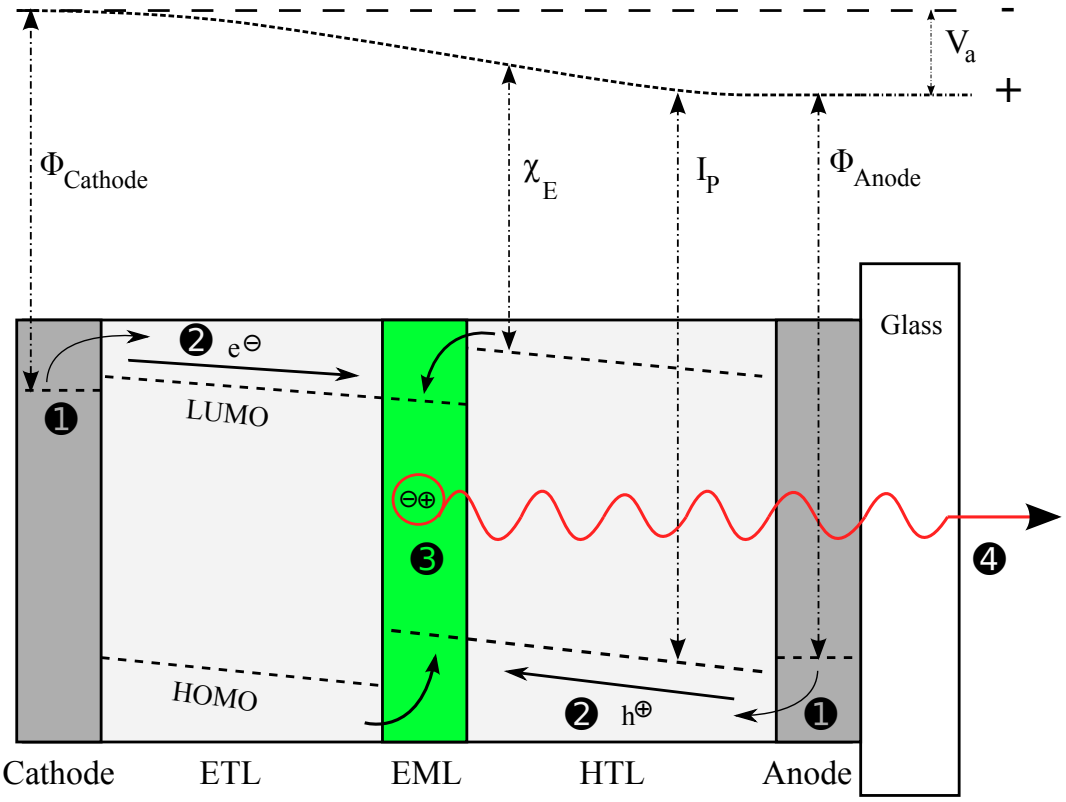


Figure 2.6: OLED layer structure and band diagram.

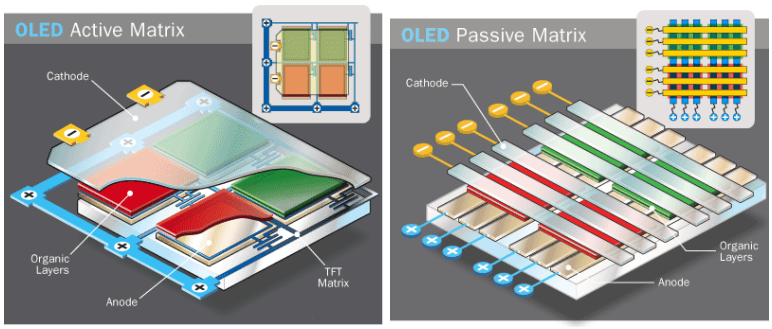
to the hole transport layer (HTL) and electron transport layer (ETL), (step ❷), and then recombined in emitting layer (EML), (step ❸), and emit light (step ❹).

2.2.2 OLED Display Types

There are several types of OLEDs: Passive-matrix OLED, Active-matrix OLED, Transparent OLED, Top-emitting OLED, Foldable OLED, White OLED

Passive Matrix OLED (PMOLED):

PMOLEDs have strips of cathode, organic layers and strips of anode. The anode strips are arranged perpendicular to the cathode strips. The intersections of the cathode and anode make up the pixels where light is emitted. External circuitry applies current to selected strips of anode and cathode, determining which pixels get turned on and which pixels remain off. Again, the brightness of each pixel is proportional to the amount of applied current. PMOLEDs are easy to make, but they consume more power than other types of OLED, mainly due to the power needed for the external circuitry. Even



(a) Active matrix OLED (b) Passive matrix OLED

Figure 2.7: Active matrix OLED vs Passive matrix OLED.

[14]

with the external circuitry, passive matrix OLEDs consume less power than the LCDs. Fig.2.7b shows the structure of PMOLED.

Active Matrix OLED (AMOLED):

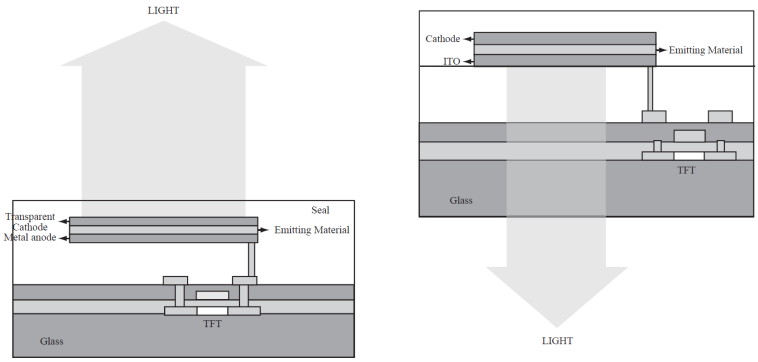
AMOLEDs have full layers of cathode, organic molecules and anode, but the anode layer overlays a thin film transistor (TFT) array that forms a matrix. The TFT array itself is the circuitry that determines which pixels get turned on to form an image. AMOLEDs consume less power than PMOLEDs because the TFT array requires less power than external circuitry, so they are efficient for large displays.[13] The best uses for AMOLEDs are computer monitors, large-screen TVs and electronic signs or billboards. During this project AMOLED is used as backplane structure for OLED. Fig.2.7a shows the AMOLED structure.

Transparent OLED (TOLED):

Typically, an OLED has a transparent ITO anode and a reflective cathode, with high and low work functions. By replacing the reflective cathode with a transparent conductive layer (e.g. ITO), a see through display can be achieved. However, since the work function of ITO is high (~ 4.7 eV), not suitable for electron injection, a suitable buffer layer between the ETL and ITO 'cathode' is needed for better carrier injection capability. Such an opaque buffer layer must be thin enough to provide high transmittance. One of the main application of TOLED is to be used for heads-up displays.

Top emitting OLED:

Typically, a top emitting OLED has a high reflective anode and a semitransparent or transparent cathode. Hence, light comes out from the semitransparent cathode side. The TFTs can be hidden underneath the reflective anode and hence the aperture ratio



(a) Top emitting OLED. (b) Bottom emitting OLED.

Figure 2.8: Top emitting OLED Vs. Bottom emitting OLED.

is increased. Top emitting is one of the most promising technologies for achieving high aperture ratio AMOLEDs. They are best suited to active matrix design.[15]

Foldable OLED (FOLED)

Foldable OLEDs have substrates made of very flexible metallic foils or plastics. Foldable OLEDs are very lightweight and durable.

2.2.3 OLED Material

There are two main kinds of OLEDs. For a molecular weight less than 1000 g/mot, the device is called a small molecule OLED, which can usually be thermally evaporated under high vacuum or spin coated in oxygen free environment. For a molecular weight over 10,000 g/mot, the device is called a polymer OLED (or polymeric light-emitting device, PLED), which can be used with Ink jet patterning and spin coating.

During this project both small molecule OLED and Polymer OLED were experimented, but only the Polymer OLED successfully fabricated. Appendix B gives a overview for process steps taken for making small molecule OLED and it's failure reason.

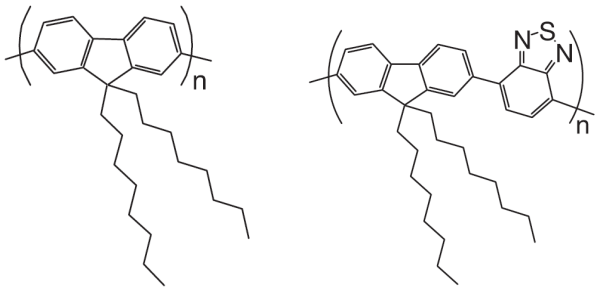
PLED Active Layer

During this project, F8 (95%):F8BT(5%) was used as active layer for fabricating PLED and supplied by Ossila Ltd[2]. This polymer blend is a mixture of F8 and F8BT polymers. Table.2.4 summarizes the semiconductor properties of these polymers and Fig.2.9 shows their chemical structure.[16]

[2]www.Ossila.com

Table 2.4: PLED active layer properties.

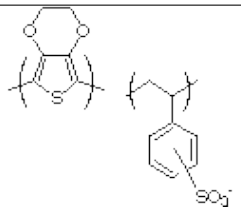
Semiconducting polymer	Physical properties	$\mu_{h,FET}$ cm^2/V.S	$\mu_{e,FET}$ cm^2/V.S	Color
F8 Poly(9,9-dioctyfluorene)	LUMO 2.4ev HOMO 5.7 ev	3×10^{-4}	5×10^{-3}	Blue
F8BT Poly(9,9-dioctylfluorene-alt-benzothiadiazole)	LUMO 3.3 eV HOMO 5.9 eV	NA	4×10^{-3}	Green



(a) F8 Chemichal structure. (b) F8BT Chemichal structure.

Figure 2.9: PLED active layer chemical structures.

Table 2.5: PEDOT:PSS properties and structure.

Polymer	Work Function	Chemichal Structure
PEDOT:PSS Poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate)	-5 eV	

Hole Blocking Layer (HBL)

PEDOT:PSS is used as a transparent, conductive polymer with high ductility in our OLED. PEDOT:PSS is spin coated on ITO surface for two reasons: first it reduces the hydrophobicty of the ITO's surfaces and second it creates smooth conductive surface on top the ITO. This polymer also acts as hole blocking layer (HBL) in out OLED. Summery of properties of the PEDOT:PSS is listed in Table.2.5.[16]

Table 2.6: Cathode material work function.

	Ca	TiO_2	Al	Ag	Au	Pd	ITO
Work Function (eV)	2.9	3.5	4.1	4.6	5.3	5.4	4.55

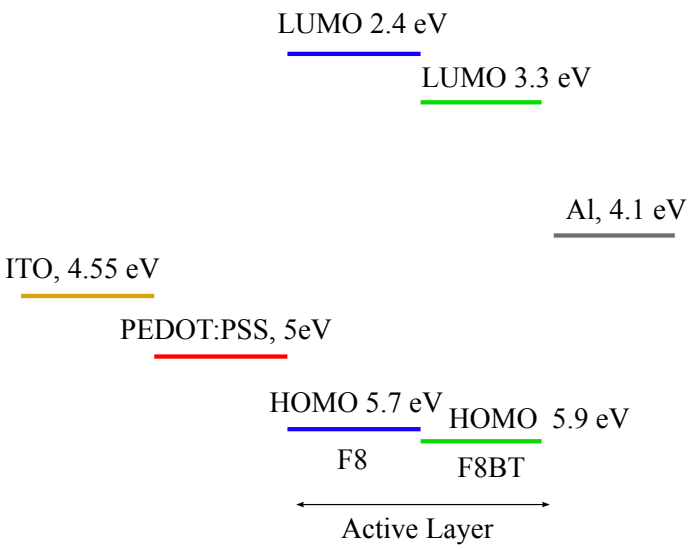


Figure 2.10: Fabricated OLED band structure.

Cathode layer

There are different materials which can be used as cathode layer. One of the main properties which cathode material should have is low work function. It is possible also to deposit two materials in combination to increase electron injection to the active layer e.g Ca plus Al gives sufficient electron injection to F8:F8BT blend polymer active layer. Table.2.6 lists different materials with their respective work function values.[17]

2.2.4 OLED Band Diagram

As shown in Fig.2.10, active layer composed of two different polymers with different HOMO and LUMO levels. As with most polymers hole transport is significantly better than electron transport which means that if we made an OLED from just F8 or F8BT then charge transport would be unbalanced. As such, the addition of the 5% F8BT to the F8, with its slightly lower HOMO, acts to trap charges and balance transport. It therefore also acts as an emissive center which is why the light is green (F8 emits in the blue, F8BT in the green). [18]

2.2.5 Life Time

Lifetime is one of the major obstacles to wide commercial applications for OLEDs. The main reasons for shorter life time are:

1. OLEDs have a thinner layer structure.
2. Organic materials are sensitive to moisture and oxygen.
3. Organic materials are not as robust as semiconductors due to larger vibration energy.[18]

Also degradation in OLEDs (mainly active layer related) can be categorized as three independent modes:

1. Dark spot formation: This phenomena occurs due to increasing non-emissive regions in OLED and gradually increases by time. Main reason for formation of dark spots is due to formation of bubbles in spin coating step of active layer.
2. Catastrophic failure (ITO spike): ITO spike occurs when the surface of the ITO is not uniform. After deposition of cathode there is a possibility that OLED is short circuited because of contact between Cathode and Anode.
3. Intrinsic degradation: Happens due to organic materials quality, which during time degrades and loses it chemical structure.

2.2.6 Fabrication

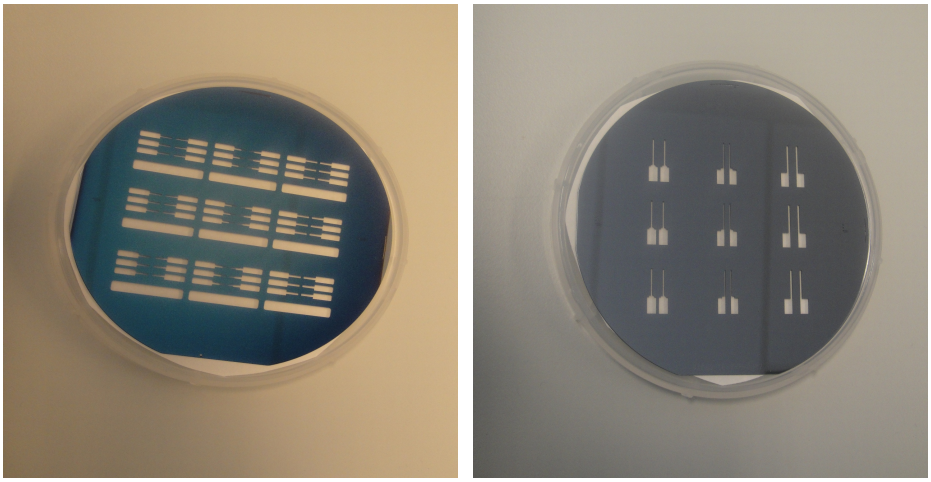
In this subsection, the steps which are taken for making a 6 pixel PMOLED device is explained in 5 steps.

Creating Anode and Cathode stripe's shadow mask:

For creating stripes for *Anode* and *Cathode* layers two shadow masks were created from Si wafer. First 6 μm oxide is grown with PECVD on both side of the Si wafer, then Si wafer is coated with photoresist. With a photomask which is patterned with anode layer, we pattern the Si wafer with contact aligner lithography machine, then we develop the photoresist. After, by using dry etching, we create open trench (wafer through) in patterned areas of the Si wafer (approximately 2 hours). We do the same steps for creating cathode shadow mask. Fig.2.11 shows the shadow masks for cathode and anode.

ITO Deposition

By using shadow mask for Anode we deposit 100 nm of Indium Tin Oxide (ITO) on a glass wafer. Shown in Fig.2.12.



(a) Anode Stripes (b) Cathode stripes

Figure 2.11: Shadow mask for Anode and Cathode.

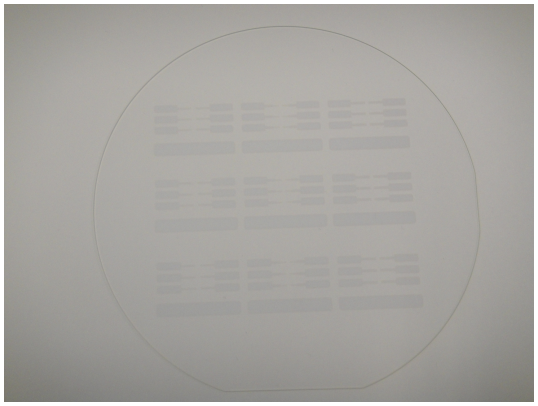


Figure 2.12: ITO Stripes on glass wafer.

PEDOT:PSS Spin Coating

For 30 seconds at 5000 RPM we spin coat the glass wafer with PEDOT:PSS. This will create a 40 nm thick layer of top of the ITO. After spin coating we clean the unwanted PEDOT:PSS from the surface. We place it on hot plate (150° C)until transferring to glovebox.

Active Layer Spin Coating

Because of the size of glass wafer (4 inches wafer), we have to spin coat the F8:F8BT fluid at higher RPM (> 3000), so it can cover most of the surface. After spin coating we clean the unwanted areas and then we place it on hot plate for 20 minutes at 80° C.

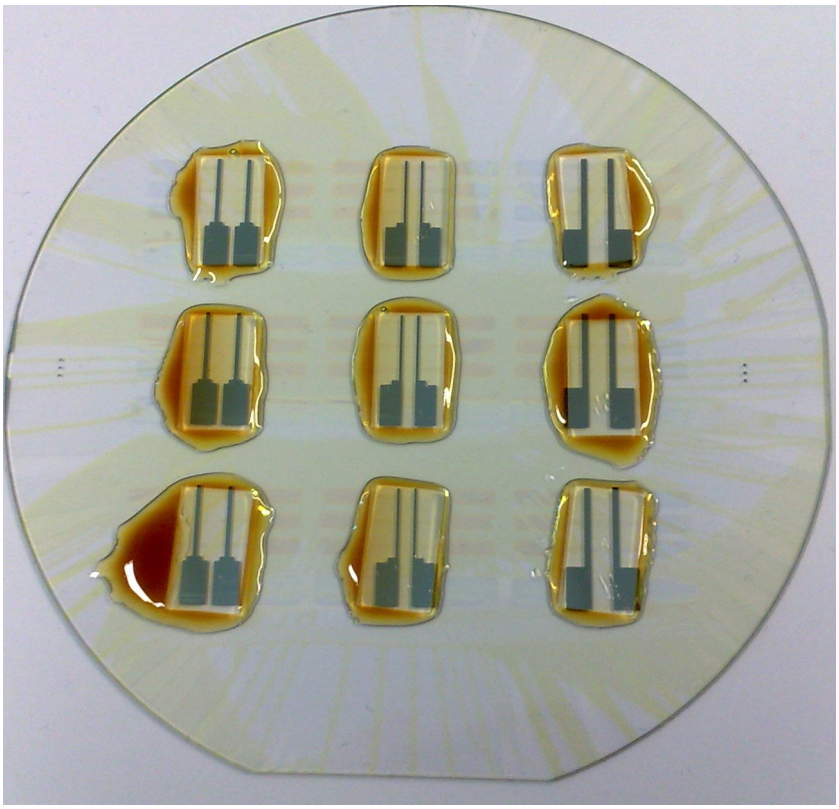


Figure 2.13: Fabricated OLEDs with encapsulation.

Cathode Deposition

For depositing cathode layer we use the cathode shadow mask and place it in position so that cathode stripes become perpendicular to the Anode stripes. Then we evaporate 100 nm of Al on the wafer and our cathode strips are formed.

Complete PLED fabrication flowchart is included in Appendix A.

2.2.7 Encapsulation

For protecting the active layer from moisture and oxygen and at the same time keeping the active area from deterioration, we encapsulate the pixel areas with glass cover and epoxy. This epoxy is gel like material which, under UV light, hardens and keeps the oxygen and moisture away from active layer. Encapsulation should be done inside the glovebox in presence of nitrogen gas (oxygen free environment).

Pixel Design 3

In this Chapter we will discuss the OLED display pixel types and their operation, then the modules which are developed for the simulation of OLED and afterward the Photodiodes will be discussed.

3.1 Pixel Types

The voltage programming method addresses the data voltages to the pixel circuit, while the current programming method addresses the current data to the pixel.

Although the voltage programmed pixel circuits have provided an evident performance of non-uniformity compensation, they still suffer from the I_{OLED} non-uniformity due to the other variation factors. One is the mobility variation and it cannot be memorized itself. It is rather difficult to compensate the mobility variation in the voltage modulation method.[13] On the other hand, it is almost possible to compensate the nonuniform mobility of TFT as well as the threshold voltage of TFT in the current programming method. The supply voltage drop phenomena is also a serious problem in the voltage programmed pixel circuits.[19]

The current programming method employs the current source unit from the data driver and addresses the current data to the pixel circuit in which the data current is memorized during the emission frame. It should be noted that the scheme can compensate both threshold voltage and mobility variations of TFTs. They are free from cross talk caused by the voltage drop in power supply line, while most of voltage modulation schemes suffer from it especially when we go to larger panels or higher brightness. In the pixel circuit, the data current (I_{Data}) determines a drive voltage (V_{GATE}) of the driving TFT to flow the OLED current with respect to I_{Data}.[20]

3.1.1 Pixel Architecture

2-Tr Pixel

The simplest AMOLED pixel which has pixel memory uses two transistors (NMOS) and one capacitor. One TFT (T2) drives the current for the OLED and another TFT

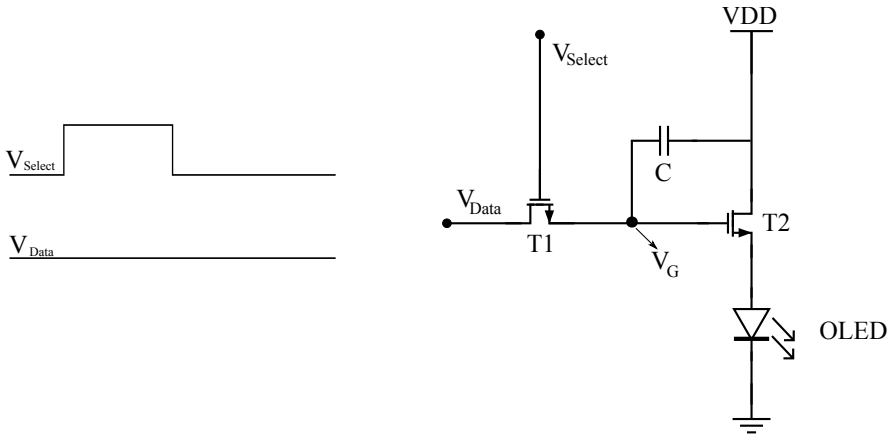


Figure 3.1: 2-Tr Voltage programmable pixel.

(T1) acts as a switch to sample and hold a voltage onto the storage capacitor C as shown in Fig. 3.1. During the raw select, T1 Turns on and transfers the voltage from V_{Data} (column electrode) to the gate of the driving transistor (T2). After addressing, T1 switches off and programed voltage (V_{Data}) is kept in on the gate of driving transistor T2 for the rest of the frame time. The role of Storage capacitance their is to prevent discharge of the T2 gate node but in meantime allows continuous driving of the OLED by driving transistor T2. when T2 is in saturation mode it behaves as a constant current source.[21] Current Supplied to OLED by T2 transistor is equal to I_d, which is given by:

$$I_d = K^{'} \mu_{FE} (V_{gs} - V_{th})^2$$

Where $K^{'}$is transistor size ratio (W/L) and gate oxide (C_{ox}), μ_{FE} is the filed effect mobility and V_{gs} and V_{th} are the gate source voltage and the threshold voltage of the transistor respectively. Because the T2 transistor's current which drives the OLED is proportional to $(V_{gs} - V_{th})^2$and μ_{FE}, any non-uniformity in the threshold voltage and mobility will result in pixel luminance variation.

6-Tr Pixel

The 6-Tr voltage programmable pixel consists of five NMOS switches (T1∼T5), a NMOS driving transistor (T6) and a storage capacitance (C) shown in Fig. 3.2. This Pixel is driven by three scan lines which are sequential. First storage capacitor is reset by V_{DD}. When SEL_{n-1} signal is high, T1 is switched on. At this stage a pre-charging voltage is applied to the gate of driving transistor T6 and T3. Second, V_{Data} voltage is applied to the source of T3 through T4 and the threshold voltage of T3 (V_{th-T3}) is stored in the gate of T3. When SEL_n is high T2 and T4 are switched on. At this

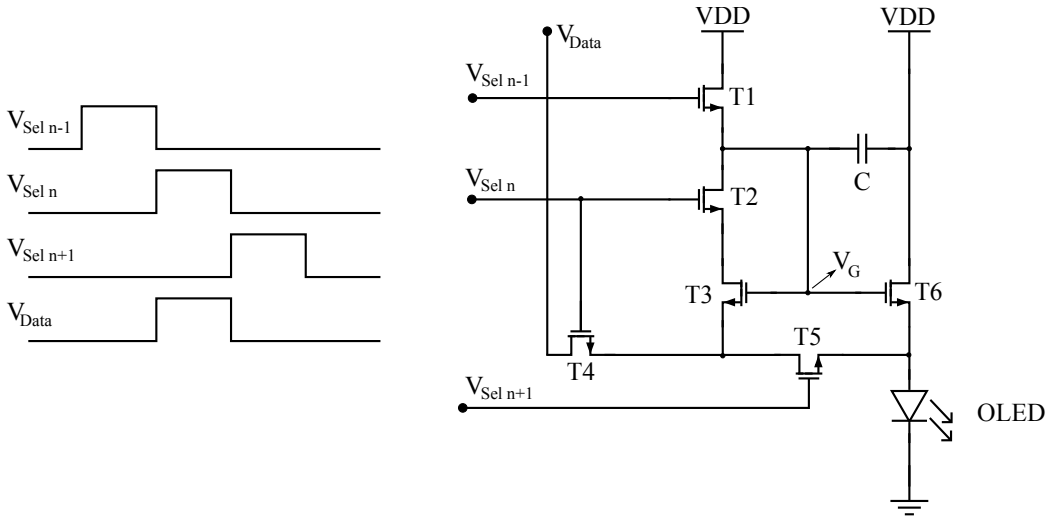


Figure 3.2: 6-Tr Voltage programmable pixel.

time the gate voltage of T3 will discharge through T3 and T4 until T3 is switched off so that Storage capacitance stores ($V_{th-T3} + V_{Data}$). Lastly when $SEL_{n+1}$is high then T5 is switched on. At this moment the source of T3 and T6 (driving transistor) reach the same voltage. Two transistors,T3 and T6 have the same gate voltages and source voltages so both have the same deterioration characteristics. The threshold voltage of T3 and T6 will shift equally. As a result threshold variation of driving transistor can be compensated by threshold variation of T3.[22] The main advantage of this pixel is that no additional control signal is needed.

4-Tr Pixel

The 4-Tr current programmable pixel consists of three NMOS switches (T1,T2 and T4), a driving transistor (T3) and cascade capacitors (C1 and C2) shown in Fig. 3.3. When V_{Scan} is high T1 and T2 is switched on and I_{Data} passes through T1 and T3 to OLED meanwhile T4 remaining switched off. When pixel changes from on state to off state, V_{Scan} switches off T1 and T2 meanwhile T4 are switched on by $V_{Control}$. Since the gate voltage of the T3 (driving transistor) is reduced to off state, scale down current with ratio of cascaded capacitor will flow through OLED.[23] The main advantage of this pixel is that by accurately setting the ration of the C2 and C1 we can achieve good current scaling for driving the OLED.

3.2 OLED Module

For simulation purpose a linear module has been made from a OLED I-V graph. This module consists of DC power supply, ideal diodes, resistors and OLED parasitic capacitance. As it shown in Fig. 3.4, the Value of the R1∼R5 can be calculated from I-V

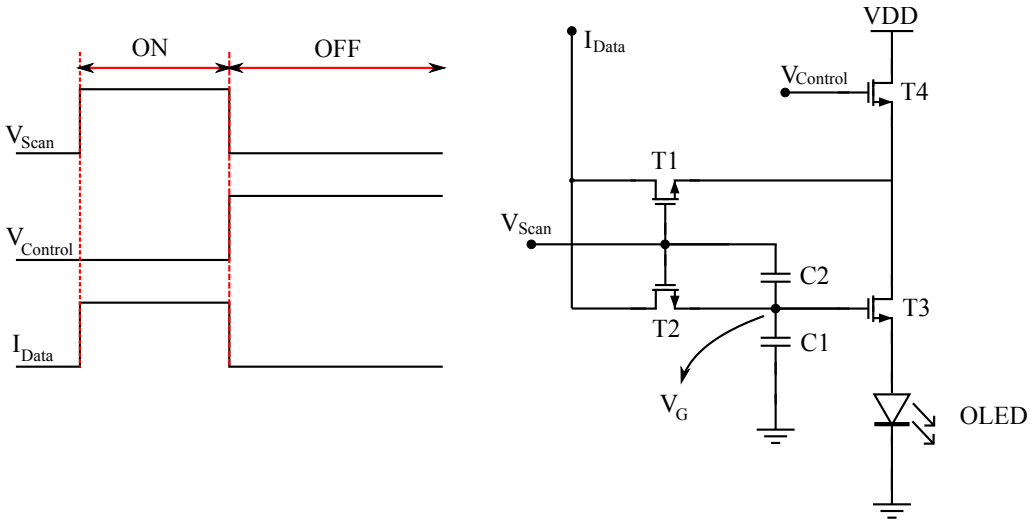


Figure 3.3: 4-Tr Current programmable pixel.

graph and by using the following equations we can calculate value of the R'1∼R'5. After doing simulation to create a match characteristic graph, some modification is made to resistor values and power supplies.

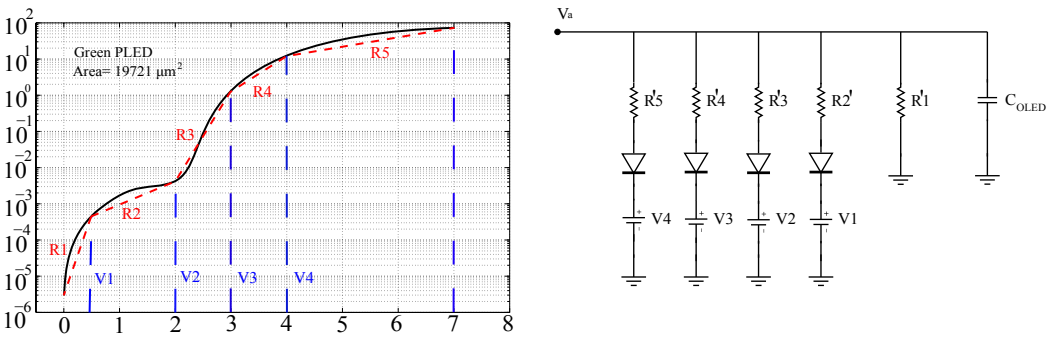


Figure 3.4: OLED Module.

Mathematical derivation from I-V graph.

$$\begin{cases} R1 \parallel R'2 = R2 & \Rightarrow 1/R'2 = 1/R2 - 1/R1 \\ R1 \parallel R'2 \parallel R'3 = R3 & \Rightarrow 1/R'3 = 1/R3 - 1/R2 \\ R1 \parallel R'2 \parallel R'3 \parallel R'4 = R4 & \Rightarrow 1/R'4 = 1/R4 - 1/R3 \\ R1 \parallel R'2 \parallel R'3 \parallel R'4 \parallel R'5 = R5 & \Rightarrow 1/R'5 = 1/R5 - 1/R4 \end{cases}$$

$$\Rightarrow \begin{cases} R5 = 0.02055 & \Omega \\ R4 = 0.06248 & \Omega \\ R3 = 0.502 & \Omega \\ R2 = 681.2 & \Omega \\ R1 = 718.39 & \Omega \end{cases}$$

$$V1 = 0.2V, V2 = 1.3V, V3 = 2.3V, V4 = 3.3V$$

It should be noted that this I-V graphs is for OLED area of 19721 $\mu m^2$and I-V characteristics is directly related to the area [23], thus our pixels are designed for real life pixel sizes of 300 $\times$ 300 μm^2. For downsizing the area in this module the values of R'1 R'5 is divided by the new area (300 $\times$ 300 μm^2).

$$R'' = R'x/Area$$

Which $x = 1..5$. By applying voltage source at node V_a from 1-7 Volts, following I-V characteristic has been achieved (Fig. 3.5).

3.3 Simulation

For Simulation of the device Agilent Advanced Design System is used with BSIM models of SG-TFT.[24]

3.3.1 2-Tr Pixel Simulation

For the transient simulation of the 2-Tr voltage programmable pixel; 5 volts have been applied to V_{Data} and V_{DD} then a voltage pulse is applied to V_{Select}. Simulation parameters and transistors sizes of 2-Tr pixel are listed in Table 3.1.

As shown in Fig.3.6, by applying 5 volts V_{Data} and 5V of pulse (V_{Select}), T1 transistor switches on and the charge is stored at the gate of T2 (V_G) which during the time the voltage variation is very low as shown in Fig.3.6c. Fig.3.6d demonstrates the I-V characteristics of the OLED. From I-V graph is evident that 2-Tr pixel can drive the OLED with current of up to 10μA and voltage of up to 4.7V.

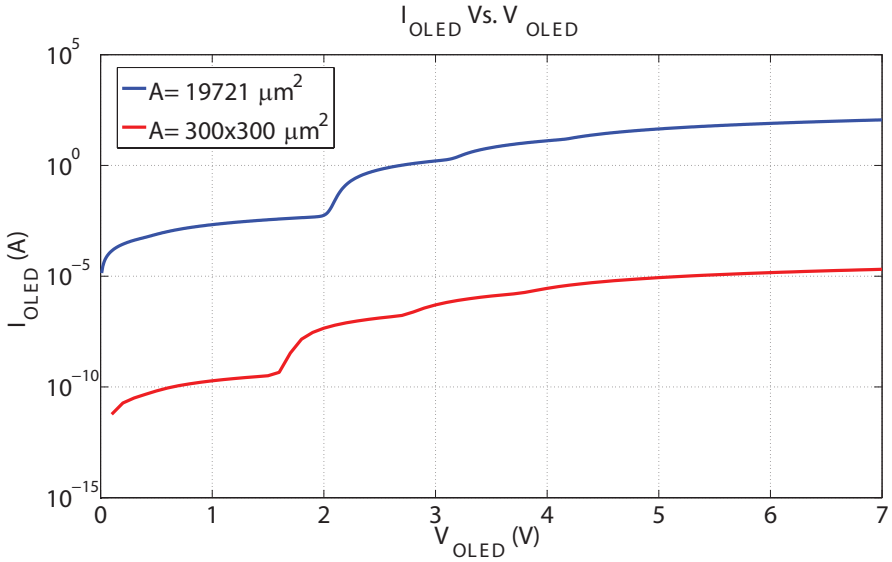


Figure 3.5: I-V characteristic of modules OLED.

Table 3.1: 2-Tr simulation parameters.

	V_{Low}	V_{High}	T_{Fall}	T_{Rise}	Width	Periode
V_{Select}	0V	5V	10ns	10ns	330µs	33330µs

(a)

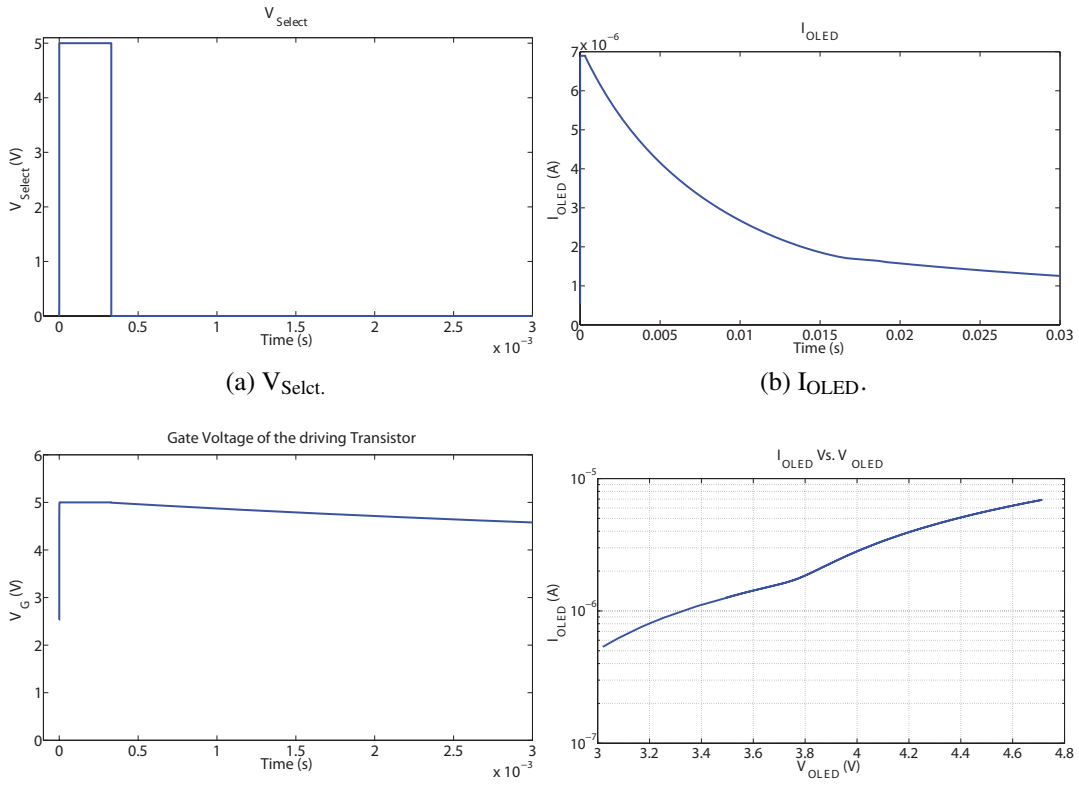
	W	L
NMOS(T1)	8µm	2µm
NMOS(T2)	28µm	2µm

(b)

3.3.2 6-Tr Pixel Simulation

For transient simulation of 6-Tr voltage programmable pixel; 10V has been applied to V_{DD} and SEL_{n-1} ,SEL_n,$SEL_{n+1}$and V_{Data} parameters and transistor sizes are listed in Table 3.2.

As shown in Fig.3.7, when SEL_{n-1} is high (10V) the gate of driving transistor (T6) is pre-charged (5V) and in the second stage when SEL_n is high then the gate voltage (V_G) of driving transistor is increases to 10V which is shown in Fig.3.7c. From I-V graph of OLED is evident that 6-Tr voltage programmable Pixel is capable of driving OLED with current of up to 20µA and voltage of 5.6V as shown in Fig.3.7e.



(a) $V_{Selct.}$

(b) I_{OLED}.

(c) Gate voltage of driving transistor.

(d) I-V characteristics of OLED.

Figure 3.6: 2-Tr Voltage programmable Pixel simulation results.

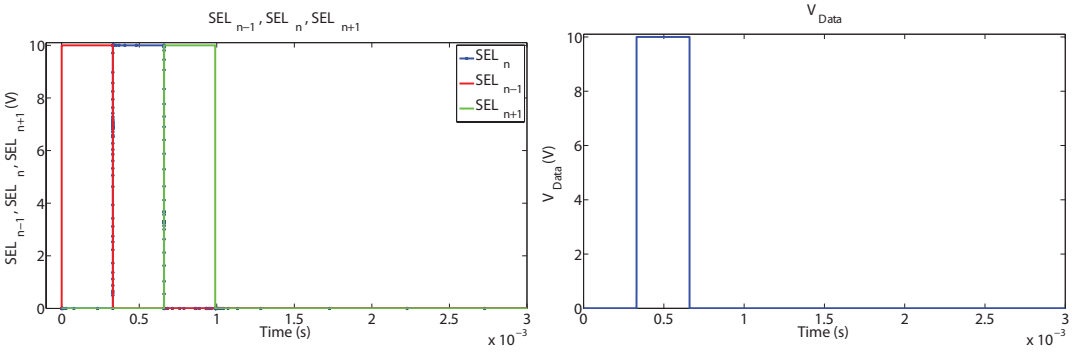
3.3.3 4-Tr Pixel Simulation

For transient simulation of 4-Tr current programmable pixel; 5V has been applied to $V_{DD}$and for V_{Scan},$V_{Control}$ and I_{Data}following parameters in Table 3.3 where used:

As shown in Fig.3.8, when the V_{Scan} is high the current (I_{Data}) passes through the T1 and T2 and to the T3 and when the $V_{Control}$ is high then the T3 is getting turned off. It is evident that by controlling the size of T4 and value of $V_{Control}$, it is possible to control how fast the T3 turns off. From I-V graph is evident that 4-Tr current programmable pixel is capable of driving OLED with a current up to 1μA and voltage of 3.6V.

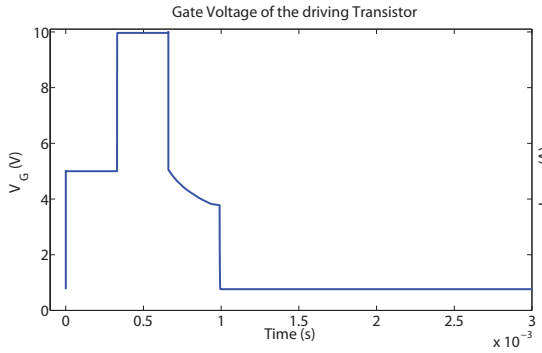
3.4 Photodiode

High responsivity, high quantum efficiency, lower dark current and linearity are the most important parameters for the photodiodes. Lateral photodiodes are not limited by the absorption length of the incident light since the carrier path and light direction

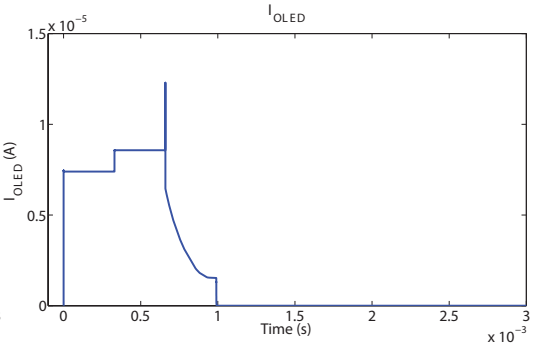


(a) SEL_{n-1} ,SEL_n,SEL_{n+1}.

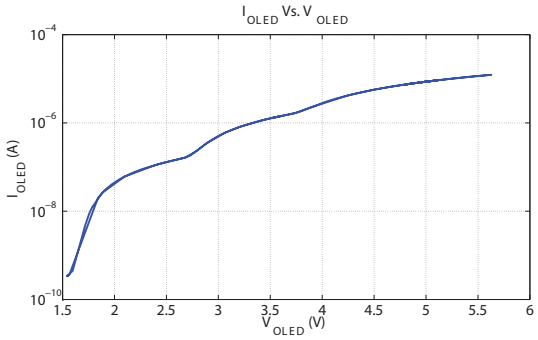
(b) V_{Data}



(c) Gate voltage of driving transistor (T6)

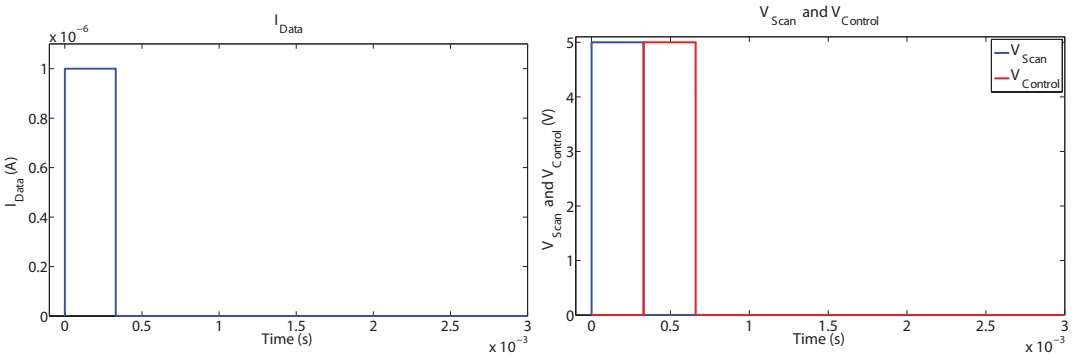


(d) OLED Current



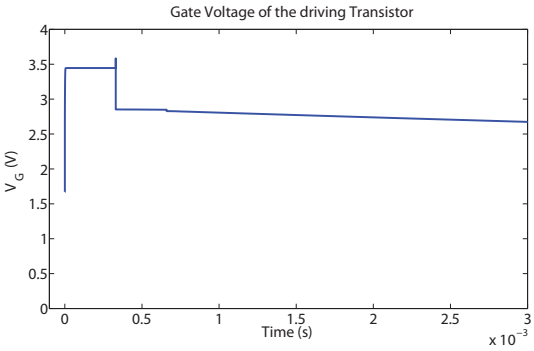
(e) I-V characteristics of OLED

Figure 3.7: 6Tr- voltage programmable pixel simulation results.

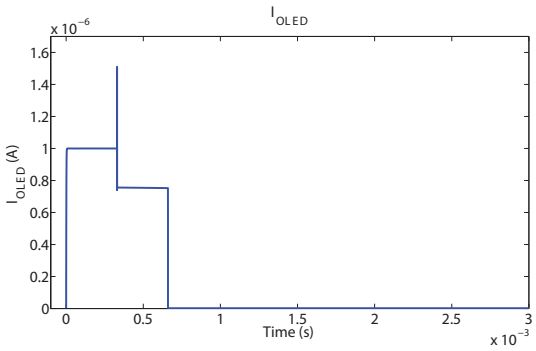


(a) I_{Data}.

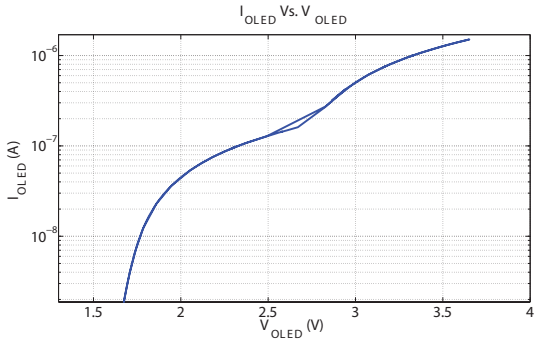
(b) $V_{Control}$and V_{Scan}



(c) Gate Voltage of driveing Transistor (T3).



(d) I_{OLED}



(e) I-V Characteristics of OLED

Figure 3.8: 4-tr current programmable pixel simulation.

Table 3.2: 6-Tr simulation parameters.

	V_{Low}	V_{High}	T_{Fall}	T_{Rise}	Width	Periode	Delay
SEL_{n-1}	0V	10V	10ns	10ns	330µs	33330µs	0s
SEL_n	0V	10V	10ns	10ns	330µs	33330µs	330µs
SEL_{n+1}	0V	10V	10ns	10ns	330µs	33330µs	660µs
V_{Data}	0V	10V	10ns	10ns	330µs	33330µs	330µs

(a)

	NMOS(T1)	NMOS(T2)	NMOS(T3)	NMOS(T4)	NMOS(T5)	NMOS(T6)
W	15µm	15µm	30µm	15µm	15µm	30µm
L	1.5µm	1.5µm	1.5µm	1.5µm	1.5µm	1.5µm

(b)

Table 3.3: 4-Tr simulation parameter.

	V_{Low}	V_{High}	T_{Fall}	T_{Rise}	Width	Periode	Delay
$V_{Control}$	0V	10V	50ns	50ns	330µs	33330µs	330µs
V_{Scan}	0V	10V	50ns	50ns	330µs	33330µs	0s
I_{Data}	0A	1µA	1ns	1ns	330µs	33330µs	0s

(a)

	NMOS(T1)	NMOS(T2)	NMOS(T3)	NMOS(T4)
W	7.6µm	7.6µm	2.2µm	7.6µm
L	1.5µm	1.5µm	1.5µm	1.5µm

(b)

are different. It means lateral photodiodes have high responsivity and are suitable for high speed and high frequency applications. [25] Single grain silicon obtained by µ-Czochralski process can be used to make high speed, low power and low dark current lateral PIN photodiodes. There are several advantages of using lateral PIN photodiodes. First of all, the photodiode can easily be integrated with thin film transistors (TFTs). Secondly the lateral PIN photodiodes are not limited by the absorption length of the incident light since the carrier path and light direction are different.[26] Different between vertical and lateral photodiode is shown in Fig3.9.

In our design an array of photodiodes was used under the ITO layer. As it is mentioned, the pixel which we are designing is bottom emitting pixel and the reflective cathode is on top layer. Based on reflection of the light from cathode, photodiodes will absorb some of the light and will be able to generate voltage.

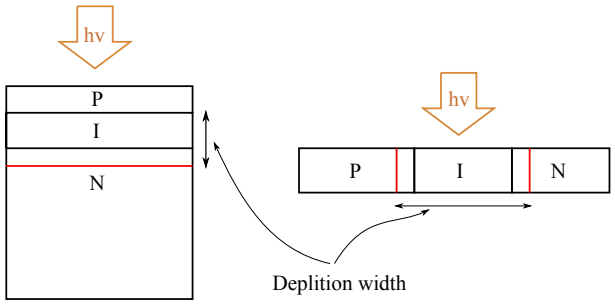
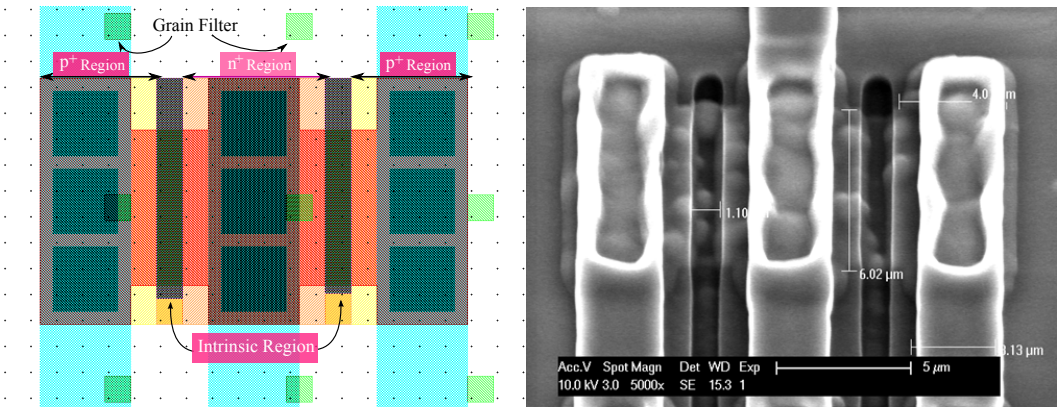


Figure 3.9: Vertical Photodiode Vs. Lateral Photodiode.

3.4.1 Photodiode Layout

As shown in Fig.3.10, we designed parallel photodiodes in an array. For instance for 306 parallel diodes totally we have a photodiode with 1896μm^2 (intrinsic) area . In designing photodiodes, intrinsic region never meets grain boundaries. Grain boundaries can deteriorate the efficiency and cause degradation of devices.



(a) Photodiode layout. (b) SEM Picture of the Photodiode.

Figure 3.10: Single Grain PiN diode.

Single grain PIN photodiode process step is same as Single Grain TFT, with one exception which after doping the Al gate is removed and replaced with 300 nm of oxide ,which forms the intrensic region.

3.5 Readout

A circuit has been designed as a readout device for photodiode arrays. This readout circuit consists of three transistors as shown in Fig.3.11.

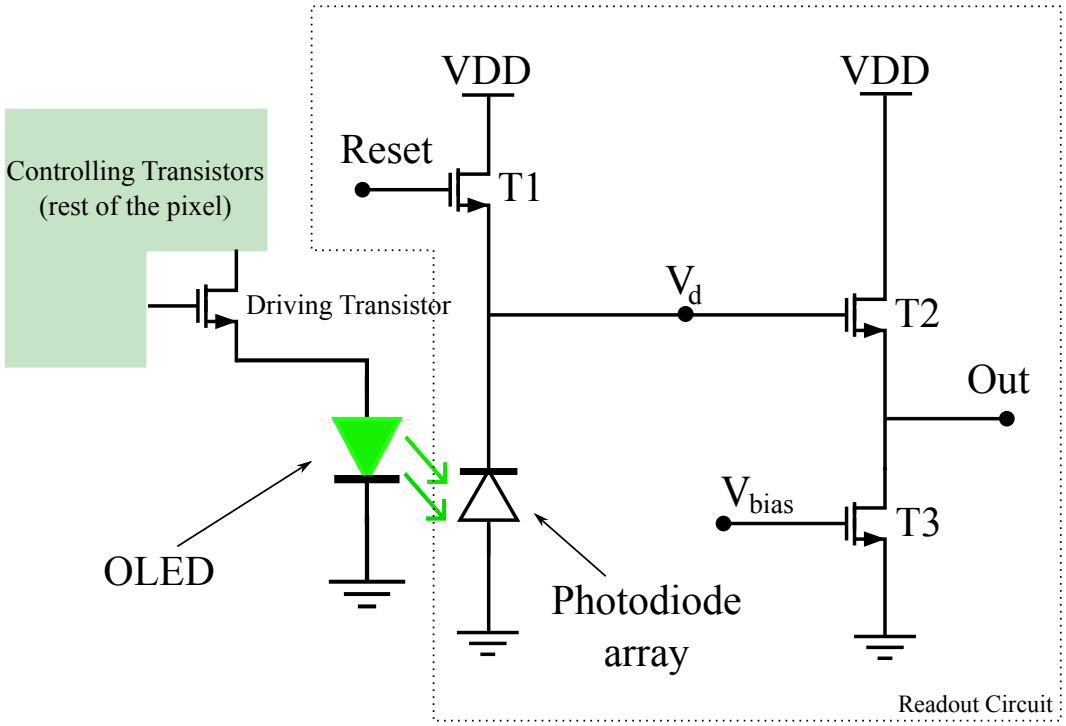


Figure 3.11: Photodiode readout circuit.

When negative voltage is applied to V_{Bias}, we can readout the current at output, mathematical derivation below shows that the sensitivity of device is dependent on $g_m$of the T2 transistor. also by applying positive voltage to V_{Bias}we can read the voltage at output.

$$I = I_0 \exp^{\frac{-V_d}{V_T}}$$

$$V_d = V_T \ln \frac{I_0}{I}$$

$$I_{out} = g_m V_T \ln \frac{I_0}{I_d}$$

Where $I_0$is saturation current of diode, $V_d, I_d$are voltage and current of Photodiode respectively. $g_m$is the gain of T2 transistorand V_T is thermal voltage.

3.6 Layout

For realizing pixels on wafer, layout of pixel were designed as shown in Fig.3.12. This Figure shows the layout for 6-Tr voltage programmable pixel, OLED cathode, photodiode array, readout circuit which are surrounded with PADs.

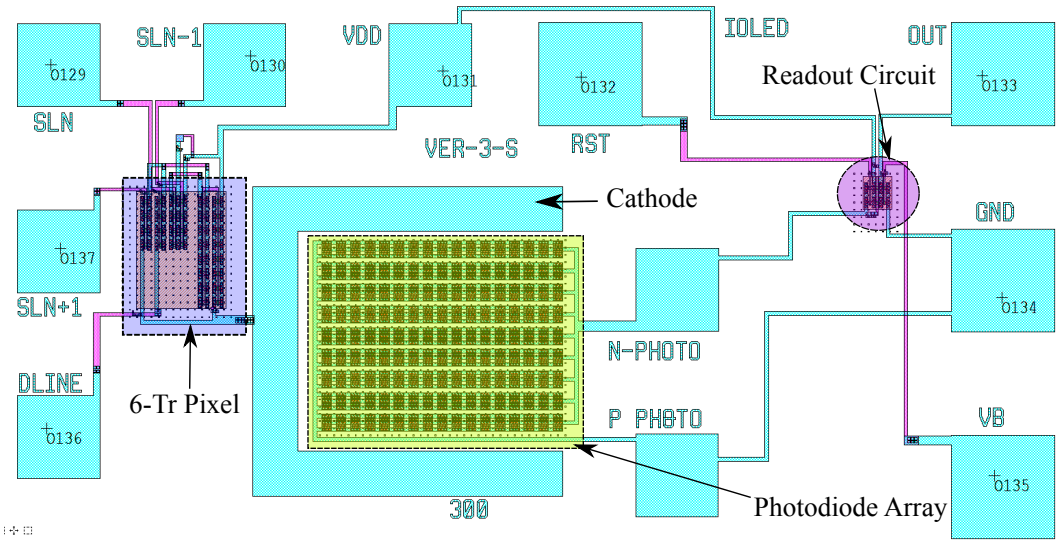


Figure 3.12: layout

3.7 Packaging

During design it was noticed that a number of the PADS, which are needed for Cascade probe station's needles to make contact with the circuit nodes, are more than available probe needles (maximum 7 available) so two pixels were modified for package fitting. For wire bonding bigger PADS had to be realized in four sides of the die and an extra metal layer have been used for interconnect. Packaged chip can be seen in Fig.3.13.

3.8 Conclusion

In this chapter different types of pixels have been investigated. Both Voltage programmable and Current Programmable have good performance with single grain TFT technology in comparison to other technologies such as a-Si or Poly-Si which have bulky designs and high power consumption, such as 20V and above. Related to reference design, pixels which are made with Single Grain TFT have 20% to 50% smaller size thus they can drive the OLED with almost the same or higher current.

Also by using lateral PIN diode array under the Anode (Transparent) it is possible to read the light intensity or just simply generate Voltage or current by using readout circuit so it can be feedback to the circuit for some compensation.

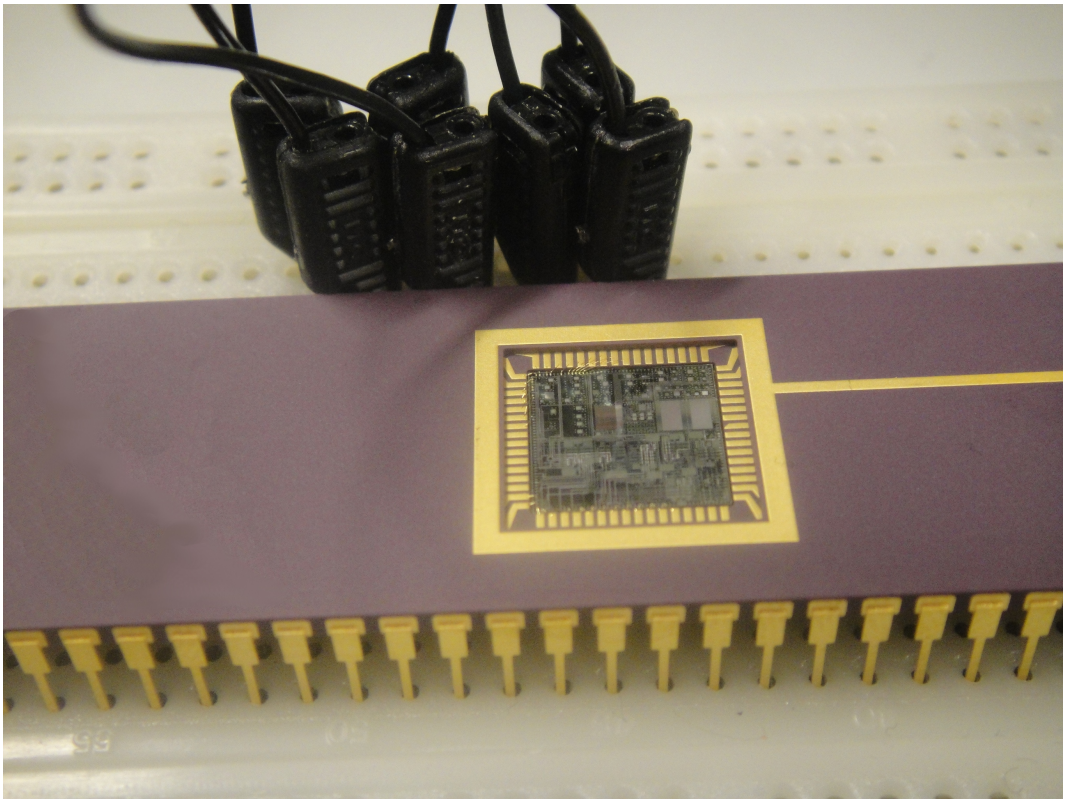


Figure 3.13: Packaged chip

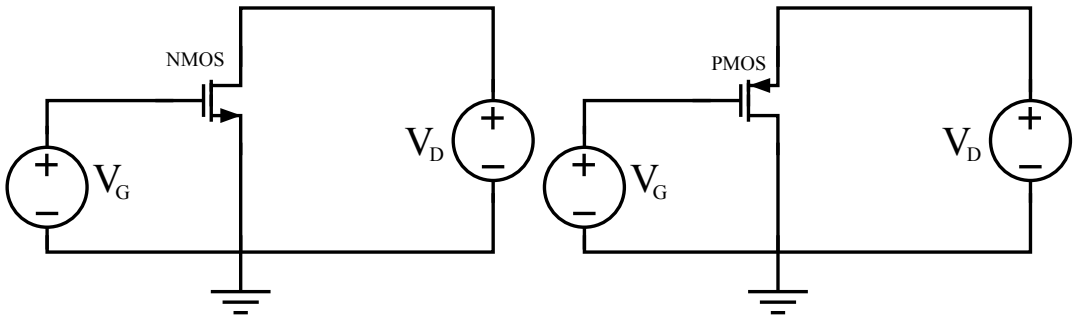
Measurement 4

In previous chapter ,Chapter 3, simulation of the devices are done based on Single Grain TFT device models in EDA tools namely Agilent Advance Design System. In this chapter, all the simulated and fabricated devices are measured and characterized.

4.1 Test Structure measurements

In Chapter 3 we discussed about pixel designs based on Single Grain TFT, now we will analyze the quality of this type of transistor by measuring the I_D-V_{GS} and I_D-V_{DS}curve. These curves can provide information about the transistors, such as the subthreshold voltage swing, the leakage current, the on-current, the threshold voltage, the mobility of the transistor, and the current and voltage characteristics of the transistor when different gate voltages are applied. Ultimately we want to compare the SG-TFT with different transistors to obtain a better knowledge of the quality of such a transistor.

In the fabricated wafers a few NMOS and PMOS structures are made for testing and characterization purpose. Fig. 4.1 demonstrates the configuration used for the measuring of the I-V characteristic of the NMOS and PMOS.



(a) NMOS measurement setup. (b) PMOS measurement setup.

Figure 4.1: NMOS and PMOS measurement setup.

Field Effect Mobility

The mobility of a transistor, describes the average drift velocity of a carrier due to an electric field, which is expressed as cm²/Vs and has the symbol μ. Since the mobility determines the speed of the transistor, a transistor with higher mobility is considered better transistor. This parameter can be calculated from the formula for the drain current, when the transistor is in the linear region. Field effect mobility is calculated from I_D-V_{GS} curve.

$$I_D = \mu C_{ox} \frac{W}{L} \left(V_{GS} - V_{th} - \frac{V_{DS}}{2} \right) V_{DS}$$

$$g_m = \frac{\delta I_D}{\delta V_{GS}} = \mu C_{ox} \frac{W}{L} V_{DS}$$

$$\mu = \frac{\delta I_D}{\delta V_{GS}} \frac{1}{C_{ox}.V_{DS}} \frac{L}{W}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

Where I_D is the drain current, C_{ox} is the oxide capacitance which is inversely proportional to the thickness of the gate oxide $t_{ox} = 30 \times 10^{-7} cm$, $\varepsilon_{ox}$is the oxide permittivity, W and L are the width and length of the depletion region of the transistor respectively and V_{th} is the threshold voltage of the transistor.

I_{ON} and I_{OFF} Current

It is important to know how much current is "leaking" when the V_{GS} is below the threshold voltage. A transistor is considered good if it has a low leakage current/off-current. This current is defined as the minimum current in the I_D-V_{GS} curve.

How much current is running through the transistor when it is switched on is important too. There has to be a significant difference between on-current and off-current. This ratio would also describe in a lesser sense the speed of the transistor.

Subthreshold Voltage Swing

When a transistor is switched on, a voltage at the gate is applied crossing the threshold voltage. The speed at which it turns on when crossing this threshold voltage is important to the quality of a transistor. A low subthreshold swing accounts for a fast transition from the off-current to the on-current. Optimally the transistor is *off* when voltage is applied at the gate that is below the threshold voltage, and *on* when the voltage goes above the threshold voltage. Subthreshold voltage can be calculated from I_D-V_{GS} curve from the slope of the I_{ON} and I_{OFF}.

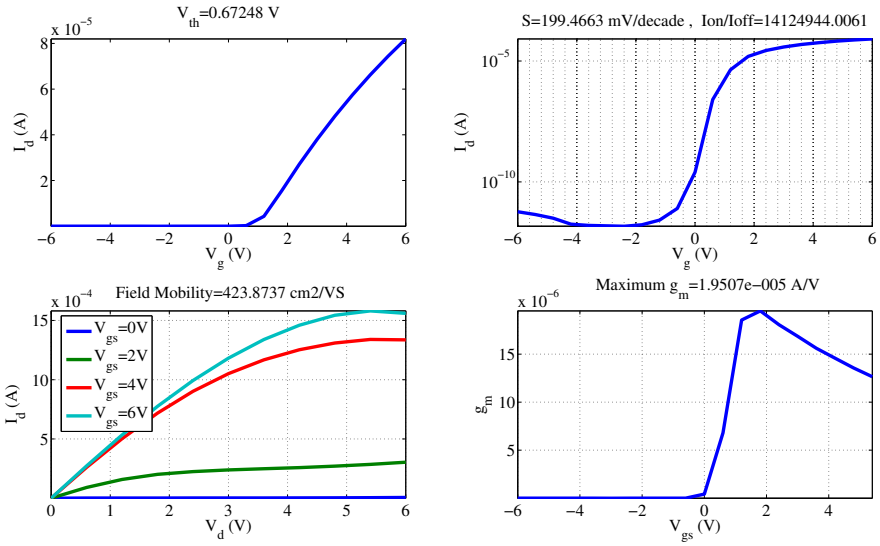


Figure 4.2: NMOS Parameters

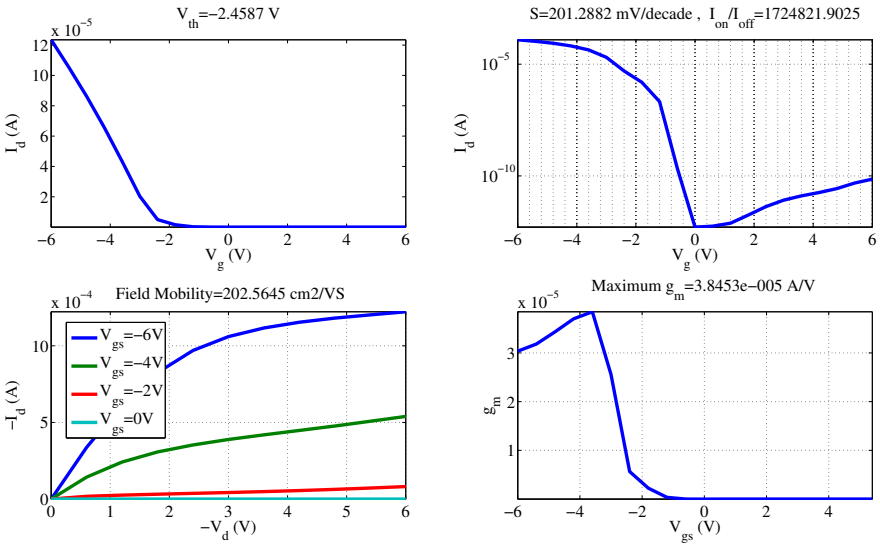
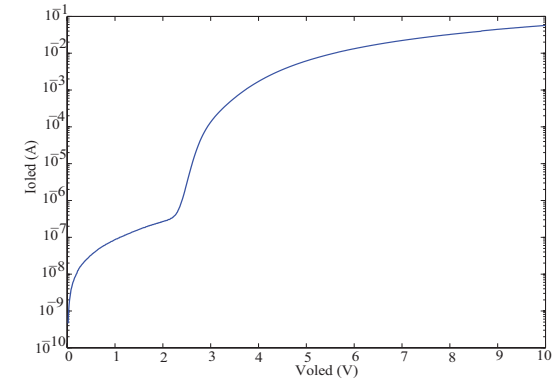


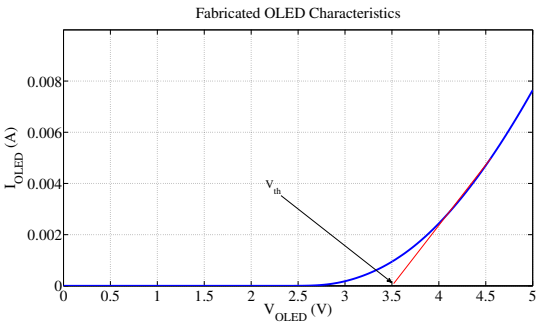
Figure 4.3: PMOS Parameters

Threshold Voltage

This parameter defines at what gate voltage the transistor is switched on and off. Preferably this voltage should be between 0V and 1V for an NMOS and between -2.5V and 0V for a PMOS, so that low gate to source voltages can drive the transistor. To compute this parameter, we need again the I_D-V_{GS} curve.



(a) Logarithmic I-V



(b) Linear I-V

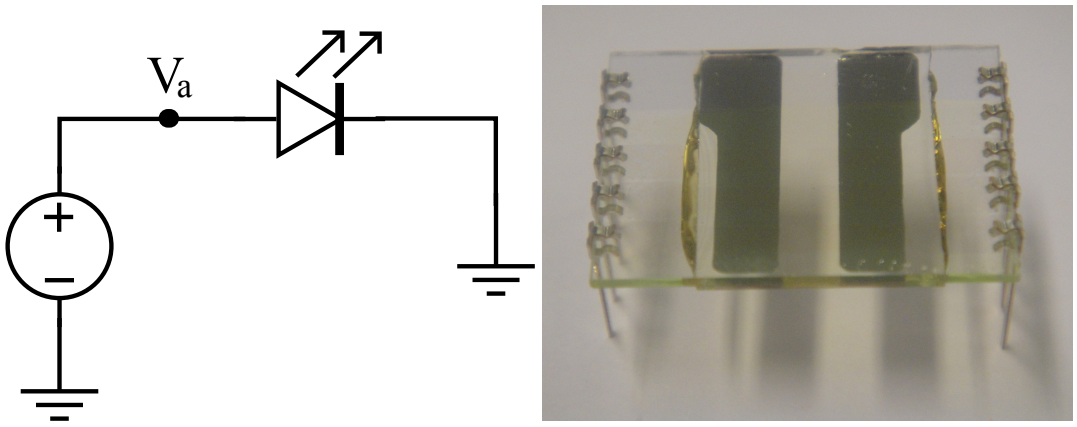
Figure 4.4: I-V characteristic of fabricated OLED

4.2 OLED Measurements

4.2.1 I-V Characterization

For getting the I-V characteristics of the fabricated OLED , Voltage at a node (Anode) is swept from 0V to 10V and cathode was grounded, as shown in Fig.4.5a. It should be noted that this I-V characterization graph is for OLED area of 1.5×3=4.5 mm^2. Threshold voltage of fabricated OLED is 3.5V as seen in Fig.4.4b.

During measurement it was noticed that driving the OLED with supply voltage over 6.5 V causes some dark spots on the surface and if OLED is driven for longer time with higher voltage (>8 V) then device fails. This is caused by some impurities in PEDOT:PSS; which is a very thin layer under the Organic material and above ITO layer according to supplier. Another effect which was noticed during measurement was heat generation at 10V applied voltage. It took just 3 minutes to complete destruction of the single OLED pixel.



(a) OLED measurement testbench. (b) 6 pixel fabricated OLED.

Figure 4.5: OLED measurement setup.

Table 4.1: Colorimetry and Photometry values for fabricated OLED

	Dominant Wavelength (λ)	FWHM[1]	Color Coordinate	Illuminance
OLED	557.511nm	70.970nm	x=0.353 y=0.616	7215.8 Lux

	Luminous Intensity (Initial)	Luminous Intensity (After 10 min with V_a=6.5 V)
OLED	100 cd/m^2	34 cd/m^2

4.2.2 Optical Measurement

For measuring optical properties of fabricated OLED (Fig.4.5b); a spectrometer (Avantes AvaSpec 2048-UA-50) is used. This device is capable of measuring light from 200 to 1100 nm spectrum. By using this spectrometer few measurements were done for measuring light intensity, color coordinate, dominant wave length, color coordinates and FWHM (Full Width at Half Max). Fig.4.6 demonstrates light intensity of fabricated OLED for different applied voltage (V_a) for OLED.

4.2.3 Color

CIE color coordinate is one of the major factor in display technology. As shown in Fig.4.7, with the primary RGB colors we can create a wide spectrum of colors simply by mixing these three colors. The more these primary colors create a wide triangle to cover most of the human eye's recognizable color spectrum, the better. Table.4.1 summarizes some of the colorimetry and photometry values of the fabricated OLED.

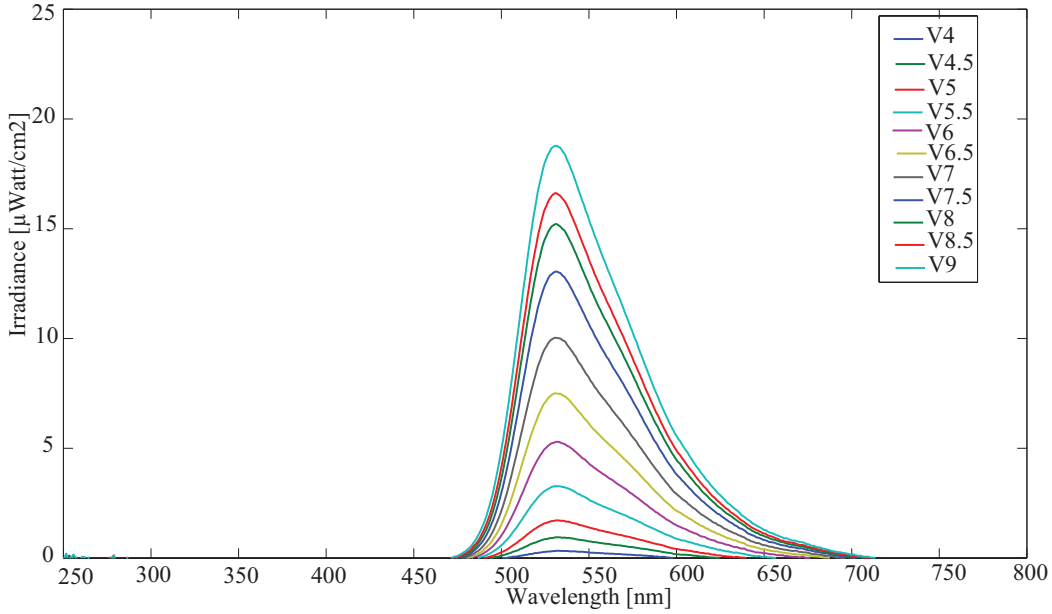


Figure 4.6: Irradiance measurement of the fabricated OLED at different applied voltage (V_a)

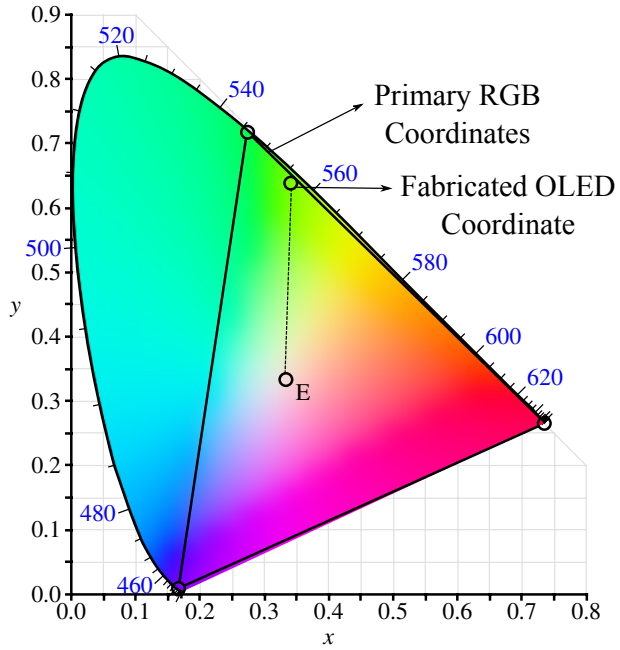


Figure 4.7: Gamut of the CIE RGB primaries and location of primaries on the CIE 1931 xy chromaticity diagram. Vs. Gamut of the fabricated OLED

4.3 Pixel Measurements

For measuring OLED pixels, Cascade 34 probe station with combination of HP DC parameter analyzer and Agilent ICCAP 2009 tool was used. Fabricated OLED then was connected to the parameter analyzer in parallel with the relevant nodes for the cathode and anode in the wafer (pixel).

4.3.1 2-Tr Voltage programmable pixel

For measuring the 2-Tr voltage programmable OLED pixel following measurement setup used as shown in Fig.4.8e. At this setup, 5 V constant DC source was supplied to V_{Data} and V_{DD}.Then V_{Select} is swept from 0 V to 5 V with steps of 500 mV. By these settings, pixel is delivering maximum $V_{OLED}$of 4.4 V and $I_{OLED}$of 3.7×10^{-3}A as shown in Fig.4.9.

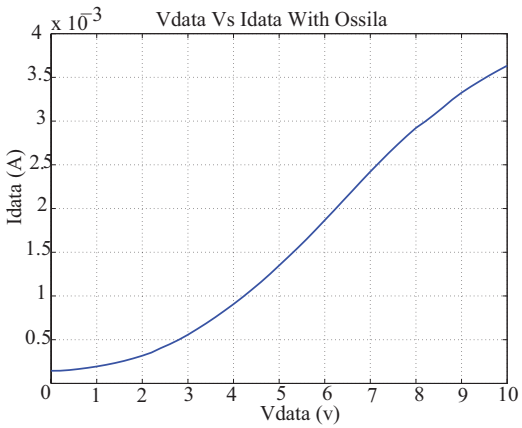
4.3.2 6-Tr Voltage programmable pixel

Measuring 6-Tr voltage programmable pixel was complicated due to number of the input nodes needed (limitation with Cascade probe stations needles which are only 6). Fig.4.9c demonstrates measurement setup which was used for measuring the 6-Tr OLED pixel. Due to number of needle limitation V_{Seln-1} and V_{Seln}were connected to same node in probe station and eventually to the parameter analyzer and swept from 0 V to 10 V with steps of 1.25 V. *Sweeping order* of this node is set to *One* (Loop one). $V_{Sel\ n+1}$then swept from 0 V to 10 V with steps of 1.25 V. *Sweeping order* of this node is set to *Two* (Loop two). Eventually $V_{Data}$is swept from 0 V to 10 V with steps of 500 mV. *Sweeping order* of this node is set *three* (Loop three). Meanwhile V_{DD} is supplied with constant 10 V DC source.

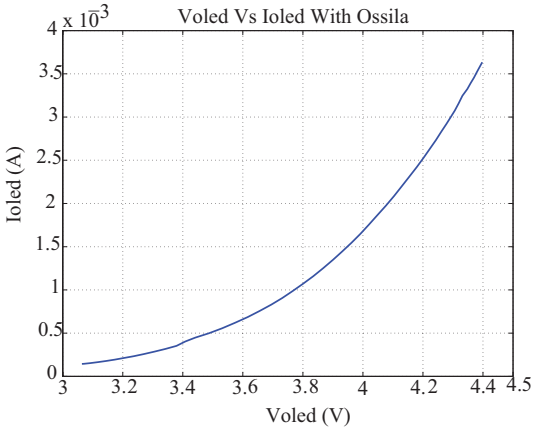
I-V characteristics of the OLED is shown in Fig.4.9b. The results confirms that 6-Tr pixel can drive the OLED with V_{OLED} of 3.45 V and I_{OLED} of 9×10^{-4}A.

4.3.3 4-Tr Current programmable pixel

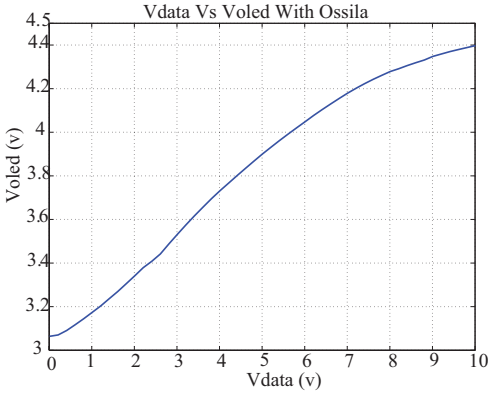
Because all the measurements are done with DC parameter analyzer, there weren't any possibility to feed a current pulse to I_{Data} as an input, even by using RC coupling with help of function generator. Using cables to feed any kind of pulse with amplitude less than 500 μA was heavily distorted because of the length of the cables and their resistance and capacitance. For measurement of the 4-Tr current programmable pixel I_{Data} was swept from 0V to 10 μA with steps of 1 μA; V_{Scan} and $V_{Control}$ is swept from 0 V to 5 V with steps of 0.5 V as a inner loop sweep, so for each step of I_{Data}; V_{Scan} and $V_{Control}$ goes from 0 V to 5 V. When V_{Scan} and $V_{Control}$ reaches to 2.5-3 volts, T1, T2, T4 turns on and depending on the I_{Data} value the OLED emits light. Unfortunately after the first loop which charges the C1 and C2, there is a charge spark which makes the parameter analyzer to control the current (namely gives compliance error). So after



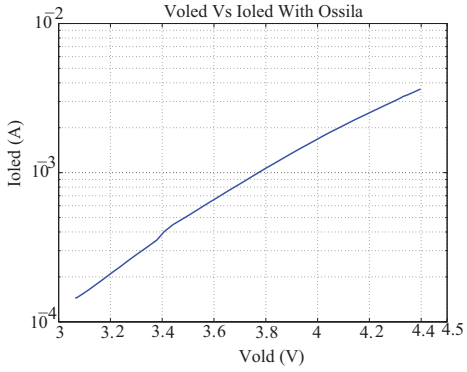
(a)



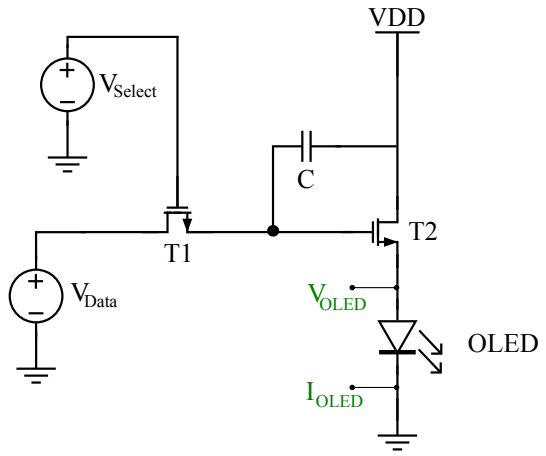
(b)



(c)

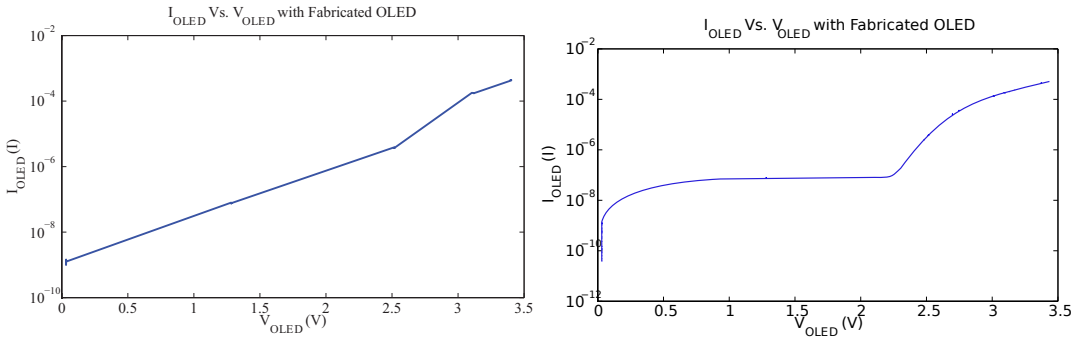


(d)



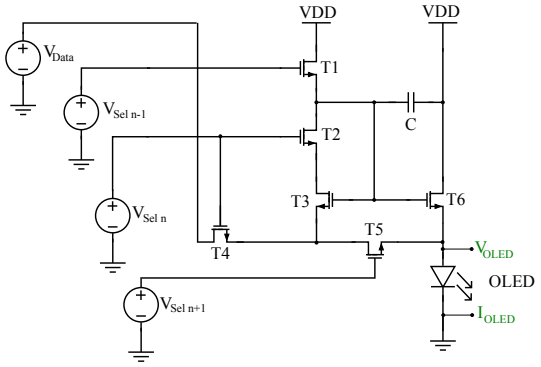
(e) 2-Tr Voltage programmable pixel measurement testbench.

Figure 4.8: 2-Tr pixel measurement with Fabricated OLED.



(a) Logarithmic I-V charachtristic of OLED with 3 Sweeps

(b) Logarithmic I-V charachtristic of OLED with 3 Sweeps



(c) 6-Tr voltage programmable pixel measurement testbench.

Figure 4.9: 2-Tr measurement results.

the bright flash of light emitted from OLED in first loop the rest of the measurement period parameter analyzer limits the current.

So for measuring this device, inside the parameter analyzer there is a function called *delay* and *hold* which gives a short delay between loops. For reading the output periodically, this time just a single point is given for the $I_{data}$and V_{Scan}. Then $V_{Control}$ is swept as first loop with same values as before. By using an Ammeter which was connected to the anode and cathode of the OLED we were able to read the final steady output, current and voltage. This measurement was repeated for coupled of times for I_{Data}ranging from 0.5 µA to 5 µA with steps of 0.5 µA. The highest out put for V_{OLED} and I_{OLED}were 5.6 V and 4.8×10^{-5}A respectively when I_{Data}= 3 µA.

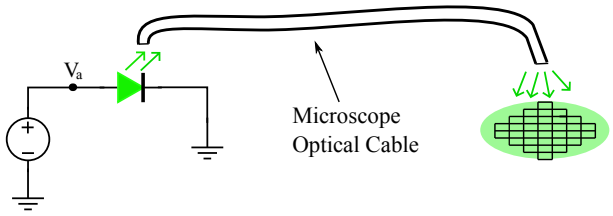


Figure 4.10: Measurement Setup.

4.4 Photodiode Measurements

4.4.1 I-V Characteristic

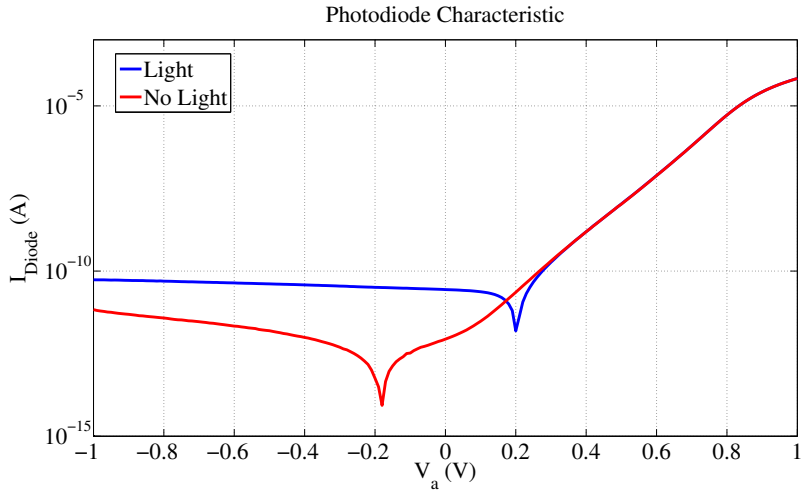
For measuring photodiode's response under the light, normal light source from Microscope was used. The white light from the bulb which has a power of 150W is transferred to to the probe station with a 1.2 meter optical cable which is a tube shape cable with inner side coated with reflective material. Because of the distance between the light source and the probe station's microscope, some percentage of the light photons are lost and even by using higher magnification lens for microscope to focus the light in specific location on the wafer, still we couldn't have true reflection of the light on the wafer, as shown in Fig.4.10.

By sweeping V_a(Anode of the photodiode) from -1 V to 1 V and measuring the current under condition when there are *Light* and *No Light*, results show that photodiode with intrinsic area of 1836 μm^2has a sensitivity of approximately 100 to microscope light, as shown in Fig.4.11a.

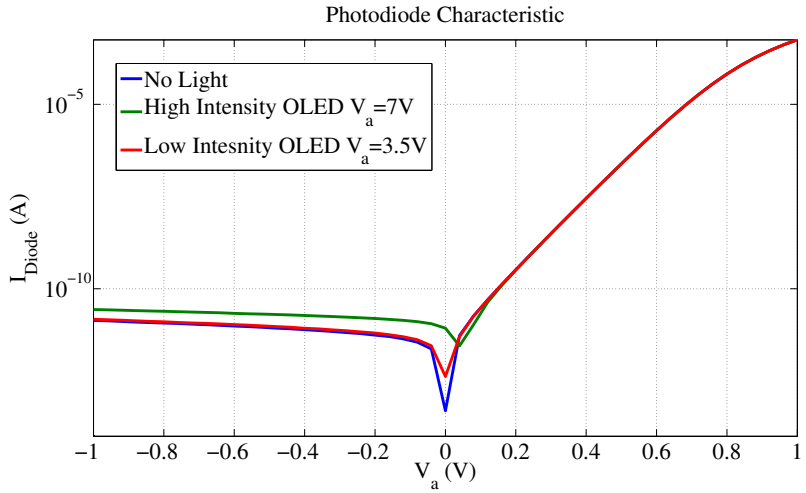
For measuring sensitivity of the photodiode with fabricated OLED same steps as above was carried out except, instead of using normal microscope lamp, OLED was used as light source. By biasing the OLED at 3.5V and 7V(V_a=3.5 V and 7 V) we measured the I-V characteristic of the photodiode. It should be noted that the light source geometry was small (1.5$\times$ 3 mm^2) in comparison with microscope's bulb and calibration of the optical cable wasn't possible as in normal microscope lamps which the light is focused by a lens to the optical cable, unfortunately the fabricated device was too small for that lens and not all the light from OLED transferred to the probe stations microscope, but visually we could confirm that a dim light was reaching to the surface. With this setup, it was possible to see the sensitivity of the photodiode to the OLED light with 0.5 fold. as shown in Fig.4.11b.

4.4.2 Quantum Efficiency

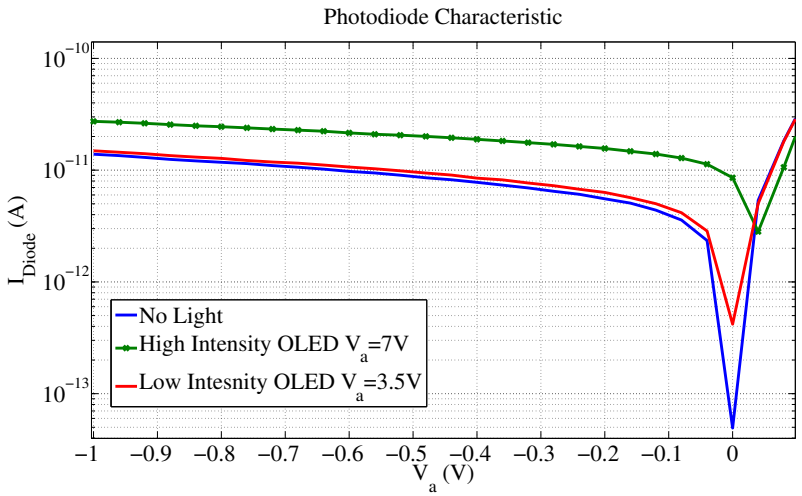
Quantum efficiency is a quantity defined for a photosensitive device, such as photodiode, as the percentage of photons hitting the photoreactive surface (intrinsic region) that will produce an electron hole pair. It is an accurate measurement of the device's electrical sensitivity to light. Since the energy of a photon depends on its wavelength,



(a) Photodiode I-V under microscop light



(b) Photodiode I-V under fabricated OLED.



(c)

Figure 4.11: Photodiode I-V characteristics.

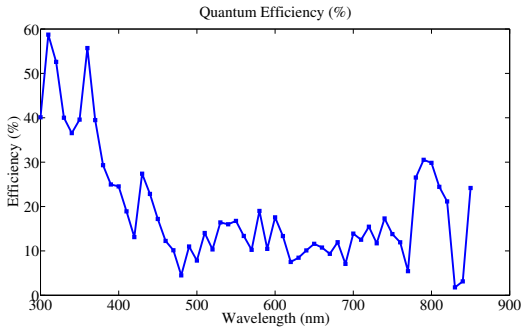


Figure 4.12: Quantum Efficiency

quantum efficiency is often measured over a range of different wavelengths to characterize a device's efficiency at each photon energy.

We performed quantum efficiency measurement from 300nm till 850nm wavelengths with Spectral response analyzer. First the photodiode reverse biased at -0.1 V and then device creates an incident light with different wave length and measures the output current of the photodiode for each of those wave length. Fig.4.12 shows the quantum efficiency curve. As it can be seen, this curve has peak equal to 60 % around 310nm and decreases with increasing wavelength. In visible light wavelengths it is 15% because of 250nm thin silicon layer. By increasing the thickness of the silicon we can gradually increase the quantum efficiency of the photodiode in visible light wavelength region.

4.4.3 Responsivity

To calculate the responsivity of the photodiode with fabricated OLED, we can use the following equation:

$$Responsivity = \frac{\left[\frac{I_{Diode}[A]}{Total\,intrinsic\,Area\,[m^2]}\right]}{Irradiance\ [W/m^2]} = \frac{\frac{2.73\times10^{-11}}{1836\times10^{-12}}}{\frac{10\times10^{-6}}{10^{-4}}} = 0.12\ [\mathrm{A/W}]$$

For 1 Watt (optical power) of the fabricated OLED the responsivity of the photodiode is equal to 0.12 A/W. It should be noted that here we assumed that OLED is located on top of the photodiodes and hence no loss of light is experienced.

4.5 Readout Circuit Measurements

Readout circuit which is designed to readout the current generated from photodiode under *Light* and *No Light* is setup for measurement as shown in Fig.4.13. This measurement is repeated two times, once at presence of light and then in dark environment.

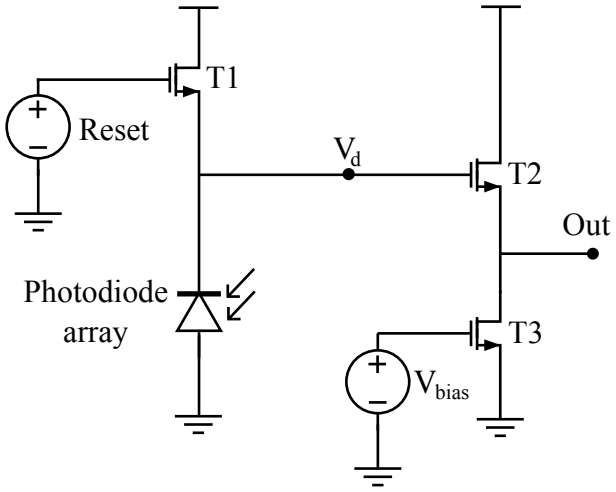


Figure 4.13: Readout measurement setup.

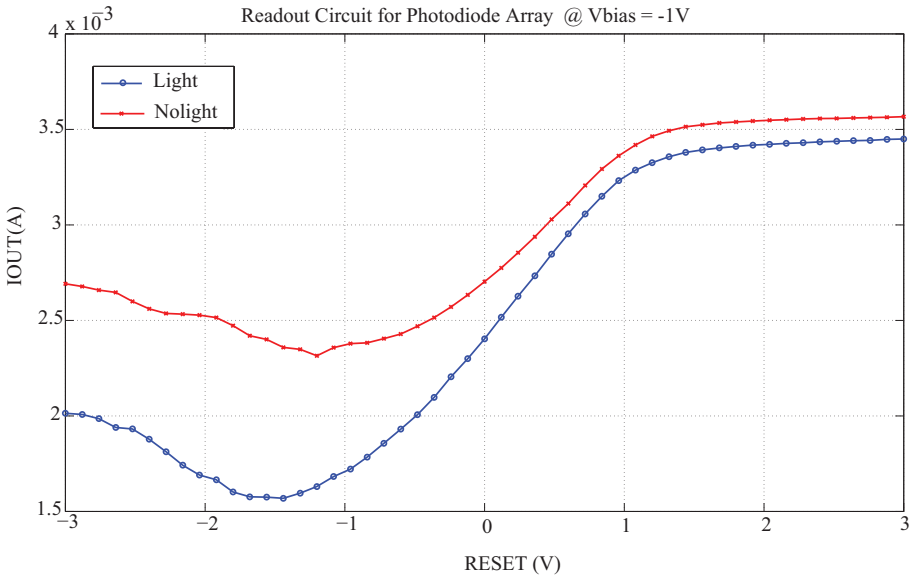


Figure 4.14: Readout circuit connected to photodiode under microscope light and no light.

By Sweeping V_{Reset} from -3 V to 3 V, applying -1 V to V_{Bias} and supplying 5 V DC source to V_{DD} following result have been achieved which is shown in Fig.4.14. This result clearly indicate that there is approximately 1 mA sensitivity at readout circuit in transition from dark to presence of light. It should be noted that I_{OUT} is dependent to g_m of the T2 transistor hence bigger g_m equals to bigger current at output.

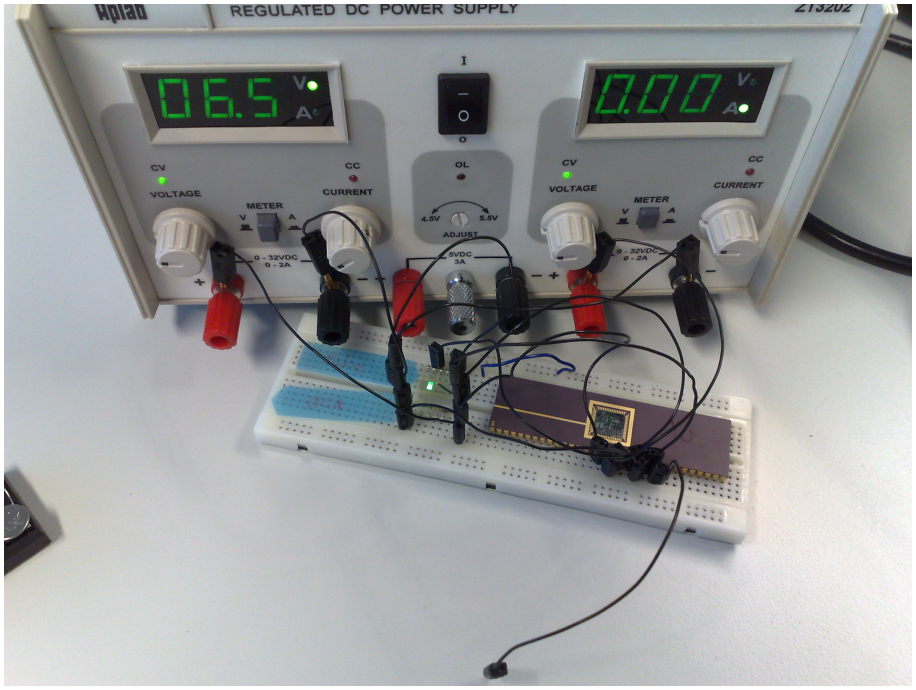


Figure 4.15: Measurement setup.

Conclusions and Future Work 5

This chapter gives an overview of the project's contributions.

5.1 Conclusions

In this thesis work I investigated organic light emitting diode displays backplane TFTs based on μ-Czochralski Single Grain Thin Film Transistors. New pixel structure is purposed which accompanies a photodiode array under the Anode/Cathode layer depending on OLED pixel, being top emitting or bottom emitting has been designed and fabricated.

For back plane TFTs different pixel structures has been designed and fabricated based on voltage programmable pixel and current programmable pixel and they have been characterized based on 4.5 mm^2PLED. Since the voltage programmed pixel circuits have provided an evident performance of non-uniformity compensation, they still suffer from the I_{OLED} non-uniformity due to the threshold voltage variation. Purposed solution for threshold variation was to give optical feedback from photodiode array back to the pixel. Meanwhile the current programmable pixel can compensate the nonuniform mobility of TFT as well as the threshold voltage of TFT in the current programming method. We achieved very good uniformity and high current in the pixels by using SG-TFTs, in designed pixels. Measured results shows that SG-TFT could be a good candidate for replacing poly Si TFTs, because of their good uniformity, high mobility.

Fitting photodiode array beneath Anode/Cathode also shows that with light emitted from OLED, it is possible to read the generated current and give feedback to the pixel.

During this thesis work OLED samples are fabricated based on F8:F8BT organic polymer (PLED) and characterized.

5.2 Future work

During this thesis work I made some experiment with OLED and SG-TFT pixels and there where some complications and new ideas, and from my experience I found them useful to mention for future works.

- During OLED (PLED) fabrication we made $\sim$40 nm film of active layer, it is useful to experiment with different thickness of active layer to see how it effects the I-V characteristics of the OLED.
- More experiments should be done with different cathode layer materials.
- Pulse converters and control signals of the pixel should be designed inside wafer (externally it is not possible most of the times).
- More investigation should be done with 4-Tr current programmable pixel.
- Glass Substrate or flexible substrate to be used for TFT pixels rather than Si wafer.
- Integration of the OLED and TFTs on same wafer.

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PLED Flowchart A

Fabrication of Organic Light Emitting Diode based on PLED

1. Glass or PET substrate with 100 nm$\sim$ 300 nm ITO deposited by useing shadow mask to create the *Anode* and one *Cathode* strip.
2. Cleaning the ITO substrate with Oxygen plasma stripper.
3. Filtering PEDOT:PSS using 0.45 μm PVDF filter for removing any impurities.
4. Spin for 30 seconds at 5000 RPM to produce $\sim$ 40 nm film of PEDOT:PSS.
5. Cleaning the PEDOT:PSS from the cathode using a cotton bud with water.
6. Place on hotplate at 150º C and store there until ready to transfer to glovebox. Once spin coating of the PEDOT:PSS is complete it is essential to get it onto the hotplate as quickly as possible .
7. After transfer to glovebox bake at 150º C for 5 minutes in N2 environment to remove any residual water.
8. Heat to 80º C for 10 mins to re-dissolve any aggregates that have formed.
9. Cool to room temperature for 10 minutes.
10. By using 0.45 μm PTFE filter, filter 95% F8 : 5% F8BT solution (active layer).
11. Spin for 30 seconds at 2000 RPM to produce thickness of $\sim$ 80 nm (~5000 RPM for big substrates >6 cm).
12. Clean any areas where active layer is not required using cotton bud and toluene.
13. Bake at 80º C for 10 minutes before evaporation.
14. Evaporate between 2.5 and 10 nm of Calcium at 0.5 Å/s and a pressure of ideally <10-6 mBar. Thinner layers will produce slightly brighter layers due to calcium being a relatively poor reflector.

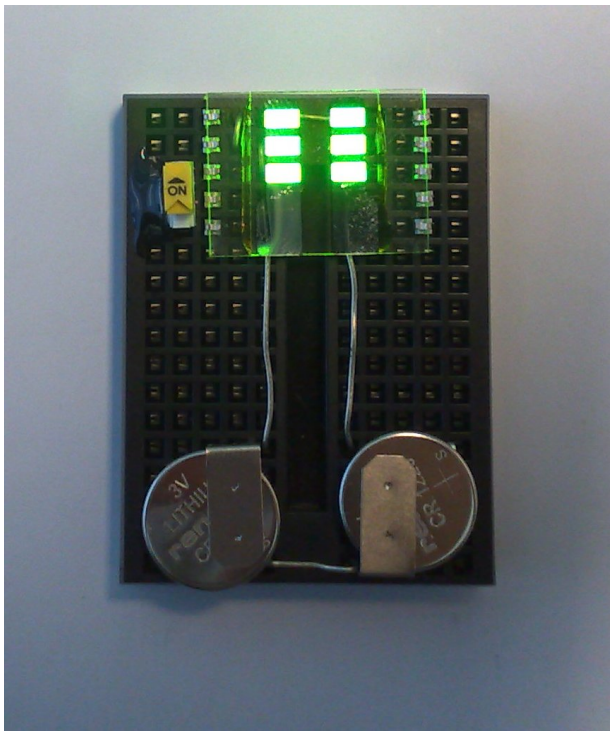


Figure A.1: Green OLED Pixels.

15. Evaporate >50 nm of silver or Aluminium (silver has slightly better reflectivity) at a rate of 1.5 Å /s and a pressure of ideally <10-6 mBar. The thickness of this layer does not really matter so long as it is more than about 25 nm at which point it is optically opaque and highly conductive.

16. **OPTIONAL**: Evaporate 100 nm of Calcium to act as a "getter" layer to improve lifetime and enable visualization of any oxygen/water ingress.

17. Encapsulate using glass slide and Ossila EE1 epoxy under N2 atmosphere.

18. Cure for $\sim$ 30 minutes in low power UV light box.

Small Molecule OLED B

During This project two types of OLED have been used, polymer based and small molecule OLED. Polymer based OLED is explained in Chapter 2. But regarding small molecule OLED, there were some complications which are explained here.

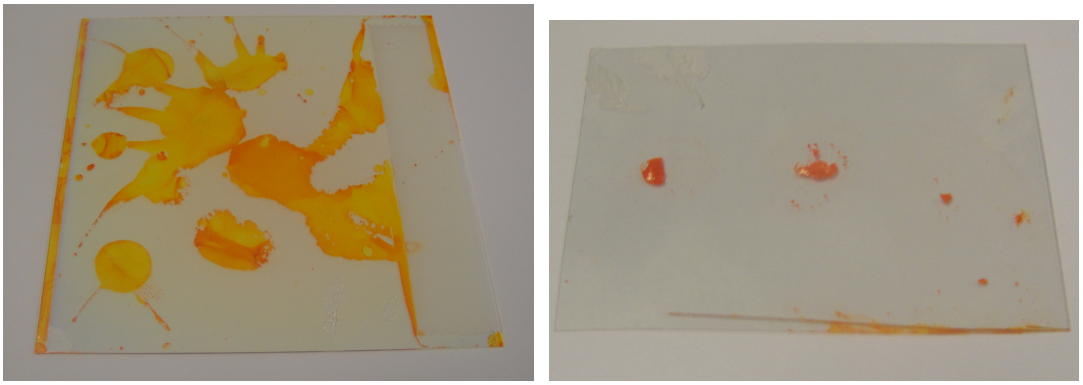
Small molecule OLED which were experimented were supplied from E2M Technology Ltd and the OLED fluid was orangish red color (RED DIAMOND™). RED DIAMOND™ is blend of Tris(2,2'-bipyridyl)dichloro-ruthenium (II) hexahydrate, Ammonium hexafluorophosphate and Acetonitrile.

Couple of experiments were done with this OLED and different samples were made on glass substrate and PET substrate but all of them were unsuccessful. The company provided the ITO films (ITO on PET substrate) and also we made some ITO on glass (100 nm thick ITO) samples in TUDelft for this experiment. During spin coating of the active layer (RED DIAMOND™) on some test substrates, it was notices that the viscosity of the OLED fluid is high and fluid doesn't spread evenly on the surface of ITO, shown in Fig.B.1. For solving this issue, we increased the spiner's RPM to more than 3000 RPM.

First experiments were done with ITO films (ITO on PET substrate). During spin coating of the active layer, it was noticed that the surface of the ITO is very hydrophobic and and fluid forms a thick bubble, shown in Fig.B.1b. Meanwhile because of the flexible substrate, ITO surface wasn't flat and and distribution of the fluid on the substrate wasn't even.

Second set of experiments were done with ITO on glass substrate which was processed in TUDelft. We spin coated the OLED fluid for 30 seconds at 3500 RPM and we were able to cover most of the surface of ITO, as shown in Fig.B.2 . After placing the substrate on hot plate for 10 minutes at 80° C, we deposited the Al cathode layer.

During measurement, it was notices that there are some electrical spikes between the anode and cathode of the fabricated OLED. After some investigation it became apparent that, because of the low temperature (room temperature) ITO deposition, ITO surface forms a ring shape and because the thickness of the OLED on top of ITO is less than 100 nm, this roughness of ITO causes some non uniformity in OLED layer, when the device is operated under high electric field or after a long time, the progressive electric short phenomenon appears because of collapse of the defect position.[1]



(a) Active layer on Hydrophobic surface of ITO on glass.

(b) Active layer on hydrophobic surface of ITO on PET.

Figure B.1: Hydrophobic ITO.

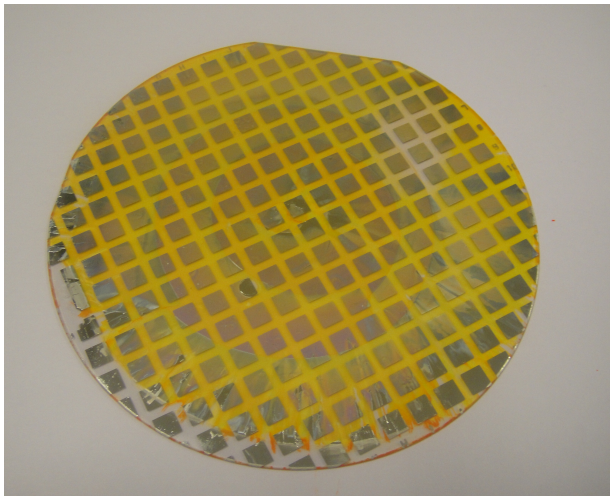


Figure B.2: Small molecule OLED on glass substrate.