Scaling behavior and parasitic series resistance in disordered organic field-effect transistors

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The scaling behavior of the transfer characteristics of solution-processed disordered organic thin-film transistors with channel length is investigated. This is done for a variety of organic semiconductors in combination with gold injecting electrodes. From the channel-length dependence of the transistor resistance in the conducting ON-state, we determine the field-effect mobility and the parasitic series resistance. The extracted parasitic resistance, typically in the MΩ range, depends on the applied gate voltage, and we find experimentally that the parasitic resistance decreases with increasing field-effect mobility. 


The interest in organic thin-film transistors (TFTs) has grown rapidly due to envisaged applications, such as integrated circuits and active-matrix displays. The switching speed of organic integrated circuits can be estimated from the performance of the individual transistors and is roughly proportional to \( \mu_{FE}/L^2 \), where \( L \) is the channel length of the transistor, and \( \mu_{FE} \) is the field-effect mobility. To reach higher switching speeds, the search for higher mobility materials is therefore important, but it is also of great interest to downsize the transistor geometries. In this work, the scaling behavior of the transfer characteristics with transistor channel length is investigated for a variety of solution-processable organic TFTs.

In the experiments, we use heavily doped Si wafers as the gate electrode, with a 200-nm-thick layer of thermally oxidized SiO\(_2\) as the gate-insulating layer. Using conventional lithography, gold source and drain contacts 100 nm thick are defined, with channel widths ranging from 1 mm to 1 cm and channel lengths between 0.75 and 40 \( \mu \)m. The structures typically have an underetch of 0.5 \( \mu \)m, which we neglect in the following analysis. A 10-nm layer of titanium acts as an adhesion layer for the gold on the SiO\(_2\). The SiO\(_2\) layer is treated with the primer hexamethyldisilazane to make the surface hydrophobic. No special care is taken to clean the gold surface prior to deposition of the semiconductor. Poly(2,5-thienylene vinylene) (PTV) films as semiconductor layer are deposited using a precursor-route process. 3 We systematically varied the processing conditions for the conversion from precursor to PTV, and we determined the average degree of conversion using the method described by Fuchigami et al. 4 This enabled us to systematically study PTV transistors at various degrees of conversion ranging from 60% to 100%, and consequently over a range of field-effect mobilities, between \( 10^{-4}\) and \( 10^{-3}\) cm\(^2\)/V s. Poly(3-hexyl thiophene) (P3HT) is spin-coated from a 1 wt % chloroform solution. Films of poly[(2-methoxy-5-(3’,7’-dimethoxyloxy)]-p-phenylene vinylene (OC\(_10\) C\(_{10}\)-PPV) and poly[(2,5-di-(3’,7’-dimethoxyloxy)]-p-phenylene vinylene) (OC\(_{10}\) C\(_{10}\)-PPV), are spun from a 0.5 wt % toluene solution. Pentacene thin films are deposited using a precursor-route process. 3 The measurements are performed on freshly prepared samples in order to minimize external doping and degradation effects. 5 The PTV, OC\(_{10}\) C\(_{10}\)-PPV, OC\(_{10}\) C\(_{10}\)-PPV, and pentacene samples are measured in air, whereas the P3HT samples are measured in vacuum and dark after a thermal dedope procedure. 6 The electrical characteristics are recorded using an HP4155B semiconductor parameter analyzer.

Typical source–drain current \( I_{ds} \) versus gate voltage \( V_g \) characteristics for solution-processed PTV and P3HT are shown in Fig. 1 for different channel lengths, where \( W \) is kept constant. The position of the switch-on voltage \( V_{so} \), which determines the onset of the field effect and is defined as the flatband condition of the transistor, does not vary much between the transistors with different channel length. At low source–drain voltage, \( V_{ds} = 2 \) V, where the in-plane drift field is much smaller than the applied gate field (gradual channel approximation), 3 the field-effect mobility is evaluated using

\[
\mu_{FE}(V_g) = \frac{L}{WC_i V_{ds}} \frac{\partial I_{ds}}{\partial V_g},
\]

where \( W \) is the channel width and \( C_i \) the capacitance of the insulating layer per unit area.

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The field-effect mobilities for both PTV and P3HT are found to depend on the channel length of the transistor, which can be seen from the insets of Fig. 1. By comparing the output characteristics multiplied by the channel length, that is, at constant source–drain field, for short- and long-channel transistors, we clearly see an effective current decrease for shorter channel lengths, which is demonstrated for P3HT in Fig. 2. Furthermore, at low drain voltages, the output characteristics of the long transistor show ohmic behavior, whereas for the short-channel transistors, at low drain voltages, superlinear output characteristics are observed. Because \( \mu_{FE} \) is decreasing with reduced \( L \), the reduction of the channel length will not result in the expected increase of the switching speed in circuits.

From amorphous silicon TFTs, it is well known that the presence of source and drain parasitic resistances, \( R_s \) and \( R_d \), respectively, can give rise to an apparent \( \mu_{FE} \) that decreases with decreasing channel length. This is due to the fact that in shorter channels, a relatively larger fraction of the applied source–drain voltage drops over the parasitic resistance, as compared with the long-channel transistors. To be able to evaluate the performance of the organic semiconductor, a correction for the parasitic resistance, \( R_p = R_s + R_d \), is required. A theoretical approach to this end was presented by Horowitz et al. Experimentally, it has been demonstrated that the influence of \( R_p \) can be reduced by modifying the interface between the current injecting contacts and the organic semiconductor. For experimental evaluation of \( R_p \), Kelvin probe force microscopy has been employed. Here, we investigate the scaling behavior of the transistor current, to estimate \( R_p \).

We plot the total device resistance, \( R_{ON} = V_{ds}/I_{ds} \), as a function of the nominal channel length \( L \), for different gate voltages in Fig. 3. In the linear operating regime of the transistor, the channel resistance varies linearly with the channel length. The parasitic resistance, \( R_p = R_s + R_d \), at the source and drain contacts is assumed to be independent of \( L \). The \( R_{ON} \) can then be expressed as:

\[
R_{ON}(L) = \frac{\partial V_{ds}}{\partial I_{ds}} \bigg|_{V_{ds} = 0, V_g} = R_{ch}(L) + R_p. 
\]

The experimental data are, in first order, well described by this equation, with \( R_{ON} \) depending linearly on \( L \) (see Fig. 3).

From the slopes of the plots in Fig. 3, we find the channel resistance \( R_{ch} \), the inverse of which, \( [\Delta R_{ON}/\Delta L]^{-1} \), is the channel conductivity. From the derivative of the channel conductivity, the field-effect mobility, corrected for \( R_p \), can be obtained:

\[
\frac{\partial}{\partial V_g} \left[ \frac{\Delta R_{ON}}{\Delta L} \right]^{-1} = \mu_{FE}(V_g) W C_i. 
\]
The resulting corrected mobilities are plotted in the insets of Fig. 1. The corrected curve yields a higher overall \( \mu_{\text{FE}}(V_g) \). From the insets of Fig. 1(b), it is clear that for the 40-\( \mu \)m channel, the influence of \( R_p \) is small, as \( \mu_{\text{FE}} \) obtained from Eq. (1) is close to the corrected mobility. We note that any nonlinearity of \( \mu_{\text{FE}} \) with \( V_g \) in our samples cannot be \textit{a priori} attributed to the presence of an \( R_p \), but is more probably the result of a specific density of states in the semiconductor at the semiconductor/insulator interface. From the analysis with Eq. (2), we find \( R_p \) in Fig. 3 as the intercept of \( R_{\text{ON}} \) at \( L = 0 \). This \( R_p \), typically on the order of 1\( \Omega \) for our devices, is found to decrease with increasing gate voltage, that is, with increasing carrier density.

We find experimentally that both the field-effect mobility and the parasitic resistance depend on \( V_g \). In Fig. 4, we plot the experimentally determined \( R_p \), multiplied with the channel width, and effective \( \mu_{\text{FE}} \) obtained from the scaling analysis of several organic semiconductors. In addition, data from a P3HT study of Sirringhaus et al.\(^{11}\) are included. An empirical relation is observed between the mobility and the parasitic resistance for the polymeric TFTs in contact with the gold/titanium stack. A possible reason for this empirical observation is that the density of localized states in the polymer is of importance for the charge injection efficiency. Why this results in a very similar dependence of \( \mu_{\text{FE}} \) on \( R_p \) for different polymeric semiconductors is unclear at present. In literature it has been demonstrated that injection-limited current into a disordered polymer can be described by thermally assisted hopping from the electrode into the localized states of the polymer, which are broadened due to disorder.\(^{18}\) As a representation of this effect, the \( R_p \) for injection into a semiconducting polymer is found to depend on the charge carrier mobility in the polymer.\(^{19}\) For the molecular semiconductor pentacene, the data are more scattered, and do not follow the trend observed for the polymeric transistors (see Fig. 4). We attribute this to the polycrystalline nature of the pentacene films, which depends on the processing conditions.

The origin of the observed parasitic series resistance, or injection-limited current, can be due to a combination of effects. In general, geometrical or morphological contact problems between the semiconductor film and the gold contacts can be of importance, which is indicated by the scattered pentacene data. However, the data for the polymers are much more consistent, and suggest that the injection barrier is related to material parameters of electrode and semiconductor layer rather than processing variations. A mismatch between the work function of the gold, at 5.1 eV, and the highest occupied molecular orbital level of the semiconductors (for the materials used here: around 5.2 eV) would lead to an injection barrier for holes. The width of this injection barrier can be narrowed by accumulating charge in the semiconductor, through the field effect, by applying a \( V_g \).\(^{20}\) For a small barrier height, in the order of the thermal energy \( k_B T \), this will result in an ohmic parasitic resistance, whereas for higher barrier heights, a nonohmic parasitic resistance will be present at the electrode/semiconductor interface.

In conclusion, we have used channel-length-dependent measurements to experimentally determine the effective field-effect mobility, corrected for parasitic series resistance, in a variety of spin-coated organic field-effect transistors. For the investigated transistors, we extract a parasitic series resistance, which depends on \( V_g \). This parasitic resistance is attributed to an injection barrier with a height on the order of a few times \( k_B T \), which results in an ohmic parasitic series resistance. Experimentally, we find that the parasitic resistance decreases with increasing charge carrier mobility for the investigated polymeric field-effect transistors.

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