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Number of Levels, Arm Inductance and Modulation Trade-offs for High Power Medium Voltage Grid-Connected Modular Multilevel Converters

Aditya Shekhar, Lucia Beloqui Larumbe, Thiago Batista Soeiro, Yang Wu and Pavol Bauer

***Abstract*—There is an increasing focus on integrating flexible dc links for bulk power routing in medium voltage distribution grids. In such applications, the ac-dc Modular Multilevel Converter (MMC) devised for medium voltage and high-power ratings can be an interesting choice. This paper highlights some less explored design trade-offs arising due to the limitation on N in relation to modulation frequency and arm inductance. Specifically, the study intends to describe the interdependent influence of each degree of freedom on several aspects such as capacitor voltage balancing, circulating currents and harmonic performance. Finally, the importance of considering interharmonics in the performance assessment of the MMC instead of the conventional interpretation of distortion calculation is highlighted.**

***Index Terms*—capacitor voltage balancing, circulating current, design steps, grid-connected, harmonic performance, optimal submodules.**

I. Introduction

Unlike high voltage applications of the Modular Multilevel Converter (MMC) where number of submodules (N) is very high (usually $N > 100$), that for medium voltage applications is lower ($N < 25$ for a 20 kV dc link). This paper is based on the premise that the limited number of submodules introduce some less explored design trade-offs that make the optimal selection of N of paramount importance [1]–[3]. Optimal design of MMC is relevant because of increasing interest for its medium voltage high power applications in distribution grids [4]–[9].

Reference [3] showed that the choice of a high Insulated-Gate Bipolar Transistor (IGBT) blocking voltage such as 6.5 kV can minimize the required N for a given dc link voltage, thus reducing the conduction losses as a trade-off for higher switching losses. Similarly, a blocking voltage of 1.2 kV (or lower) may have lower switching losses but higher conduction losses due to high N. Thus, the paper suggested, from purely an efficiency standpoint, that the optimum choice is likely to be a compromise such as a blocking voltage of 1.7 kV or 3.3 kV. This is, however, only a part of the picture forming the design choices.

Section II discusses the trade-offs between number of submodules, arm inductance (L_{arm}) and modulation technique and specifically highlights the dependence of the design choice on capacitor voltage balancing, high frequency ripple in the internally circulating current and harmonic performance of output waveforms. The minimum limit on L_{arm} due to the possibility of resonance with arm capacitance is explored. Section III numerically shows that capacitor voltage balancing is independent of N and L_{arm} for the considered operation and the requirement sets a minimum limit on switching frequency. Section IV quantifies the variation in circulating current with varying design parameters to suggest that the associated high frequency ripple reduces relatively more significantly with N. Section V explores the impact of the available degrees of freedom on the total demand distortion (TDD) of output ac current of the MMC. Finally, Section VI describes the step-by-step design procedure followed and summarizes the optimized values obtained for the given specifications for the studied high-power medium voltage grid-connected MMC.

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II. Design Considerations

The schematic of half bridge MMC and the available scale-down lab prototype is shown in Fig. 1. The half-bridge topology was chosen for high power back-to-back MMC operation due to its superior efficiency and comparatively lower cost as compared to full bridge [10]. It consists of N submodules (SM) and inductance L_{arm} per arm. Each SM consists of two IGBT switches (T_1, T_2) with anti-parallel diodes (D_1, D_2) and a capacitor (C_{sm}). The specifications of the converters are fixed with dc link voltage v_{d} and the operating power given in Table II. The upper and lower arm currents $i_{\text{u,M}}$ and $i_{\text{l,M}}$, dc link current i_{d} and the output current $i_{\text{s,M}}$ are shown corresponding to the phase M.

The current work extends the design procedure highlighted in [3] by focusing on three degrees of freedom: N, switching frequency (f_{sw}) and arm inductance (L_{arm}). These parameters and their influence on three performance indicators of the half bridge MMC are highlighted in Fig. 2, namely: capacitor voltage ripple (ΔV), circulating current ripple (Δi) and the power quality (TDD of $i_{\text{s,M}}$). The parameters of the simulated system are mentioned in the Appendix.

A. Number of Submodules (N)

The optimal number of sub-modules for the given $v_{\text{d}} = 17$ kV can be either 5, 7, 9, 17 or 24 based on the market available IGBT switch blocking voltage (V_{blk}) of 6.5, 4.5, 3.3, 1.7 and 1.2 kV respectively [3]. These values were selected based

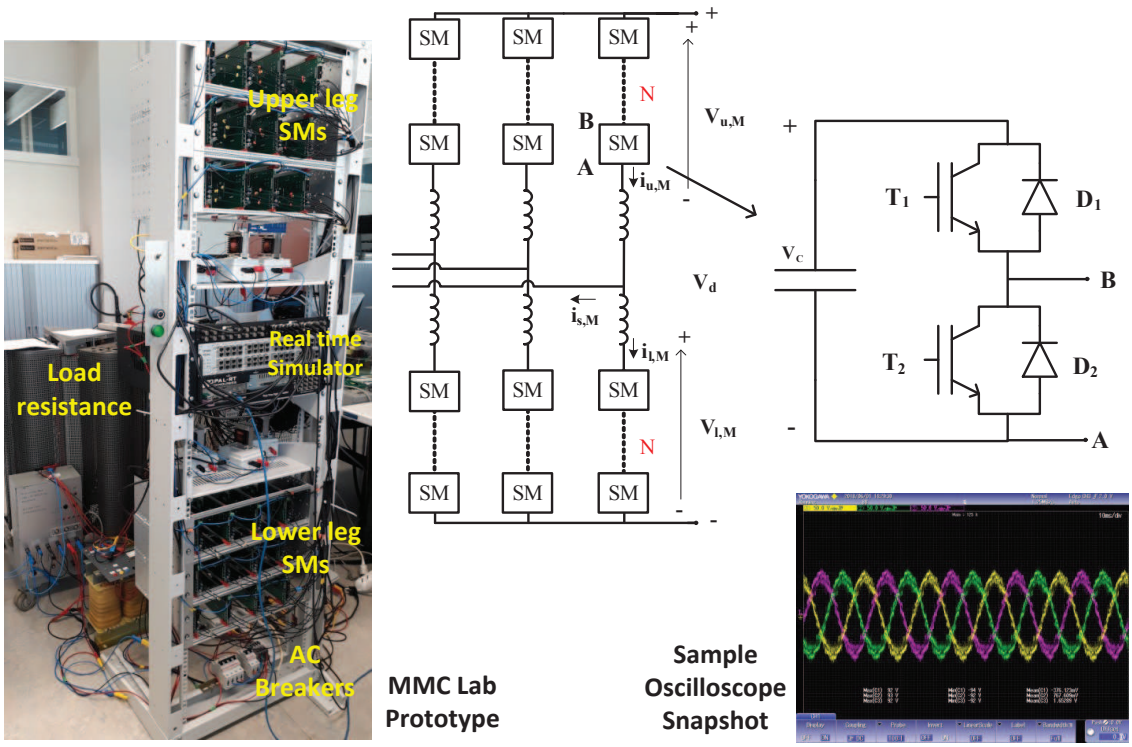


Fig. 1: Three phase ac-dc modular multilevel converter with half bridge submodules.

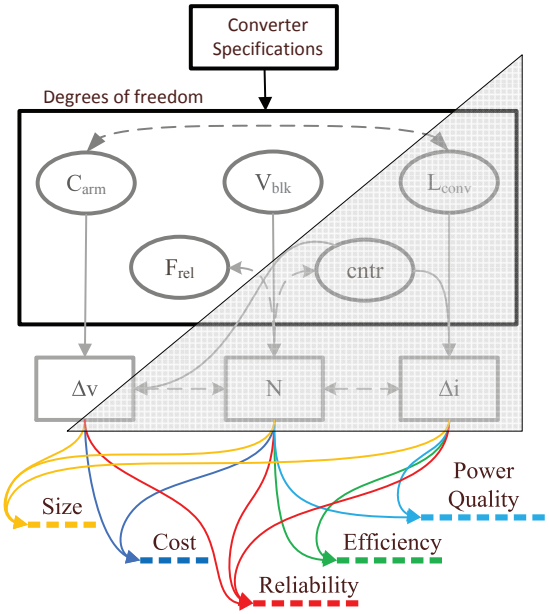


Fig. 2: Degrees of freedom and performance criteria for MMC design of given specification considered in this paper.

on the average component of capacitor voltage ripple governed by arm energy storage requirements from C_{arm} [11] and the reliability factor (F_{rel}) associated with the safety factor (S_f) of the IGBT switch [1]. For example, the submodule capacitance of 2...3.3 mF is chosen as a thumb-rule corresponding to total energy storage capability of 25...40 kJ/MVA in trade-off with average voltage ripple ($\Delta V_{\text{c,avg}}$) [11]. Then, the optimal N for a given IGBT switch rating is chosen such that the $\Delta V_{\text{c,avg}}$ can be met adequately with S_f between 0.6...0.7 [3].

The efficiency of the converter with different N was quantified for the rated power and it was shown that below the effective frequency of 3.5 kHz, the losses with 1.7 and 1.2 kV are highest. According to [3], the final design choice between $N = 5$, 7, and 9 would depend on power quality, capacitor voltage balancing needs and circulating currents in trade-off with L_{arm} and f_{sw}. These aspects are explored subsequently.

B. Arm Inductance (L_{arm})

A higher L_{arm} is preferred because it limits the circulating currents in the MMC [12], [13], limits the rate of rise of arm current during dc link fault [13], [14] and improves harmonic performance for output ac currents [2]. On the other hand, this increases the conduction losses and size of the converter. Furthermore, minimizing L_{arm} can be beneficial in improving the reactive power capability of the MMC.

The constraint associated with the resonance of L_{arm} with C_{arm} should be considered [15]. Fig. 3 gives insight on this constraint specific to the design conditions of the considered MMC with $N = 9$. In this example, h is the harmonic order for the circulating current and m is the operating modulating index of the converter. The paper highlights that no inserted arm capacitance ($C_{\text{sm}}/N_{\text{u}}$, where N_{u} is an integer between 1 to N) should fall within the resonance band described by h & m for the given L_{arm}.

Depending on the inserted number of submodules, the arm capacitance has nine possible values for the given C_{sm}.

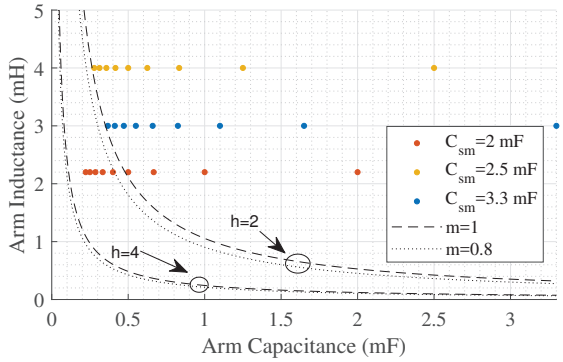


Fig. 3: Constraint on L_{arm} due to resonance with C_{arm} for N=9 for low frequency circulating current ripples. The dots show different resonant frequencies for different N_{u}.

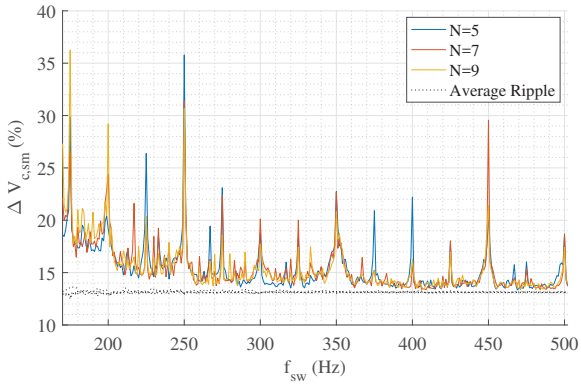
The L_{arm} should be chosen such that none of these nine values create resonance for the circulating current (without considering the circulating current controller) [15]. With lower number of N, number of critical resonant points corresponding to possible arm capacitances will reduce. In this paper, the inductance in the range of 2...5 mH will be explored.

C. Modulation Aspects

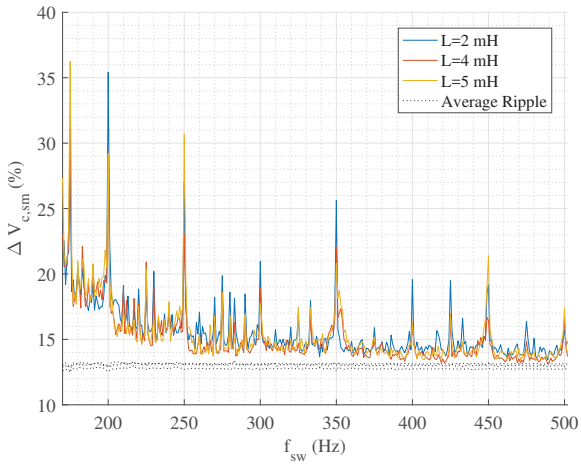
A discussion on different PWM methods on switching frequency, voltage balancing capability and harmonics is offered in [16]. Carrier based modulation technique such as Phase-Shifted Pulse Width Modulation (PS-PWM) is preferred over nearest level modulation for low number of sub-modules per arm [17], [18], such as $N = 5$, 7 and 9 considered in this paper. It will be shown that capacitor voltage balancing needs sets a minimum limit on switching frequency (f_{sw}) for PS-PWM independent of N and L_{arm}. Additionally, it is interesting a high enough f_{sw} as this can limit the circulating currents and total harmonic distortion in the output waveform. However, increasing f_{sw} enlarges the switching losses in trade-off with conduction losses associated with N and L_{arm}. This trade-off is particularly relevant for medium voltage high-power applications because the effective frequency is switching loss limited for low number of sub-modules such as $N = 5$, 7 and conduction loss limited for higher number (N =9, 17, 24) [3]. That is, for a given set of operational requirements, minimization of switching losses is more important as compared to conduction losses for lower N and vice-versa for higher N. Depending on the modulation technique, the number of levels (N+1) can be increased in trade-off with circulating current.

III. Capacitor Voltage Ripple

The maximum submodule (SM) capacitor voltage ripple ($\Delta V_{\text{c,sm}}$) as a percentage of average SM voltage ($\frac{v_{\text{d}}}{N}$) is shown in Fig. 4. Switch model simulations were performed using parameters listed in Table II based on the fully loaded MMC with current controllers as suggested in [19], [20] with a frequency sweep between the range of 150-500 Hz at a step of 1 Hz. PS-PWM method is used with no phase shift between the carriers corresponding to upper and lower arms of the MMC.



(a)



(b)

Fig. 4: Simulated maximum voltage ripple in submodule capacitors with f_{sw} for $C_{\text{sm}}/N = 0.22$ mF and for (a) varying N with $L_{arm} = 5$ mH (b) varying L_{arm} with $N = 9$.

The observation that the local ripple due to capacitor voltage imbalance decreases with f_{sw} and that this decline is particularly significant for lower f_{sw} is consistent with the findings in [21]. However, unlike [21], a clear tendency was not observed with the variation in N (Fig. 4a), possibly because the selected simulation parameters in [21] were corresponding to extremely high power (in GW) and voltage (320 kV). Nevertheless, the same study also predicts weak to no dependence of $\Delta V_{\text{c,sm}}$ with $N > 10$. Fig. 4b shows that $\Delta V_{\text{c,sm}}$ is independent of L_{arm} as well.

The result suggests that the capacitor voltage balancing requirements set a minimum limit on the required switching frequency ($f_{\text{sw,min}}$) independent of the chosen N and L_{arm} where the local ripple is negligible and the $\Delta V_{\text{c,sm}}$ converges to the operating power dependent average voltage ripple corresponding to the total arm capacitance. This aspect can be of importance while optimizing the three degrees of freedom for converter harmonic performance, but may not necessarily always be an issue because at medium voltage

levels the conduction loss constraint puts an upper limit on the optimal N [2], [3], [22]. Therefore, it is suggested as a design thumb-rule, that the first approximation of the switching frequency should be independently chosen above the minimum required $\Delta V_{\text{c,sm}}$ for the given modulation method and operating conditions before choosing the optimal N and L_{arm}. It can be observed that a $\Delta V_{\text{c,sm}}$ reasonably close to the $\Delta V_{\text{c,avg}}$ can be obtained for $f_{\text{sw,min}} > 250\,\text{Hz}$. In Fig. 5, it can be seen that $f_{\text{sw,min}}$ where the actual $\Delta V_{\text{c,sm}}$ is close to the designed arm energy storage dependent average ripple is similar, about 250 Hz even with higher total arm capacitance ($C_{\text{sm}}/N = 0.37\,\text{mF}$).

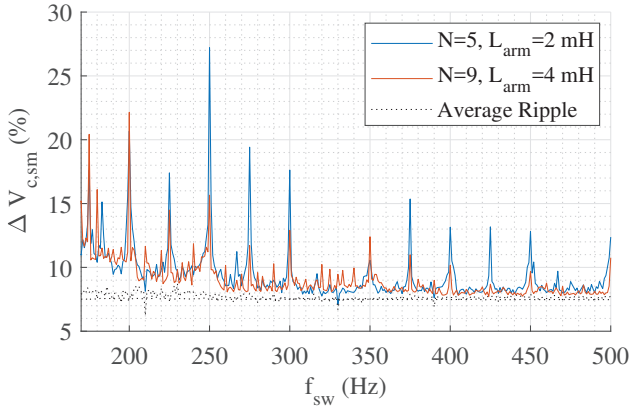


Fig. 5: Simulated maximum voltage ripple in submodule capacitors with switching frequency for $C_{\text{sm}}/N = 0.37\,\text{mF}$.

Another important observation is that when f_{sw} is a multiple of 50 Hz, the capacitor balancing is much worse for PS-PWM and thus, in MMCs, the value of f_{sw} is usually selected to give a non-integer frequency ratio [20], [23]. The empirical evidence for this is shown in Fig. 6.

In this experiment, the 4-submodule MMC lab prototype with $C_{\text{sm}} = 4\,\text{mH}$ shown in Fig. 1 is run using a DC source at 100 V with a modulation index of 1 to power a resistive load of 60 Ω at the ac side. Gate signals generated using PS-PWM by the real time simulator were sent to the sub-modules using optical fibres. The individual SM capacitor voltages were observed to be balanced with non 50-multiple switching frequency of 997 Hz but not when it is 1000 Hz. With this supporting insight for [23], the design switching frequency will be chosen a prime number.

IV. Circulating Current Ripple

An interesting discussion on circulating current ripple (ΔI_{c}) variation with arm inductance is provided in [12], but the impact of N is not explored. In the current work, we want to study the combined impact of f_{sw}, N and L_{arm} on ΔI_{c}.

Fig. 7 shows the simulated frequency sweep results for ΔI_{c} as a percentage of its mean value, which decreases with increase in f_{sw}, N and L_{arm}.

In these results, the circulating current controller is designed based on the principles in [13], [23] with bandwidth mentioned in [24] and peak high frequency ripple component is computed in steady state. The main observation is that decrease in ΔI_{c}

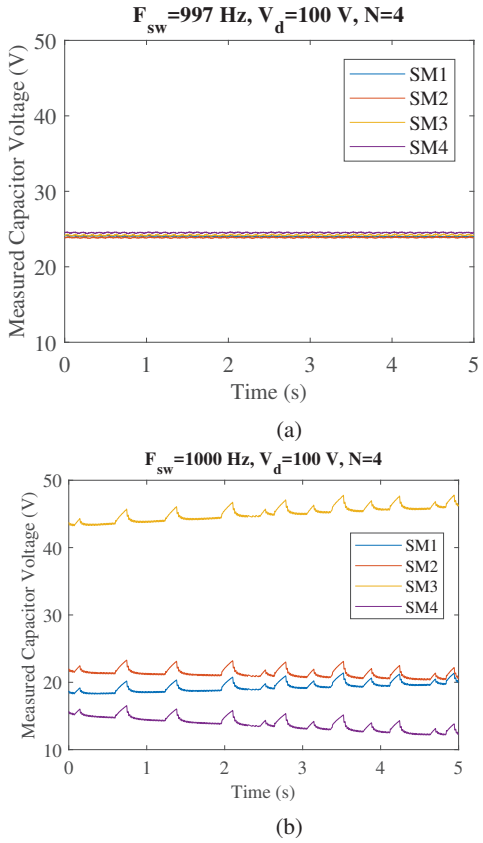


Fig. 6: Experimental result showing capacitor imbalance due to slightly different switching frequency a) 997 Hz b) 1000 Hz.

is more significant with N, as compared to f_{sw} and L_{arm} and appear independent of total arm energy. Though the circulating current controller may mitigate the resonance limits imposed, the $L_{\text{arm,min}}$ described by Fig. 3 should be considered for robust design. While the impact of high frequency circulating current on efficiency of MMC may be marginal and its effect of component reliability and electro-magnetic interference (EMI) is beyond the scope of this paper, it is suggested that the designed ΔI_{c} be below 20 % as a design thumb-rule for the considered operational conditions of the MMC.

V. Harmonic Performance

In this section, the objective is to find the minimum values of f_{sw}, N and L_{arm} in order to achieve acceptable harmonic performance.

A. Assumptions for Acceptable Harmonic Performance

In this paper, the current harmonic limits defined in the standard IEEE 519 (2014) are going to be followed. These are shown in Table I for LV and MV applications [25]. The limits are set depending on the short-circuit ratio (SCR, the ratio of the available short-circuit current from the grid, I_{SC}, to the load current, I_{L}). The simulations are performed with a high SCR=100 and therefore, result in correspondingly high current harmonics at point of common coupling (PCC) due to

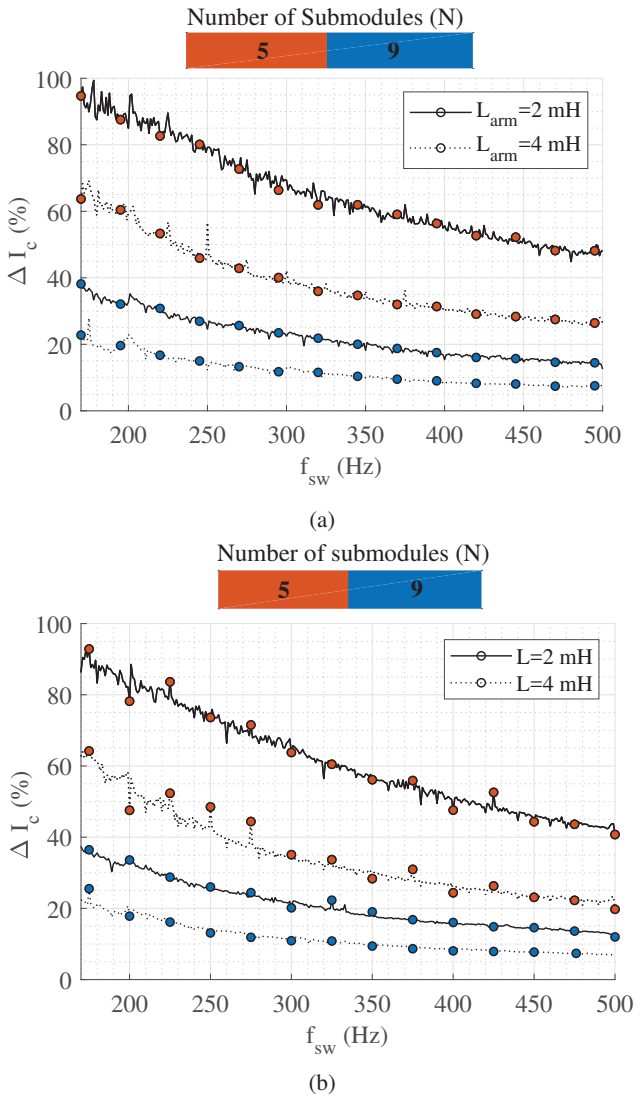


Fig. 7: Switching frequency, arm inductance and number of submodules trade-off for high frequency circulating current ripple with (a) $C_{\text{sm}}/N = 0.22\,\text{mF}$ (b) $C_{\text{sm}}/N = 0.37\,\text{mF}$.

low assumed grid inductance. However, the design procedure is chosen to comply with harmonic limits corresponding to the lowest SCR ($I_{\text{SC}}/I_{\text{L}} < 20$ in Table I), due to the fact that here the limits are the strictest. These two assumptions ensure that the design procedure follows the most stringent requirements for the output current harmonic performance. If voltage harmonic performance is used as design criteria, the worse case assumptions should be different.

The Total Demand Distortion (TDD) is defined as Eq. 1, where I_{h} is the current amplitude of the h-th harmonic component (h-th integer multiple of the fundamental, f_0) [25]. $I_{1,\text{max}}$ is the maximum demand current and $H = 50$.

$$TDD = \frac{\sqrt{\sum_{h=2}^{H} I_h^2}}{I_{1,max}} \tag{1}$$

TABLE I: Maximum current distortion limits for systems rated 120 V - 69 kV (as percent of fundamental). Table for odd harmonics (even harmonics limits are 25 % of these) [25]

$I_{\text{SC}}/I_{\text{L}}$	3≤ h<11	11≤ h<17	17≤ h<23	23≤ h<35	35≤ h<50	TDD
<20	4.0	2.0	1.5	0.6	0.3	5.0
20<50	7.0	3.5	2.5	1.0	0.5	8.0
50<100	10.0	4.5	4.0	1.5	0.7	12.0
100<1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

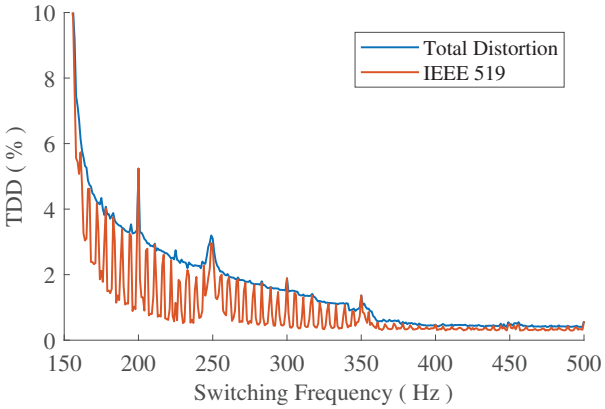


Fig. 8: Simulation results ($N = 9$ and $L_{\text{arm}} = 3$ mH). Comparison of TDD calculated without interharmonics (IEEE 519) with TDD calculated with interharmonics (all distortion).

It can be inferred that the straightforward interpretation of (1) may not take into account the harmonic components that appear at frequencies that are non-integer multiple of the fundamental, referred to as 'interharmonics' in [26]–[28]. In the case of the MMC, interharmonic distortion might be especially important because f_{sw} is typically selected as a non-integer multiple of the fundamental (Section III). As a consequence, the effective switching frequency $f_{\text{eff}} = N f_{\text{sw}}$ is not necessarily an integer multiple of 50 Hz. Including interharmonics in the calculation of TDD is relevant because the associated switching harmonic sidebands will appear around the effective frequency and its multiples [29].

Fig. 8 shows the TDD calculated without interharmonics according to (1) as compared to the TDD calculated taking into account the interharmonics. It is observed that TDD is the same in both methods when the $f_{\text{eff}} = N f_{\text{sw}}$ is a multiple of 50 Hz, while for all other f_{eff}, the TDD is much lower if interharmonics are ignored. Thus, from here on, the TDD results presented include the interharmonic contribution.

B. Design Parameters Influence on Harmonic Performance

Simulation results for output current TDD with varying f_{sw}, N and L_{arm} are shown in Fig. 9. It can be observed that the TDD limit of $< 5\,\%$ is met for the majority of N and L_{arm} combinations with the $f_{\text{sw,min}} = 250\,\text{Hz}$ set by the capacitor balancing requirement for PS-PWM (refer Section III).

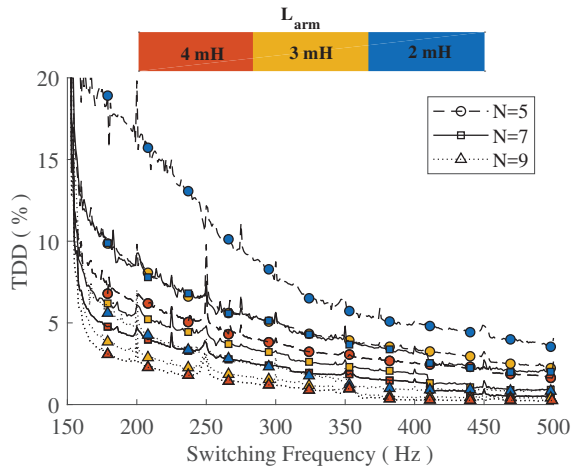


Fig. 9: Output current TDD with varying f_{sw} for different N and L_{arm}.

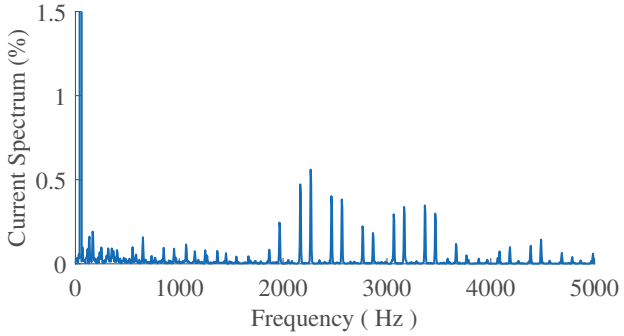


Fig. 10: Simulation results. Current spectrum (as percent from the fundamental) for $f_{\text{sw}} = 313\,\text{Hz}$, $N = 9$ and $L_{\text{arm}} = 3\,\text{mH}$.

However, the design must comply with the individual harmonic limits presented in Table I. As an example, the current spectrum for $N = 9$, $f_{sw} = 313\,\text{Hz}$ and $L_{\text{arm}} = 3\,\text{mH}$ is shown in Fig. 10. It can be observed that the switching harmonics appear around ($f_{\text{eff}} = 2817\,\text{Hz}$) and are not compliant for the limit of 0.3 % for the orders $35 \leq h < 50$.

The current spectrum should be checked for all combinations of N, f_{sw} and L_{arm} in order to see which ones achieve compliance. Before doing this, it is useful to limit the number of possible combinations by using the relation of f_{eff} with efficiency. If the $f_{\text{eff}} = N f_{\text{sw}}$ is chosen higher than 2500 Hz, then a significant part of the switching harmonic content will fall in a frequency range that it is not restricted in the requirements (as the TDD and the individual harmonic limits are defined until the 50^{th} order i.e. 2500 Hz). Since the sidebands $f_{\text{eff}} \pm 5f_0$ and $f_{\text{eff}} \pm 3f_0$ typically have high magnitude, it is suggested to consider the minimum effective frequency of $f_{\text{eff,min}} = 2750\,\text{Hz}$ (55^{th} order).

The optimal value of N for minimizing the total converter losses as a function of f_{eff} is given in [3]. For $f_{\text{eff}} = 2750\,\text{Hz}$, it is shown that $N = 9$ presents the highest efficiency with the considered operating conditions. Thus, N =9 is selected and to comply with the limits, either L_{arm} or f_{sw} can be increased.

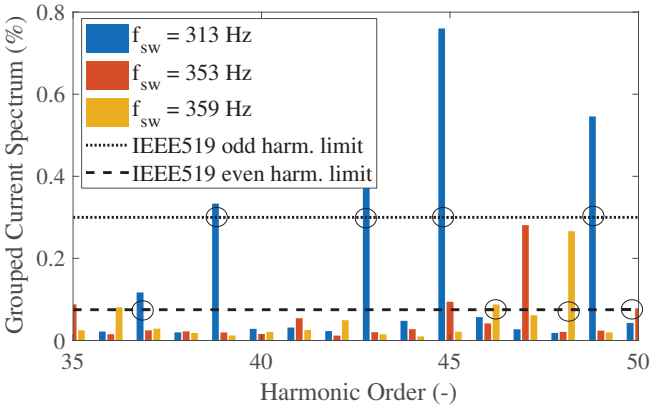


Fig. 11: Simulation results. Grouped current spectrum (as percent from the fundamental) for $N = 9$, $L_{\text{arm}} = 3\,\text{mH}$ and different switching frequencies.

$L_{\text{arm}} = 3\,\text{mH}$ is the minimum arm inductance required to prevent resonance with arm capacitances corresponding to $C_{\text{sm}} = 3.3\,\text{mF}$ (refer Fig. 3). Since it is proved in [3] that the efficiency of the converter for medium voltage high power application is conduction loss limited for $N = 9$, prime numbers of $f_{\text{sw}} > 305\,\text{Hz}$ are considered.

Fig. 11 shows the current spectrum for $35 \leq h < 50$ for different f_{sw}. As limits in Table I are defined for only integer harmonic frequencies, a grouping technique was applied, wherein the energy of the interharmonics was summed to the adjacent integer harmonic frequencies. For harmonic orders below 35 compliance was always met. However, for $N = 9$, $L_{\text{arm}} = 3\,\text{mH}$ and $f_{\text{sw}} = 313\,\text{Hz}$ (plot in blue), the individual harmonic limits are not met (violations are marked by a circle). The switching frequency was increased until all the harmonic orders were within limits, which happened for $f_{\text{sw}} = 353\,\text{Hz}$ (plot in red). It was observed that the limit was violated for a higher switching frequency of 359 Hz. This is possibly due to the way that the grouping techniques work: if one interharmonic happens to lie at a frequency closer to an odd harmonic number its energy will be added to an odd harmonic number, which will be beneficial for compliance because the permissible limits are higher for odd harmonic numbers than for even numbers.

It is therefore concluded that switching frequency ($f_{\text{sw}} = 353\,\text{Hz}$) achieves harmonic compliance for $N = 9$ and $L_{\text{arm}} = 3\,\text{mH}$ for the considered operating conditions. The final $f_{\text{eff}} = 9 * 353 = 3177\,\text{Hz}$ leads to an approximate semiconductor efficiency (associated with conduction and switching losses in submodules) of 99.3 % at full load according [3]. It can be inferred that this design choice maximizes the achievable efficiency while simultaneously complying with harmonic performance criteria in contrast with $N = 5$ or 7. At the same time, this design achieves reasonably low circulating current ripple ($\Delta I_{\text{c}} < 20\,\%$).

VI. Conclusion and Design Steps

The design trade-offs for high power medium voltage half bridge submodule based MMC in terms of number of levels,

arm inductance and switching frequency are shown. Based on the study, 3.3 kV IGBT based $N = 9$ SMs, $f_{\text{sw}} = 353$ Hz with PS-PWM modulation and $L_{\text{arm}} = 3$ mH was chosen as optimal design parameters for a 11 MVA, 10 kV line to line ac to 17.15 kV dc MMC. It was shown that with the chosen parameters, the individual SM were well balanced with a ripple close to $< 10\,\%$ average SM voltage ripple corresponding to $C_{\text{arm}} = 3.3$ mF. Further, the high frequency peak circulating current ripple ΔI_{c} is below 20 %. The harmonic performance of the output ac current is compliant with IEEE 519 standard while taking into account the interharmonics.

Based on the designed methodology in this paper combined with reference [3] the following selection process is suggested:

- For the given dc link voltage, the possible values of N corresponding to market available switch blocking voltage should be calculated. in this paper, the values can be 5, 7, 9, 17 or 24. These are optimized values based on average SM voltage ripple and IGBT safety factor [3].
- Determine the semiconductor losses (conduction+switching) as a function of effective frequency for different N [3].
- Choose the modulation technique depending on N. As a thumb-rule, PS-PWM is selected for low $N = 5$,7 and 9, while NLC+Sorting can be used for higher N.
- Define the minimum required frequency $f_{\text{sw,min}}$ depending on the capacitor voltage balancing need.
- Estimate the minimum arm inductance to ensure that there is no resonance with any possible inserted arm capacitance. Fault current rate of rise limiting requirements can be included in the consideration.
- Determine the harmonic performance of the converter at full load with varying f_{sw} and L_{arm} for different N and check if the TDD and individual harmonic limits comply in accordance to IEEE 519.
- Compare the possible candidate switching frequencies (preferably prime for capacitor voltage balancing needs) that give the minimum losses for the selected N and L_{arm} while being compliant with harmonic performance requirements.
- In case of similar efficiency and performance indicators, select the N, L_{arm} and f_{sw} that give lower peak circulating current.

The simulated waveforms of the optimally designed MMC in full load grid-connected operation are in the Appendix.

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APPENDIX
SYSTEM PARAMETERS AND DESIGNED MMC WAVEFORMS

The parameters of the simulated MMC are listed in Table II.

TABLE II: Test Converter Parameters

Parameter	Values
Power Capacity	11.12 MVA, pf=0.9
Line to line grid voltage	10 kV
Grid SCR	100
DC Link Voltage	17.15 kV
Submodule Capacitance	2-3.3 mF
Number of submodules	5, 7, 9
Arm Inductance	2-5 mH
Arm Resistance	0.1 Ω
Switching Frequency	150-500 Hz

Based on the study, it is concluded that $N = 9$, $f_{sw} = 353$ Hz and $L_{arm} = 3$ mH is compliant with the required harmonic performance limit with balanced SM capacitor voltages and low circulating currents. The controller bandwidths used in the simulations are indicated in [24]. The individual SM capacitor voltages with PS-PWM for the designed MMC is shown in Fig. 12.

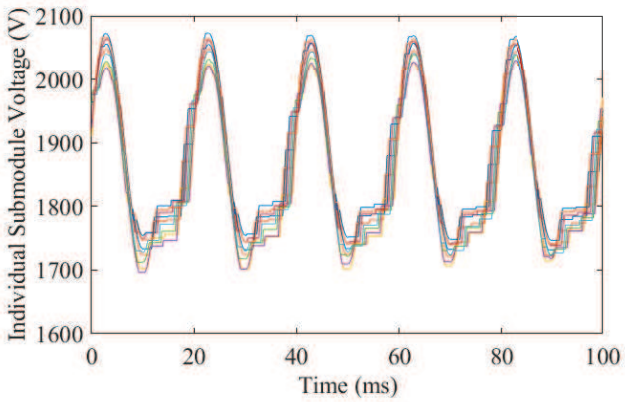

Fig. 12: Simulated individual SM capacitor voltages for the designed converter for 10-cycles at steady state full-load operation.

The simulated upper and lower arm sum capacitor voltages for submodule capacitance of 3.3 mF are shown in Fig. 13. The voltages are normalized with respect to the dc link voltage.

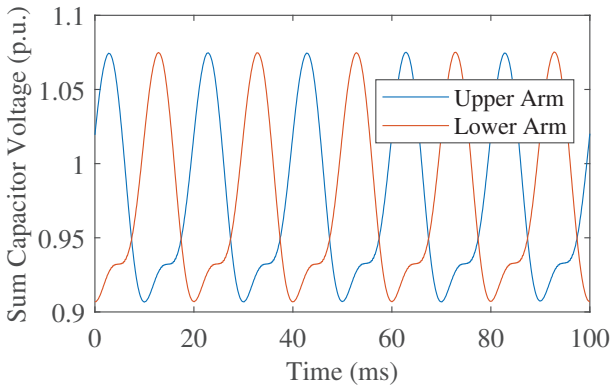

Fig. 13: Simulated upper and lower arm sum capacitor voltages for one phase of the designed MMC at steady state full-load operation.

The circulating and output current of the MMC is shown in Fig. 14. The waveforms are normalized with one-third of the rated dc link current and peak ac current respectively.

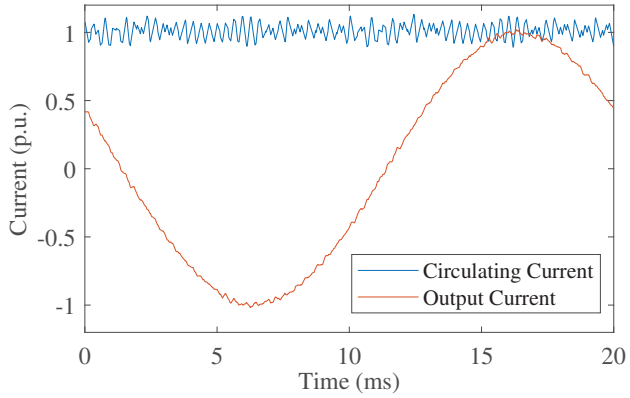

Fig. 14: Simulated circulating and output current for the designed MMC at full load.

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