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Integrated Digital and Analog Circuit Blocks in a Scalable Silicon Carbide CMOS Technology

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***Abstract*— The wide bandgap of silicon carbide (SiC) has attracted a large interest over the past years in many research fields, such as power electronics, high operation temperature circuits, harsh environmental sensing, and more. To facilitate research on complex integrated SiC circuits, ensure reproducibility, and cut down cost, the availability of a low-voltage SiC technology for integrated circuits is of paramount importance. Here, we report on a scalable and open state-of-the-art SiC CMOS technology that addresses this need. An overview of technology parameters, including MOSFET threshold voltage, subthreshold slope, slope factor, and process transconductance, is reported. Conventional integrated digital and analog circuits, ranging from inverters to a 2-bit analog-to-digital converter, are reported. First yield predictions for both analog and digital circuits show great potential for increasing the amount of integrated devices in future applications.**

***Index Terms*— 4H-SiC, integrated SiC electronics, silicon carbide, silicon carbide CMOS, wide bandgap.**

I. Introduction

SILICON carbide (SiC) is a wide-bandgap material that has been extensively researched over the past decades, especially for the application in power electronics [1], [2]. Together with galium nitride (GaN), the future market of wide-bandgap materials in power electronics is expected to be booming [3]. This foresight and the developed technologies pave the way for application in other fields as well [4]–[7], such as harsh environment sensing [8], [9] and ultraviolet detectors, though there are challenges for the next generation of devices to overcome [10].

The bandgap of 4H-SiC is 3.2 eV, which is almost three times larger than that of silicon [11]. This property allows for applications in higher operation temperatures, ultraviolet photodetection, radiation exposure resistance, and overall harsher environments [12], [13]. Development of discrete SiC components, such as MOSFETs and sensors, for operation in harsh environments is one side of the coin, whereas the other is the integration with on-chip electronics to allow for complete systems to be exposed to these harsh conditions.

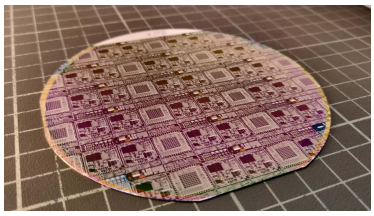

Fig. 1. Photograph of the 4 in SiC device wafer in the Fraunhofer IISB technology.

A decade ago, Raytheon Systems Limited developed a proprietary 1.2 μm SiC CMOS technology, called high temperature silicon carbide (HiTSiC), and demonstrated integrated circuits [14], [15]. The group of Mantooth at the University of Arkansas demonstrated a comparator [16], 8-bit digital-to-analog converter (DAC) [17], voltage and current references [18], gate driver [19], complex digital circuits [20], protection circuits in voltage regulators and switch-mode converters [21], digitally controlled pulsewidth modulation (PWM) generator [22], and data converters [23]. However, the HiTSiC technology was discontinued in 2018. Other in-house SiC CMOS technologies are reported by General Electric Global Research Center in the United States of America, for example [24], [25]. But in strong contrast with silicon services like Europractice, accessible SiC CMOS fabrication technologies are scarce to nonexistent.

Additionally, a promising SiC bipolar junction transistor (BJT) technology for high temperature and harsh environments, called high temperature power electronic systems with SiC integrated circuit (HOTSiC), was developed by the group of Zetterling at the KTH in Sweden [26], [27]. It is implemented by mesa etching in a complex epitaxial layer stack on top of a monocrystalline SiC wafer. In this technology, an OR/NOR gate [28], emitter-coupled logic (ECL)-based logic circuits [29], operational amplifier [30], differential amplifier [31], high current linear voltage regulator [32], and 8-bit DAC [33] were implemented and characterized up to 500 °C. Though BJTs and CMOS are the most popular flavors in silicon-based technologies, JFET [34], [35] and MESFET [36],

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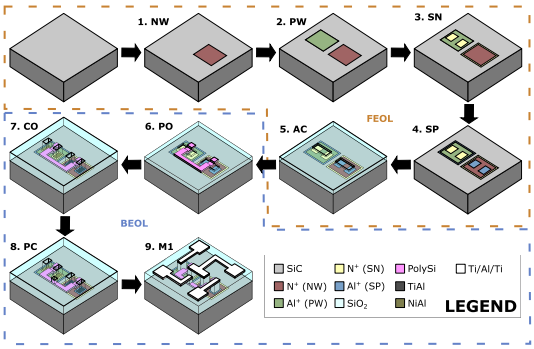

Fig. 2. Schematic of the fabrication steps of the Fraunhofer IISB 4H-SiC CMOS technology. The FEOL includes the definition of the doped NW, PW, SN, and SP regions, as well as the definition of the active area. The BEOL includes the definition of the polysilicon and metal interconnect layers, with corresponding silicide contacts and vias.

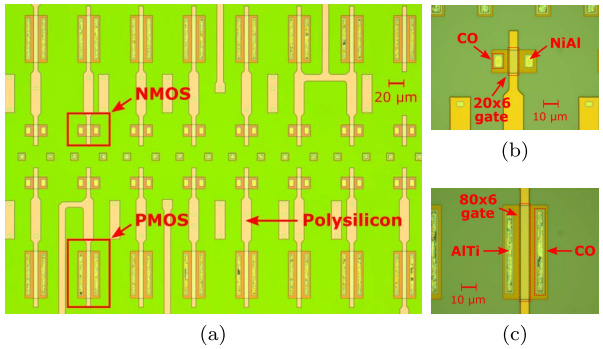

Fig. 3. Fabrication result after step 8 (PC), as illustrated in Fig. 2, of (a) multiple devices, (b) single 20 × 6 nMOS, and (c) 80 × 6 pMOS device. The formed silicides inside the contact openings are clearly visible. Note that none of the implanted regions can be observed.

[37] technologies have also been researched in the favor of stable operation at high temperatures. Although the MOSFET gate dielectric reliability has been a concern [38], [39], more recent work contradicts the poor reliability prediction and predict much longer lifetimes [40]. Moreover, CMOS technologies are typically preferred in mixed-signal circuit designs and have lower power consumption.

More recently, a promising new SiC CMOS technology candidate arose. This state-of-the-art 4H-SiC CMOS [41], [42] was developed by the Fraunhofer Institute for Integrated Systems and Devices Technology (IISB), based in Erlangen, Germany. The group of Mantooth at the University of Arkansas reported high-temperature memory SRAM cells [43] in this technology and Fraunhofer IISB demonstrated compatible UV photodetectors [44], [45] and temperature sensors [46].

This work reports on the state-of-the-art open 6 μm SiC CMOS technology, developed at Fraunhofer IISB, by providing an overview of the technology and results of implemented devices and circuits on a multiproject wafer design (Fig. 1). The completeness of this work is illustrated by the derivation of a selection of technology parameters for this technology and the inclusion of high-temperature operation up to 200 °C. The potential of this technology is moreover, reflected by some integrated analog and digital building blocks, that have been realized with good yield values. Future implementations in this technology will benefit from this work using the reported technology parameters and use of the building blocks toward increased performance and integration.

II. Technology Overview

The fabrication process steps of the Fraunhofer IISB 4H-SiC CMOS technology are illustrated in Fig. 2 for an inverter, where each step corresponds to a design layer. The starting substrate is a 350-μm thick 100 mm n-type 4H-SiC wafer with a 1–2 μm epitaxial n-type $>1 \times 10^{18}$ cm^{-3} buffer layer and an 8-μm epitaxial n-type 5×10^{14} cm^{-3} top layer. The front-end-of-line (FEOL) implements the doped regions by ion implantation, forming the n-well (NW), p-well (PW), shallow n-type (SN), and shallow p-type (SP), which are activated by a 1700 °C anneal for 30 min. The NW and SN are formed by N^+ implantation and the PW and SP by Al^+ implantation. The active area (AC) is implemented by wet etching the field oxide at the ohmic contact and MOSFET channel locations, followed by thermal gate oxidation. The resulting gate oxide thickness is 50 nm and the field oxide is 400 nm.

The back-end-of-line (BEOL) starts with implementation of a 500-nm polysilicon layer (PO), for the gate and short interconnects. An oxide passivation layer of 400 nm is deposited followed by the definition of ohmic contacts (CO) to the SN and SP layers in two steps. First, the openings to the SP layer are opened using a lithography mask, which is followed by the deposition and patterning of 80 nm/300 nm Ti/Al inside the openings. The procedure is repeated to form the openings to the SN layer and implements 50 nm NiAl patterns inside these openings. Rapid thermal annealing (RTA) at 980 °C is employed to form silicides in the contact openings, which ensures ohmic contacts from the metallization stack to the doped regions in the substrate. This is possible due to the high thermal stability of the present layers other than the contact metals. The final result is shown in Fig. 3. It should be noted that the patterned area of the metals in the contact openings is smaller than the etched openings, to avoid diffusion of these metals between the SiC–SiO_2 interface and generally into SiO_2 during the RTA. As a result, the CO design layer actually requires three separate lithography masks. Other metal stacks are investigated by Fraunhofer IISB [47], and ideally a single stack can be used to contact both the SN and SP regions simultaneously. The process then continues by opening the contacts to the polysilicon (PC). The metallization is completed by deposition and patterning of a 50 nm/700 nm/20 nm Ti/Al/Ti interconnect layer (M1). This reduces the thermal budget to 400 °C and should be adhered to in future implementations of multiple metal interconnect layers.

The dimensions of a NAND logic gate are included in Fig. 4 to illustrate the dimensions for the Fraunhofer IISB technology. This work includes a single metal interconnect layer, and polysilicon can be used as a second interconnect layer, at the cost of a larger sheet resistance and resulting in reduced frequency performance. The MOSFETs are implemented in the corresponding low-doped well that is connected to a highly doped guard ring. This helps reduce crosstalk or latch-up between the devices, but also means that one of the well types is electrically connected to the substrate. In this technology, n-type SiC substrates are used, which results in the electrical connection of all pMOS wells to the substrate. Devices that

TABLE I
MEAN VALUES OF THE SHEET RESISTANCES IN THE TECHNOLOGY AT ROOM TEMPERATURE, DERIVED FROM WAFER-LEVEL RESULTS OF 35 DIES. EACH DIE-LEVEL MEASUREMENT CONSISTS OF THE IV EXTRACTION FROM THE RESPECTIVE STRUCTURES, BIASED IN THE LINEAR REGION, FOLLOWED BY A LINEAR CURVE FIT. THE NW LAYER IS NOT REPORTED, AS IT IS CHALLENGING TO MEASURE DUE TO ITS IMPLEMENTATION DIRECTLY IN THE N-TYPE SUBSTRATE

Layer	Design ID	Sheet resistance
P-well	PW	$(431 \pm 19)\,\mathrm{k\Omega sq^{-1}}$
Shallow n-type	SN	$(1.03 \pm 0.01)\,\mathrm{k\Omega sq^{-1}}$
Shallow p-type	SP	$(40.4 \pm 1.3)\,\mathrm{k\Omega sq^{-1}}$
Polysilicon	PO	$(14.0 \pm 0.1)\,\mathrm{\Omega sq^{-1}}$
First metal	M1	$(47 \pm 3)\,\mathrm{m\Omega sq^{-1}}$

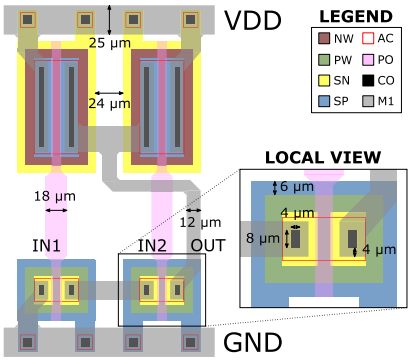

Fig. 4. Layout design example of a NAND logic gate in the Fraunhofer IISB SiC CMOS technology, highlighting several feature sizes. The inset shows the local feature sizes of an nMOS device, which is identical for the pMOS or scaled for the channel width. The logic gate is built from 20 μm $\times$ 6 μm nMOS and 80 μm $\times$ 6 μm pMOS devices. Note that the PC layer is not used in this logic block.

have channel widths above 200 μm are implemented through multiple fingers in parallel, within the same well and including a single guard ring.

III. PERFORMANCE

A. Technology Parameters

The reported structures are measured on wafer-level using a MicroTech Cascade probe station that is fitted with seven probe needles. The probe station is paired to an Agilant 4156C Precision Semiconductor Parameter Analyzer and IC-CAP measurement software. Measurements on higher temperature levels are performed on chip-level. The wafer-level results of the sheet resistance are listed in Table I. To evaluate the performance of the technology, the MOSFET threshold voltage, subthreshold slope, slope factor, and process transconductance are extracted from device measurements and reported in Table II.

The I_{ds}/V_{gs} curves of a selection of SiC nMOS and pMOS geometries at different temperature levels are measured and depicted in Fig. 5. The nMOS drain current scales as expected with the W/L ratio, which is less evident for the pMOS as it shows saturation effects. The pMOS current driving capability is very low, such that even the attached measurement equipment is a too large load. This is attributed to the relative large contact resistance and can be improved by optimizing the silicide to the p-type areas. The curves do show that this saturation effect is greatly reduced for increased W/L ratios, so that interfacing with off-chip loads is feasible.

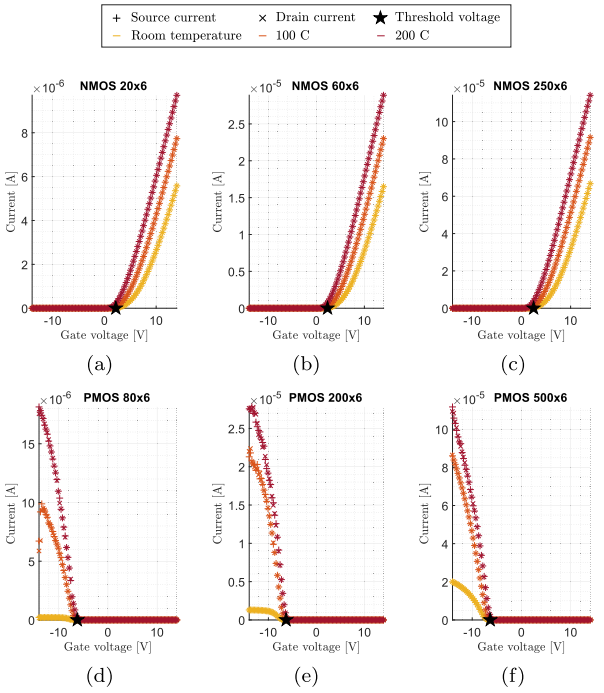

Fig. 5. Measured I_{ds}/V_{gs} curves at different temperature levels with marked threshold voltage on die (0,0) of (a) 20 μm $\times$ 6 μm nMOS, (b) 60 μm $\times$ 6 μm nMOS, (c) 250 $\times$ 6 μm nMOS, (d) 80 μm $\times$ 6 μm pMOS, (e) 200 μm $\times$ 6 μm pMOS, and (f) 500 μm $\times$ 6 μm pMOS SiC devices. The devices are biased in the linear region at 0.2 and -2 V for nMOS and pMOS, respectively. The source and drain currents are equal, indicating no leakage current.

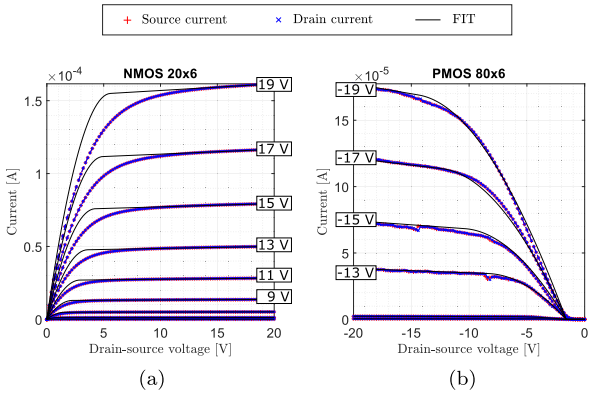

Fig. 6. I_{ds}/V_{ds} curves on die (0,0) for a selection of V_{gs} values and (a) 20 μm $\times$ 6 μm nMOS and (b) 80 μm $\times$ 6 μm pMOS devices. The curves are fitted to the unified model for manual analysis [48] and are achieved by assuming a $V_{dsat,n} = 2$ V, $V_{dsat,p} = -1$, $\lambda_n = 0.003$, and $\lambda_p = 0.01$. To account for deviation in the linear region, the transition point in the nMOS curves is moved to lower V_{ds} by a factor 1/3 and the pMOS curves are shifted to higher V_{ds} by -1.6 V. The source and drain currents are equal, indicating no leakage current.

The drain current magnitude for both nMOS and pMOS is highly dependent on temperature levels and shows less saturation effects for higher temperature. Furthermore, other parameters such as the mobility also improve with higher temperature, reaching 18.8 and 9.8 $\mathrm{cm^2V^{-1}s^{-1}}$ for the largest nMOS and pMOS, respectively. Related to this limited current driving capability is the increased V_{ds} bias, which reduces the saturation effect and allows extraction of some technology parameters. However, this increased bias is likely to shift the threshold voltage toward more negative values and reduce the

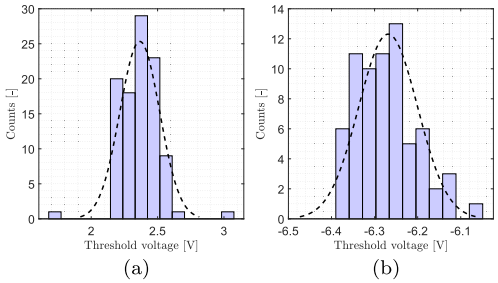

Fig. 7. Threshold voltage distributions of (a) nMOS and (b) pMOS devices, with a normal distribution fit in the dashed line that yields 2.37 ± 0.15 and -6.27 ± 0.07 for the nMOS and pMOS distribution, respectively. All device geometries in Fig. 5 are considered which totals 102 devices for each plot. The amount of histogram bins are 15 and 11 for the nMOS and pMOS result, respectively.

TABLE II

MEAN VALUES OF THE THRESHOLD VOLTAGE V_{TH}, SUBTHRESHOLD SLOPE S, SLOPE FACTOR n, PROCESS TRANSCONDUCTANCE PARAMETER k', AND MOBILITY μ IN THE TECHNOLOGY AT ROOM TEMPERATURE, DERIVED FROM WAFER-LEVEL RESULTS OF 35 DIES. THE SINGLE DEVICE YIELD IS HIGH (>97%), WITH ONLY ONE DIE CONSISTENTLY BROKEN. THE μ_p STANDARD DEVIATION IS HIGH DUE TO SIGNIFICANT NONLINEARITY IN THE I_{DS}/V_{GS} CURVES

nMOS devices			
size	$20\,\mu\text{m} \times 6\,\mu\text{m}$	$60\,\mu\text{m} \times 6\,\mu\text{m}$	$250\,\mu\text{m} \times 6\,\mu\text{m}$
$V_{th,n}$	(2.23 ± 0.12) V	(2.39 ± 0.12) V	(2.48 ± 0.07) V
S_n	(0.20 ± 0.03) V dec^{-1}	(0.20 ± 0.01) V dec^{-1}	(0.18 ± 0.02) V dec^{-1}
n_n	3.4 ± 0.5	3.3 ± 0.2	3.1 ± 0.4
k'_n	$(0.45 \pm 0.37)\,\mu\text{A V}^{-2}$	$(0.46 \pm 0.37)\,\mu\text{A V}^{-2}$	$(0.48 \pm 0.37)\,\mu\text{A V}^{-2}$
μ_n	(14.2 ± 2.6) cm^2 V^{-1} s^{-1}	(14.5 ± 0.4) cm^2 V^{-1} s^{-1}	(14.5 ± 0.3) cm^2 V^{-1} s^{-1}
pMOS devices			
size	$80\,\mu\text{m} \times 6\,\mu\text{m}$	$200\,\mu\text{m} \times 6\,\mu\text{m}$	$500\,\mu\text{m} \times 6\,\mu\text{m}$
$V_{th,p}$	(-6.25 ± 0.07) V	(-6.28 ± 0.07) V	(-6.26 ± 0.05) V
S_p	(0.25 ± 0.07) V dec^{-1}	(0.26 ± 0.09) V dec^{-1}	(0.26 ± 0.08) V dec^{-1}
n_p	4.2 ± 1.1	4.4 ± 1.5	4.3 ± 1.3
k'_p	$(0.33 \pm 0.26)\,\mu\text{A V}^{-2}$	$(0.39 \pm 0.30)\,\mu\text{A V}^{-2}$	$(0.38 \pm 0.29)\,\mu\text{A V}^{-2}$
μ_p	(0.1 ± 0.1) cm^2 V^{-1} s^{-1}	(0.2 ± 0.2) cm^2 V^{-1} s^{-1}	(0.1 ± 0.1) cm^2 V^{-1} s^{-1}

subthreshold swing. The reported asymmetry of the threshold voltages could be addressed in future work by means of a blanket p-type ion implantation to shift both nMOS and pMOS threshold voltages toward more positive levels.

The I_{ds}/V_{ds} curves for a selection of V_{gs} values and minimum size nMOS and pMOS devices are measured and depicted in Fig. 6. The nMOS drain current shows both quadratic and linear increase in magnitude for lower and higher V_{gs} values, respectively, illustrating that both saturation and velocity saturation are relevant. For the pMOS device, the behavior is close to linear increasing drain current, indicating mostly velocity saturation. The unified model for manual analysis [48] is fitted to the curves by empirical determination of the fitting parameters. To achieve a good fit, the transition point from linear to saturation of the nMOS devices is moved to lower V_{ds} levels and the starting point of the pMOS fit is shifted to higher V_{ds} levels. This shift for the pMOS also validates the higher V_{ds} used for the V_{th} extraction.

The threshold voltages V_{th} are extracted using the second-derivative method [49] and the distribution of the extracted values is given in Fig. 7. The subthreshold slopes S are extracted by considering the maximum of the inverse slope and are used to calculate the slope factors n [48]. The reported slope factors are far from the established silicon-based technologies [50], [51] that typically have $n < 2$. The process

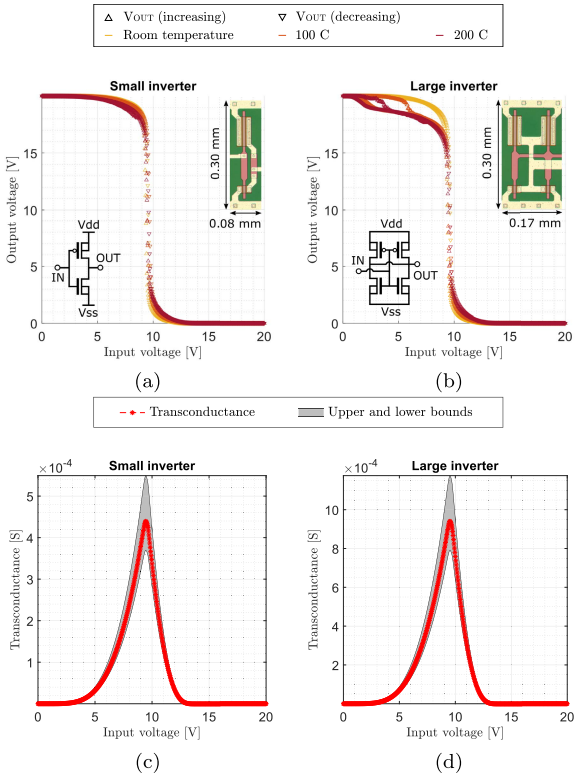

Fig. 8. Measured V_{out}/V_{in} curves at different temperature levels of (a) minimum size inverter and (b) large inverter and the calculated G_m/V_{in} curves of (c) minimum size inverter and (d) large inverter on die (0,0). The lower and upper limits of G_m are determined by considering the standard deviation of n and the insets show the respective circuits and micro photographs. The inverter yield is >97% over 35 dies for both variants, with only one die consistently broken.

transconductance parameter k' is extracted at high V_{gs} and V_{ds}, as the corrections to the fit do not allow extraction in the linear region. Therefore, k' is extracted at $V_{ds} = 20$ V and $V_{gs} > 5$ V or $V_{gs} < -12$ V for nMOS or pMOS, respectively. Finally, the device mobility is extracted in linear mode.

B. Digital and Analog Circuit Blocks

This SiC CMOS technology is currently rated for operation at a 20 V supply voltage with input and output signals in the same range. Future work would benefit from reducing this for better matching with standard ICs. The V_{out}/V_{in} responses of two inverter variants are given in Fig. 8(a) and (b), with corresponding circuits and micro-photographs in the insets. The small inverter is implemented in the minimum size nMOS ($20\ \mu\text{m} \times 6\ \mu\text{m}$) and pMOS ($80\ \mu\text{m} \times 6\ \mu\text{m}$). The large inverter connects two minimum size devices in parallel, which doubles the device W/L ratio. The only significant effect by increased temperature is a lower high output level of the large inverter. The switching voltages are found at the maximum I_{dd} current and equal (9.2 ± 0.7) V and (9.2 ± 0.5) V for the small and large inverter, respectively. The switching voltage V_m is calculated [48] through

$$V_m = \frac{\alpha\left(V_{\text{th},n} + \frac{V_{\text{dsat},n}}{2}\right) + \beta\left(V_{\text{dd}} + V_{\text{th},p} + \frac{V_{\text{dsat},p}}{2}\right)}{\alpha + \beta} \quad (1)$$

where $\alpha = k_n V_{\text{dsat},n}$ and $\beta = k_p V_{\text{dsat},p}$. This results in a switching voltage of 9.4 V, which is close to the measured

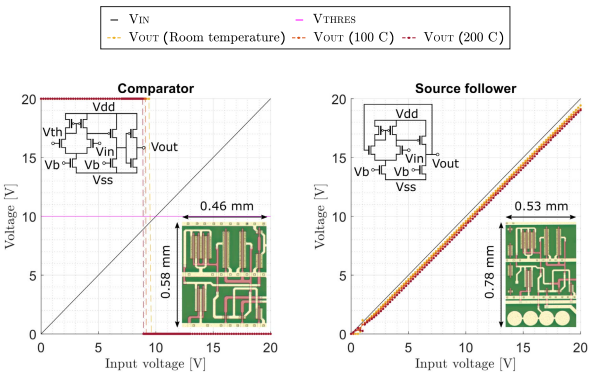

Fig. 9. Measured V_{out}/V_{in} curves at different temperature levels of (a) comparator for a threshold of 10 V and (b) source follower on die (0,0). Both circuits are biased at 1.5 V using an off-chip source and the insets show the respective circuits and micro photographs. All body contacts are connected to V_{ss} or V_{dd} for nMOS and pMOS, respectively.

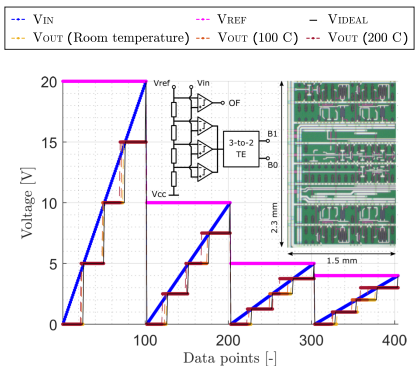

Fig. 10. Measured V_{out}/V_{in} curves of the 2-bit ADC at different temperature levels, for input ranges set by V_{ref} at 20, 10, 5, and 4 V on die (−3, −2). The circuit is biased at 1.5 V using an off-chip voltage source and the insets show the respective circuit and micro-photograph. The comparator in Fig. 9(a) and 20 kΩ SN resistors are used in this design.

value and therefore validates the parameters in Table II, as the inverter matches the assumption of high V_{ds} and V_{gs} for each device. Furthermore, a suggestion can be made for the geometry ratio of future implementations by calculating the ratio [48] for $V_m = 1/2 \cdot V_{dd}$ through

$$\frac{W_p/L_p}{W_n/L_n} = \frac{k'_n V_{dsat,n}\left(V_m - V_{th,n} - \frac{V_{dsat,n}}{2}\right)}{k'_p V_{dsat,p}\left(V_{dd} - V_m + V_{th,p} + \frac{V_{dsat,p}}{2}\right)} \quad (2)$$

which evaluates to 6 at room temperature, indicating that the current design ratio of 4 should be increased. Certainly, future improvements to the pMOS device should re-evaluate this ratio. The inverter logic gate can also be considered as a push-pull-based transconductance amplifier, with the inverter transconductance G_m given by adding the gate–drain small signal transconductance of the nMOS and pMOS devices [50]. The resulting G_m/V_{in} curves are given in Fig. 8(c) and (d) and the maximum transconductance is found at the switching voltage and equals to approximately 0.22–0.33 mS and 0.44–0.66 mS for the small and large inverter, respectively.

The dc characteristics of NAND and NOR logic gates over 26 dies were verified through investigation of every input combination and the resulting output voltage, with a tolerance of 10% ($V_{low} < 2$ V and $V_{high} > 18$ V). Two NAND gates are considered, one with the layout in Fig. 4 and one with an additional polysilicon crossover, with wafer-level yields of >93% and >88%, respectively. Similarly, two NOR gates are measured, both with a wafer-level yield of >88%. With a few logic gates, a digital 1-bit multiplexer (20 MOS devices, 0.44 mm × 0.58 mm) was implemented and verified over 26 dies with a wafer-level yield of >93%. Inverters and pass-gates are combined to implement a 1-bit analog multiplexer (8 MOS devices, 0.48 μm × 0.58 μm) and its operation was verified over 26 dies with a wafer-level yield of >92% or >84% for a maximum offset of 1 V (5% of total range) or 0.5 V (2.5% of total range), respectively. Increasing the device count further, a D-flip-flop block (66 MOS devices, 1.54 μm × 0.58 μm) was implemented and its operation verified over 26 dies with a wafer-level yield of >93%. This indicates that the true yield of single logic gates must be much higher than the given lower boundary, to achieve such high yield for the D-flip-flop.

A two-stage amplifier, implemented using an nMOS differential input pair and a common drain stage, with an output inverter, is considered as a comparator. The two stages are biased through a single off-chip voltage source of 1.5 V. The switching behavior of the comparator is measured for every integer $\{1, 2, \ldots, 19\}$ V level of the threshold voltage V_{thres} input for a linear increase sweep of the input voltage V_{in} over the entire range. The comparator V_{out}/V_{in} response for a V_{thres} of 10 V is given in Fig. 9(a), with corresponding circuit and device micro-photograph. When constraining the switching offset voltage to a maximum of 1 V (5% of total range) or 0.5 V (2.5% of total range), the comparator yield over 26 dies is >88% or >73%, respectively, at room temperature. Increased temperature also significantly increases the comparator offset and thus reduces its yield if considering the same maximum allowed offset.

A unity-gain buffer, or source follower, is implemented using the same two-stage amplifier architecture as in the comparator. The V_{out}/V_{in} response is given in Fig. 9(b), with the corresponding circuit and device micro-photograph. Typical behavior is the output of ∼0 V for low input levels (<2 V) and some devices also show clipping for high input levels. When constraining the mean offset voltage between input and output to a maximum of 1 V (5% of total range) or 0.5 V (2.5% of total range), the source follower yield over 26 dies is >92% or >80%, respectively, at room temperature. Similar to the comparator, the source follower offset increases with temperature.

Digital and analog blocks are combined in a 2-bit resistive ladder analog-to-digital converter (ADC) with a tunable input range (68 MOS devices) through V_{ref}, of which the response of four ranges is depicted in Fig. 10. The ideal ADC response V_{ideal} is included and the two digital output bits B_0 and B_1 are used to calculate the corresponding output voltage V_{out}. The overflow bit OF is not measured due to the 7 probe maximum taken into account in the layout design. The maximum differential nonlinearity (DNL) equals to 1.5 ± 0.5 LSB, the maximum integral nonlinearity (INL) equals to 1.3 ± 0.5 LSB, and the yield is >75% over 28 dies

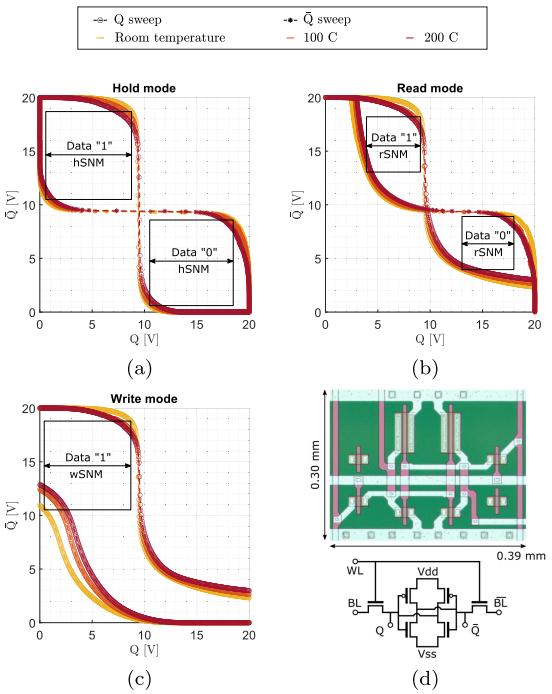

Fig. 11. Measured Q/$\bar{Q}$ SRAM cell butterfly curves for different temperature levels of (a) hold, (b) read, and (c) write mode including (d) circuit and micro-photograph on die (0, −2). A sweep of Q or $\bar{Q}$ and the maximum size squares are drawn for SNM derivation and a single sweep is depicted for the write mode in favor of readability. All body contacts are connected to V_{ss} or V_{dd} for nMOS and pMOS, respectively.

at room temperature. The larger offset of the comparators at higher temperatures translates to larger offsets of the ADC, especially in the lower operating ranges.

Finally, the characterization curves of a static random access memory (SRAM) cell in different modes, commonly known as the butterfly curves, are extracted to find the respective static noise margins (SNMs) that give indication of the data state stability. The reported SNM values are taken from the minimum between the data 0 and 1 cases. The wafer-level results over 28 dies have a yield of >85%. The hold mode, or standby mode, characteristics are depicted in Fig. 11(a) and represents two inverters connected in parallel in opposite direction as WL, BL, and $\bar{\text{BL}}$ are connected to ground. The corresponding hSNM equals to 7.1 ± 10 V, which is close to the ideal value of 10 V considering the technology supply voltage. The read mode characteristics are depicted in Fig. 11(b), which shows the effect of read stress on the ability of the device to pull the measured terminals to 0 V as WL, BL, and $\bar{\text{BL}}$ are connected to V_{dd}. As a consequence, the SNM is inevitably reduced and the corresponding rSNM equals to 4.4 ± 0.7 V. The write mode characteristics for the data 1 case are depicted in Fig. 11(c), of which the SNM derivation is slightly different as the largest square is drawn between the corresponding read and write mode curves. In this mode, WL and BL are connected to V_{dd} and $\bar{\text{BL}}$ to ground when sweeping Q, while BL and $\bar{\text{BL}}$ are swapped when sweeping $\bar{Q}$. The corresponding wSNM equals to 7.5 ± 0.9 V, which is even closer to the ideal value than the hSNM. All noise margins are reduced for the higher temperature levels, while retaining correct function. In comparison, the aforementioned results in the same technology of the group of Mantooth at the University of Arkansas found an hSNM and rSNM of 4.65 and 1.90 V, respectively, and did not report the wSNM [43]. The devices in this work have improved SNM values with a factor of 1.5 and 2.3 for the hSNM and rSNM, respectively.

The reports from devices to mixed-signal circuit implementations provide a thorough overview of the capabilities of the described technology. This open technology can be used in future implementations toward sensor integration and characterization in harsh environments.

IV. Conclusion

The state-of-the-art 6 μm 4H-SiC CMOS technology overview is given and design considerations are provided. The presented devices were additionally measured up to a temperature of 200 °C. A selection of technology parameters is extracted from devices on wafer-level through dc analysis, including the threshold voltage, subthreshold slope, slope factor, and process transconductance parameter. The CMOS devices are not characterized by a steep subthreshold slope (see Table II), so a slower transition between the off and on state is expected. This implies that future digital SiC CMOS electronics designed in this technology will need to operate at low frequencies. Furthermore, the minimum size inverter is used for the validation of parameters and a recommendation for increasing the future nMOS and pMOS device geometry ratio is provided. Future implementations would moreover benefit from the investigation of device gate lengths below 6 μm to reduce circuit footprints.

The single MOS device yield figures are high, considering the still premature level of integrated mixed signal technologies. Designed circuits with increased device count show similar yield levels >70%, further indicating great potential for future integration of higher device counts. The investigated blocks are inverters, NAND gates, NOR gates, 1-bit digital multiplexers, 1-bit analog multiplexers, D-flip-flops, push-pull transconductance amplifiers, comparators, source followers, 2-bit ADC and SRAM cells. Compared to previous work in the same technology, the SRAM cells have greatly improved the SNM values. The performance does not compare with the state-of-the-art silicon implementations, but shows correct function and could therefore be used in environments where silicon-based devices would not be functional at all. Future work will benefit from including higher-level interconnect and analysis of on-chip passives.

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