Direct Bonding of NbN for 3-D Chip Integration of quantum processors

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Direct Bonding of NbN for 3-D Chip Integration of quantum processors

by

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This thesis is confidential and cannot be made public until July 8th, 2019.

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The cover photo is cited and partially modified from [1].
Preface

This thesis is written as a partial satisfaction for the requirements of the Master of Science Degree in Microelectronics at the faculty of Electrical Engineering, Mathematics and Computer Science, at Delft University of Technology.

This work is about deposition and direct bonding of NbN films, which could be used for cryogenic applications, in particular quantum computer. The contribution of this work could lead to fabrication of multi-layered superconducting chip that operates beneficially in low-temperature environment above 4K, which is essential in building scalable quantum processors.

In this process, difficulties have arised and it was the help of many people that have brought this thesis to success. I would therefore like to thank the following people:

• Dr.R.Ishihara for his daily supervision and guidance during the course of my project.
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• To my peers, fellow master students that have experienced the same curriculum with me.
• My family for supporting me always.

Ye Li
Delft, July 2019
Abstract

3-D chip integration is considered to be the best way for further increasing the number of qubits on chip, and also for integration of qubits and readout electronics. Works have been done to stack two wafers with superconductive interconnections as a demonstration for feasibility of 3-D qubit integration. But all of them use an extra layer of adhesives, indium in particular, to join two neighboring planes. Indium is a good choice of adhesive for wafer bonding at cryogenic temperature. However, there are potential issues to employ this extra layer of adhesive. First, the critical temperature (Tc) of indium being 3.4K means it is suitable preferably for superconducting qubits, but not good enough for qubit implementations or other cryogenic that have above-4K expectations. Second, one general problem in wafer bonding is that alignment is not accurate. Adding an extra layer of anything increases the degree of misalignment.

In this work, the extra adhesive layer is abandoned and two wafers are bonded by direct-bonding technique. First, niobium nitride (NbN) is chosen to be the skeleton for this 3-D structure due to its high Tc (18K) as well as its simple composition hence easy fabrication. Sputtering is the method used to fabricate such metal nitride. Sample with Tc=15.6K has been measured so far. Second, both wafer-scale and miniaturized pattern are designed to measure contact resistance of direct bonding of NbN films in room and cryogenic temperature.

This work shows the potential of direct-wafer bonding in 3-D chip integration at cryogenic environment, and could further lead to scaling up of quantum processors.
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Introduction

1.1. Motivation

Over the past century, mankind has been experiencing the benefits and convenience of classical computing. Today’s computers help and entertain us, connect us with people all over the world, and allow us to process huge amounts of data to solve problems and manage complex systems.

However, there are problems that today’s systems will never be able to solve. For challenges above a certain size and complexity, there is not enough computational power on Earth to tackle them. To stand a chance at solving some of these complex problems, we need a new kind of computing: one whose computational power also scales exponentially as the system size grows.

With nearly 50 years of effort and progress in physics, materials science, and computer science, quantum computing, a scientific fantasy brought forth by Richard P. Feynmann [12], is gradually being transformed into reality.

Quantum computers could provide breakthroughs in many disciplines, including materials and drug discovery, the optimization of complex systems, and artificial intelligence. And today, there are already real quantum computers that can be accessed through the cloud (see figure 1.1), and many thousands of people have used them to learn, conduct research, and tackle new problems. But these quantum computers are still not capable of realizing those breakthroughs due to its small system size and hence low computational power.

![Figure 1.1: IBM first commercial quantum computer [2]](image)

In order to increase the computational power of quantum computing systems, improvements are needed along two dimensions. One is system size; the more qubits you have, the more states can in
principle be manipulated and stored. The second is to achieve lower error rates. We need to be able to manipulate the qubit states accurately and perform sequential operations that provide answers, not noise. In this thesis, though, the focus is more inclined towards increasing efficiently the size of a quantum computing system.

In most of the current qubit implementation, in particular, superconducting qubit, all qubits are confined to the same plane. Besides, the cavity resonators and transmission lines that are used for interconnection and communication between qubits are fabricated on the same plane with qubits themselves (see figure 1.2). This chip layout strategy is applicable given the implemented number of qubits is small, say, within tens of qubits [3, 13, 14]. Extending this approach to larger numbers of qubits, however, is impractical due to the interconnect crowding that will occur when addressing qubits within a larger two-dimensional array.

Furthermore, in current qubit-testing experiments, readout electronics and qubits are in different chips placed on different temperature stages in a refrigerator. The distance between the two stages is in typical tens of centimeters long, thus requiring tangible and bulky cables for connection. This would also be a problem as the qubit count increases since there will not be enough space inside a refrigerator for cables if each qubit can be addressable by the readout circuit.

Moving into the third dimension eases all such geometrical constraints. A 3-D chip structure affords not only significantly increased connectivity among qubits beyond just nearest-neighbor interactions, which is advantageous for many types of error-correcting codes other than just surface codes, but as well much closer distance between qubits and readout planes, avoiding the use of lengthy and bulky cables (see figure 1.3).

To reach the 3rd dimension is nothing new in traditional CMOS technology. 3D-IC has long been regarded as the best candidate to prolong Moore’s Law (see figure 1.4). And the most successful application of 3D integration comes from the CMOS image sensor industry, where they stack photodiodes on top of signal processors by direct bonding. This structure forms the very basis of the increasingly powerful cameras on our cellphone (see figure 1.5). The idea of this study is to introduce 3D-structure to chips that work in cryogenic environment.
1.2. Problem

Up to now there are a few demonstrations of 3-D chip structures that are potentially used for integration of multiple superconducting qubits. In a 2017 paper [15] the authors demonstrated daisy chain pattern to show superconducting connection between the bottom of the top chip and surface.
of base substrate. They used indium as a conducting adhesive to stick two chips together. In another paper people demonstrated superconducting TSV with Al.

In other papers [10, 16, 17] in which the demonstrations are more or less identical, they all used indium bumps to bond two separate chips. Indium is a very good choice of adhesive for wafer bonding at cryogenic temperature, due to its good wettability, low melting point, and and its soft at low temperature, also it is a superconducting material.

However, there are potential issues to employ this extra layer of adhesive. First, even though 3.4K is sufficiently high critical temperature for superconducting qubits, it is not good enough for cryogenic applications above 4K, the boiling point of liquid helium, which means extra cooling procedure is needed. Second, one general problem in wafer bonding is that alignment is not accurate, and this alignment error does not scale down with technology. Adding an extra layer of anything increases the degree of misalignment, so it might not be good for some applications where fine pitch and small size are desired, say, silicon qubits. Besides, the way adhesive works is that it needs to be melted first, the molten adhesive forms certain alloy with its neighboring material and then cools down and re-crystallizes. This whole process is to a certain extent uncontrollable in size.

1.3. Goal of this study

The goal of this study is aimed at direct-bonding two neighboring wafers with joints made of superconductive material (NbN) (see figure 1.6), which avoids the introduction of adhesive layers to bond neighboring wafers, and the bonding interface could still present superconducting electrical connections in cryogenic environment above 4K.

![Figure 1.6: Conceptual diagram of NbN-to-NbN direct bonding](image)

1.4. Organization of the thesis

The thesis starts by explaining some of the basic concepts about superconductivity and sputtering in Chapter 2 and then explains the methods and results on producing high-Tc superconductive NbN film by sputtering in Chapter 3. Chapter 4 explains the concept of thermo-compression bonding, one specific type of direct wafer bonding, and principles for characterization of sheet resistance and contact resistance. Chapter 5 gives the results of bonding two wafers with NbN films as joints, including the measurement result of room-temperature sheet resistivity and contact resistance of NbN. Finally, conclusions and recommendations are presented in Chapter 6.
2. Theory of Superconductivity and Physical Vapor Deposition

2.1. Superconductivity

In certain materials (called superconductors), a phenomenon of zero electrical resistance and complete expulsion of magnetic field (Meissner Effect) can occur simultaneously when the material is cooled down to a certain characteristic critical temperature ($T_c$). In 1908, a Dutch physicist Heike Kamerlingh Onnes successfully achieved the liquefaction of helium, by which materials can be cooled down to 4.2K. Shortly after that, in 1911, he found that the resistance in a solid mercury wire immersed in liquid helium suddenly dropped to zero (See Figure 2.1).

![Figure 2.1: First measurement of superconductivity](image)

Superconductivity is a quite fragile and unstable phenomenon. A proper ambient environment needs to be set up in order to maintain a material in its superconducting state. Not only does a rise in temperature but a rise in external magnetic field or internal current could easily destroy a superconducting state. For the maximum temperature ($T_c$), maximum magnetic field ($B_c$) and maximum current density ($J_c$) that a superconductor can endure, one can plot in 3 axes to form a critical surface that separates the superconducting state of a material from its normal resistive state (See Figure 2.2). The applied field ($B$), the temperature ($T$) and the current density ($J$) must be maintained below the critical surface in order to retain superconductivity. Since the three critical values are actually inter-dependent with no analytical explanation, the critical surface of a certain material is usually derived experimentally.

As mentioned, the superconducting state can be destroyed by a rise in the applied magnetic field, which penetrates the material and suppresses the Meissner effect. From this perspective, one distinction can be made between two types of superconductors (See Figure 2.3). Type-I materials remain in the superconducting state until a given threshold $B_c$ is reached. Above $B_c$, the field abruptly penetrates
into the material and turns the superconducting state into the normal state as the critical surface is crossed. Similarly, the Type-II superconductors could expel entirely the external magnetic field until $B_{c1}$ is reached. Yet as the magnetic field increases from $B_{c1}$ to $B_{c2}$, the material can tolerate local penetration of the magnetic field which forms loops with individual flux quanta (See Figure 2.4). This is an intermediate state where superconducting and non-superconducting areas coexist in the material which enables it to preserve its superconducting properties in the presence of relatively intense applied magnetic fields. Eventually, Type-II material goes into normal state for magnetic field even larger than $B_{c2}$.

Figure 2.3: Two types of superconductors

There have been many attempts trying to theorize the phenomenon of superconductivity, the most successful of which is the BCS theory, named after John Bardeen, Leon Cooper, and John Robert Schrieffer. The theory points out that with the mediation of lattice vibration (phonon), electrons in a superconductor are grouped in pairs, called Cooper pairs, and that the motions of all of the Cooper pairs within a single superconductor are correlated; they constitute a system that functions as a single entity. A crude model for how two electrons can form a coherent pair is shown in Figure 2.5. Each of the two electrons experiences a net attraction toward the nearest positive ion due to lattice vibration and then form a relatively stable electron pair. Since an individual electron is a fermion, the electron pair seen as an entity is a boson. Then the collection of these bosons is able to condense to form the superconducting state at low temperature.
2.1. Superconductivity

Figure 2.4: Scanning SQUID microscopy image of vortices in a 200-nm-thick YBCO (A Type-II Superconductor) film [6]

Figure 2.5: A crude model for phonon-mediated Cooper pair formation

Though the BCS theory has accomplished much success in explaining the behavior of many early found superconducting materials, it has its limitations on some of the recently found superconductors like cuprate superconductors and iron-based superconductors. These superconductors are termed as unconventional superconductors since their superconducting behavior cannot be theorized by the BCS theory. More specifically, the Cooper pair formation in unconventional superconductors is achieved much less by phonon mediation but some other mechanism that is highly material-dependent and yet to be fully determined. One of the thrills of the unconventional superconductors is that many of them have $T_c$ that is way higher that their conventional counterparts (see figure 2.6). It still remains an unrelenting and exciting research to find materials with $T_c$ above room temperature.

Figure 2.6: A Timeline of Superconductor $T_c$ from year 1900 to 2015 [7]
As of today, superconducting materials have been of great usage to human society. Due to the low-loss DC electric current flow in superconductors, high-field superconducting magnets are routinely utilized in modern laboratories, medical diagnosis (MRI, see Figure 2.7(a)), as well as transportation (maglev trains, see Figure 2.7(b)). Superconductivity also plays an important role in the field of quantum computation. Superconducting qubit is now considered to be the best candidate for the construction of a quantum computer, which is made possible with the employment of Josephson tunnel junction that is a strongly non-linear circuit element available only at low temperature. Besides, qubits have longer coherence time thanks to the low dissipation and hence low noise inherent to superconductors.

![Magnetic Resonance Imaging (MRI)](image1) ![Magnetic Levitation (MagLev) Train](image2)

**Figure 2.7: Examples of Superconductivity Applications**

### 2.2. Physical Vapor Deposition

Physical Vapor Deposition (PVD) is a process of thin film deposition where target material is vaporized in a high vacuum chamber and then deposited on a substrate. Vaporization of the target material is usually done by heating the target directly or by bombarding the target with a gas that is often referred to as the sputter gas due to its function. PVD is also called sputtering when a sputter gas is employed, injected via an gas inlet into the chamber (See Figure 2.8).

![Illustration of a typical sputtering chamber](image3)

**Figure 2.8: Illustration of a typical sputtering chamber**

A sputtering process begins with that a stray electron near the target is accelerated towards the substrate by a large applied electric field and collides at halfway with a neutral sputter gas atom converting it to a positively charged ion. The collision results in two electrons which can then collide with other sputter gas atoms and ionize them, creating a cascading process until the gas breaks down and turns into plasma ready for use. In the mean time, the ionized sputter gas atoms are also accelerated towards the target, knocking off target atoms that will be ejected onto the substrate and form a rather
2.2. Physical Vapor Deposition

The microscopic image of an $Ar^+$ ion hitting the target is not very different from the collision between a cue ball and an object ball in billiards. The mechanisms behind are momentum conservation and energy conservation. In any collision, momentum is always conserved. The incident angle of $Ar^+$ ions has a big influence on the emission of target atoms. For example (See Figure 2.9), at normal incidence of ions, the primary collision can not eject an atom off the surface but the secondary collision can. Yet at oblique incidence, primary collision can directly result in ejection. The energy may also be conserved if the collision is elastic. In the case of sputtering, since the energy of incident $Ar^+$ ion is way larger than the bonding energy of target atoms, the collision can be regarded as elastic. Many types of process can take place at the target surface given the different incident $Ar^+$ ion energy (See Figure 2.10 and Table 2.1). In order to increase the sputter yield, namely to increase the number of sputtered-off target atoms for each incident $Ar^+$ ion, both the angle and energy of the ions need to be set properly (See Figure 2.11). Besides, binding energy of target atoms, relative mass of ions and atoms, as well as target temperature are also major concerns.

![Collision process](image)

(a) Collision process for $Ar^+$ with normal incident angle

![Collision process](image)

(b) Collision process for $Ar^+$ with oblique incident angle

**Figure 2.9:** Billiard-type collision process for incident $Ar^+$ with target atoms

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<td>Sticking or Reflection</td>
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<tr>
<td>Surface damage and Migration</td>
<td>5 eV ~ 10 eV</td>
</tr>
<tr>
<td>Sputtering</td>
<td>10 eV ~ 3000 eV</td>
</tr>
<tr>
<td>Implantation</td>
<td>3000 eV and above</td>
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**Table 2.1:** Typical values of incident ion energy and its corresponding target surface process type

Sputtered atoms from the target will diffuse all the way through the plasma to the substrate that is on the other end of the chamber. During their journey, the sputtered atoms will inevitably collide with the plasma particles ($Ar$, $Ar^+$, electrons), which slows the deposition rate, namely how fast the film is
10 2. Theory of Superconductivity and Physical Vapor Deposition

Figure 2.10: Interactions of sputter gas ions with target surface

Figure 2.11: Optimal energy and incident angle of sputter gas ions for high sputter yield

... deposited on the substrate. But on the other hand, the higher the ion density, the more atoms can be sputtered off the target in the first place, and the deposition is correspondingly faster. So there is an optimization on the argon plasma density to give the highest deposition rate (See Figure 2.12).

Another method that is adopted in most of the modern PVD equipmentss to increase the deposition rate is put a magnetron source behind the target (See Figure 2.13). The principle is that the target surface is immersed in a magnetic field such that primary and secondary electrons are trapped in a localised region close to the target into an endless round ‘racetrack’ as the $\vec{E} \times \vec{B}$ drift currents close in on themselves. As Figure 2.10 shows, when an incident $Ar^+$ hits the target, it may get an electron and reflect as a neutral Ar atom. Then this Ar atom could be later ionized again and retrieve its previous role as a sputter-er. With a magnetron source, the chance of stray electrons experiencing an ionising collision with an Ar atom is vastly increased and ionisation efficiency is increased too. Effectively there are more $Ar^+$ ions recycled per unit time to bombard the target and hence an enhancement of deposition rate. This also causes the impedance of the plasma to drop and the system to operate at much lower voltages than its magnetron-less counterparts (say, 500-600 V as compared with several kV).
2.2. Physical Vapor Deposition

2.2.1. Reactive Sputtering

When a reactive gas is added to the sputtering process, it is even possible to deposit compounds on the substrate (See Figure 2.14). This process is called reactive sputter deposition. The reaction is most likely to take place at the target surface since there is larger energy released when incident ions bombard the target. Since the purpose of this thesis is to produce NbN films, the target is chosen to be pure Nb and the reactive gas is \( \text{N}_2 \).

Film stoichiometry is an important parameter for optimizing functional properties like the stress in
$SiN_x$ or the index of refraction of $SiO_x$ as well as, in the context of this thesis, the $T_c$ of $NbN_x$. In order to produce high-$T_c$ NbN film by reactive sputtering, one important consideration is the partial pressure of the reactive gas inside the chamber, because the composition of the film can be controlled by varying the relative pressures of the inert and reactive gases.

The mechanism is that as the partial pressure of reactive gas in the chamber is increased, the outermost surface of the metal target will transit from a purely metallic state to a purely nitride state (often called the ‘poisoned’ state). Depositing at high rates with good NbN film stoichiometry hence high $T_c$ requires that the target be consistently kept in a fixed ‘transition’ state somewhere between the purely metallic and poisoned state.
3

Experiment Setup and Result
Discussion of PVD for high-Tc NbN film

3.1. Experimental Setup
3.1.1. Trikon Sigma 204

The NbN films are deposited in a cryo-pumped magnetron sputtering system (Trikon Sigma 204). A detailed overview of the deposition chamber and pumping system of the machine is given in figure 3.1 and figure 3.2.

Figure 3.1: Chamber vacuum Pumping-Functional
3. Experiment Setup and Result Discussion of PVD for high-Tc NbN film

By looking at a simplified version (see figure 2.8) of the chamber shown in figure 3.2, the distance between target and substrate, defined as stand-off distance, is about 5.2 cm. In between there is an optional physical collimator/shutter that blocks sputtered atoms whose emergent angle are too large to be deposited on the substrate. Atoms with low angles are able to get down into high aspect ratio features much more effectively than those with higher angles. The Nb target has a circular shape with 332 mm diameter, 7 mm thickness. The volume of whole chamber is about 24 liters. There are multiple sensors in the chamber that record during deposition parameters like discharge voltage, substrate temperature, and chamber pressure, etc.

3.1.2. Dipstick in Liquid Helium and IVVI Rack

The measurements of superconductivity of films are performed at temperature between 4.2 K and 20 K, reached by fixing sample on one end of the dipstick and immersing it in a dewar of $He^4$. Inside the dewar there are three walls and two gaps to prevent the thermal exchange by forms of convection, conduction or radiative flux between the $He^4$ liquid and ambient environment (see figure 3.3).

Close contact between the sample and helium liquid could only fix the sample temperature at 4.2 K, which is not desired to determine the critical temperature of a material. In order to sweep the temperature in $He^4$ environment, a vacuum can is employed to create a certain spacing between the sample and helium liquid (see figure 3.4). Besides, a heater and a temperature sensor are also required for tuning and keeping track of the sample temperature. For faster cooling of the sample, contact gas (vapor $He^4$) is usually injected into the vacuum can so that there is an efficient thermal path between the sample and $He^4$ liquid, which is via the contact gas instead of the hollow dipstick.

Before inserting the dipstick into a dewar full of $He^4$, a good vacuum (below $10^{-5}$ mBar) must be reached inside the tube and the vacuum can because any trace of water vapor or $N_2$ will be solidified at low temperature to take up more volume and potentially induce leakage into the can during measurement. This would not only make temperature adjustment difficult, but also raise safety issues as
3.1. Experimental Setup

Figure 3.3: Illustration of Dipstick in a $He^4$ Dewar

(a) The end of a dipstick without vacuum can
(b) The end of a dipstick with vacuum can

Figure 3.4: The end of a dipstick before vacuuming

the heater directly boiling a large amount of $He^4$ could lead to explosion.

Inside the hollow tube of the dipstick, there are multiple cables linked between the sample and the IVVI rack for electrical signal transmission. In order to measure the resistance in 4-point Kelvin fashion (see figure 3.5), two cables connect a current source module ($S_{IV}$ V-I module) and the matrix module, the current signal then goes from the matrix module all the way down into the sample through the tube. Another two cables pick the voltage signal from the sample and deliver it back into the matrix module and eventually feed into voltage measure module ($M_{3m}$ V-measure module). A module alongside ($M_{iso}$ Dual Iso-out module) will copy the voltage signal of $M_{3m}$ module and sends it to a voltage meter below for display. Heater control is realized by employing a. Also, there is another cable in the tube that records the sample temperature and sends it to the temperature controller in the rack (see figure 3.6).
3.1.3. NbN Sample on PCB

The deposited NbN films are diced and mounted on a small printed wire board (PCB) for cryogenic measurement (See Figure 3.7). The mounting procedure is achieved by gluing the samples on PCB using paste silver with good thermal conduction. Al wire is used to connect the sample surface to the pads on PCB on a wirebonder. In principle only 4 wires are needed to conduct Kelvin resistance measurement, more wires are bonded in reality in case of incomplete wielding. The PCB is then hooked to the end of a dipstick which will be later immersed in liquid $He^4$. It usually takes about half an hour for the sample to cool down to 4.2K as can be shown by the temperature controller on the IVVI rack. Programme has been written in computer to sweep the temperature and measure the film resistance.
3.2. Results and Discussion

3.2.1. Discharge Voltage and Chamber Pressure

In Figure 3.8, NbN film is deposited on 525-μm p-type (100) Si wafer (See Figure 3.10) by dc magnetron sputtering in Trikon Sigma 204, using 99.95% pure Nb target. A small opening is made by putting a piece of wafer fragments on top of the Si wafer before sputtering and removing it after sputtering. The purpose is to measure the step height and hence the thickness of the deposited NbN film.

The three curves represent the different discharge power set in the chamber: 1kW, 3kW and 5kW respectively. The plate temperature is set as 350°C and the Ar flow rate is 100 sccm. The only parameter that changes for each deposition along one curve is the \( N_\text{2} \) flow rate, ranging from 0 sccm to 100 sccm. After each deposition the Nb target is cleaned using a specialized recipe to remove target surface contamination as well as nitried layer that have accumulated on the target surface during the deposition. This cleaning procedure could remove the notorious hysteresis of the curve that often appears due to target nitridation [18]. In each deposition, the deposition time is set long enough (174 seconds) for the plasma to reach equilibrium before the discharge voltage and chamber pressure are noted down.

![Figure 3.8: Discharge voltage as a function of \( N_\text{2} \) flow rate. A clear steep slope appears as \( N_\text{2} \) flow rate increases](image)

As mentioned in 2.2.1, in order to produce high-\( T_\text{c} \) NbN film by reactive sputtering, the partial pressure of \( N_\text{2} \) inside the chamber plays an important role as it controls the target surface to be either in metallic state or nitrided state. Figure 3.8 gives the method to find the transition point between the two state. The figure shows the target voltage in the deposition chamber of Trikon 204 as a function of the \( N_\text{2} \) flow rate for different discharge power. As can be clearly seen, given a certain discharge power, a steep slope shows up in the curve as \( N_\text{2} \) flow rate reaches a certain amount. For 1KW the abrupt slope change happens when \( N_\text{2} \) flow rate is around 25 Sccm, for 3KW around 60 Sccm and for 5KW around 90 Sccm. The mechanism behind this phenomenon is that as \( N_\text{2} \) becomes abundant in the chamber, NbN film is not only formed on the substrate as desired, but also on the sputter target. Since NbN is less conductive than pure Nb, the target poisoning causes the discharge current to decrease while the discharge power is held constant. As the discharge power increases, the ion flux hitting the target becomes stronger, making it more difficult for NbN to accumulate on the target surface. Therefore, to reach the poisoned state of the target, more \( N_\text{2} \) needs to be injected into the chamber, which explains why the sharp slope appears at larger dose of \( N_\text{2} \) for higher discharge power.

The transition from metal state to nitrided state of the target can also be manifested by the curve of chamber pressure versus \( N_\text{2} \) flow rate. The NbN film formed on the target surface would block \( N_\text{2} \) from proceeding the reaction with target, which would cause the pressure to increase inside the chamber
Experiment Setup and Result Discussion of PVD for high-Tc NbN film

Figure 3.9: Chamber Pressure as a function of $N_2$ flow rate. Only a small slope change appears as $N_2$ flow rate increases.

Figure 3.10: NbN film deposited on Si substrate. A rectangular opening is made during deposition intended for film thickness measurement.

since more $N_2$ is injected by not reacted. So it is expected that the curve of chamber pressure versus $N_2$ flow rate would also display a drastic change of slope as $N_2$ increases to the amount same as those in Figure 3.8. Figure 3.9 shows the curve of chamber pressure versus $N_2$ flow rate, but the slope change is not so apparent as is in the case of Figure 3.8. Detailed reason remains to be explored.

3.2.2. $T_c$ Measurement of NbN Films

Figure 3.11 picks 5 points from the 3KW curve in Figure 3.8 and additionally attaches the result of $T_c$ measurement of NbN films that are deposited under those 5 different $N_2$ flow rate. As can be seen from the figure, films that are deposited under the elevating $N_2$ flow rate first show an increase and then decrease in $T_c$, and the film that exhibits the highest $T_c$ (15.2K) are located right at the steep slope of the curve of discharge voltage versus $N_2$ flow rate. This conforms to the theory mentioned in 2.2.1 that at the transition state of the target the deposited NbN film exhibits the highest critical temperature.

The subplot in Figure 3.11 shows the resistance measurement of the sample deposited at 75 $N_2$ flow rate with temperature sweeping from 13K to 16K. The resistance measured at each point of the sweeping temperature is normalized to the resistance at 16K where superconductivity vanishes for sure. Since the temperature sensor measures the temperature of the PCB rather than that of the sample, there is always a delay as heat transfers from the PCB to the sample: As the sweeping temperature rises, the PCB temperature is already higher than the $T_c$ of the sample; as the sweeping temperature declines, the sample reaches $T_c$ later than the PCB, hence the hysteresis of the resistance curve during measurement. So the real $T_c$ of the sample should be in between the uprising points of two curves. Middle point is a reasonable value to pick, which gives 15.2K.

Notice that at 0 Sccm of $N_2$ flow rate the deposited film is not NbN but pure Nb. Nb is also a
3.3. Comparison and Discussion

Figure 3.11: Target Discharge Voltage as a function of $N_2$ flow rate with measured $T_C$ attached. Subplot gives the normalized resistance versus computer-controlled sweeping temperature.

superconductor and its $T_C$ is reported to be around 10K. So it should come with no surprise that the $T_C$ of pure Nb is higher than that of a poorly stoichiometric NbN deposited at $N_2$ flow rate of 25 Sccm.

3.3. Comparison and Discussion

Magnetronsputteringhasbeenaprettydevelopedmethodfordepositionofsuperconducting NbN film. Besides, due to the relatively simple composition and few stoichiometric choices of NbN, other deposition methods have also been employed to produce NbN with high $T_C$. Table 3.1 gives a list in chronological order of $T_C$ demonstrated of NbN.

In general, $\sigma-NbN$ exhibits the highest $T_C$ among all the phases of NbN. As long as the phase is correct by fabrication, $T_C$ in the range of 15K–18K can always be achieved. The slight difference within this range may be set by different choice of substrate material and substrate temperature during deposition. The substrate temperature plays a more important role as elevated temperature improves the crystalline order in the films and increases the grain size. Ideally, the film would exhibit the best superconducting properties in terms of $T_C$ and critical current if the whole film consists of only 1 large grain. As for substrate material, it only affects the lattice constant of NbN at the interface region, and the effect becomes less when the thickness of the deposited film grows.
### Table 3.1: $T_c$ Comparison of NbN films in Chronological order

<table>
<thead>
<tr>
<th>Work</th>
<th>Year</th>
<th>Approach</th>
<th>Substrate Temperature</th>
<th>Substrate Material</th>
<th>$T_c$</th>
</tr>
</thead>
<tbody>
<tr>
<td>[19]</td>
<td>1971</td>
<td>RF Reactive Magnetron sputtering</td>
<td>760°C</td>
<td>Fused Quartz</td>
<td>17.3K</td>
</tr>
<tr>
<td>[20]</td>
<td>1973</td>
<td>DC Reactive Magnetron sputtering</td>
<td>600°C</td>
<td>Fused Quartz</td>
<td>15K</td>
</tr>
<tr>
<td>[21]</td>
<td>1979</td>
<td>RF Reactive Magnetron sputtering</td>
<td>600°C</td>
<td>Not Shown</td>
<td>16K</td>
</tr>
<tr>
<td>[22]</td>
<td>1983</td>
<td>DC Reactive Magnetron sputtering</td>
<td>90°C</td>
<td>Sapphire</td>
<td>14.2K</td>
</tr>
<tr>
<td>[23]</td>
<td>1983</td>
<td>DC Diode sputtering</td>
<td>90°C</td>
<td>Sapphire or Si</td>
<td>14.2K</td>
</tr>
<tr>
<td>[24]</td>
<td>1985</td>
<td>DC Reactive Magnetron Sputtering</td>
<td>80°C</td>
<td>Glass, Glazed Ceramic, Fused Quartz, or Sapphire</td>
<td>15.7K</td>
</tr>
<tr>
<td>[25]</td>
<td>1986</td>
<td>DC Reactive Magnetron Sputtering</td>
<td>450°C</td>
<td>Glass, Glazed Ceramic, Fused Quartz, or Sapphire</td>
<td>16K</td>
</tr>
<tr>
<td>[26]</td>
<td>1987</td>
<td>DC Reactive Magnetron Sputtering</td>
<td>50°C</td>
<td>Si or Glass</td>
<td>14.7K</td>
</tr>
<tr>
<td>[27]</td>
<td>1987</td>
<td>DC Reactive Magnetron Sputtering</td>
<td>150°C</td>
<td>Si</td>
<td>15.8K</td>
</tr>
<tr>
<td>[28]</td>
<td>1994</td>
<td>Pulsed Laser Deposition</td>
<td>600°C</td>
<td>MgO</td>
<td>16.6K</td>
</tr>
<tr>
<td>[29]</td>
<td>1996</td>
<td>RF Reactive Magnetron Sputtering</td>
<td>100°C</td>
<td>MgO</td>
<td>16K</td>
</tr>
<tr>
<td>[30]</td>
<td>1999</td>
<td>Pulsed Laser Deposition</td>
<td>600°C</td>
<td>MgO</td>
<td>16.6K</td>
</tr>
<tr>
<td>[31]</td>
<td>2009</td>
<td>Ion-Beam-Assisted Deposition</td>
<td>450°C</td>
<td>MgO or TiN</td>
<td>14K</td>
</tr>
<tr>
<td>[32]</td>
<td>2012</td>
<td>DC Reactive Magnetron Sputtering</td>
<td>600°C</td>
<td>MgO</td>
<td>15.5K</td>
</tr>
<tr>
<td>[33]</td>
<td>2012</td>
<td>Plasma-Enhanced Atomic Layer Deposition</td>
<td>400°C</td>
<td>Amorphous Aluminum Axide</td>
<td>10K</td>
</tr>
<tr>
<td>[34]</td>
<td>2013</td>
<td>DC Reactive Magnetron Sputtering</td>
<td>600°C</td>
<td>Si</td>
<td>14.8K</td>
</tr>
<tr>
<td>[35]</td>
<td>2014</td>
<td>DC Reactive Magnetron Sputtering</td>
<td>150°C</td>
<td>Si</td>
<td>14K</td>
</tr>
<tr>
<td>[36]</td>
<td>2016</td>
<td>Chemical Vapor Deposition</td>
<td>1300°C</td>
<td>Sapphire</td>
<td>17.6K</td>
</tr>
<tr>
<td>[37]</td>
<td>2017</td>
<td>DC Reactive Magnetron Sputtering</td>
<td>760°C</td>
<td>3C-SiC/Si</td>
<td>13.3K (4.7nm thick)</td>
</tr>
<tr>
<td>[38]</td>
<td>2017</td>
<td>Atomic Layer Deposition</td>
<td>300°C</td>
<td>Sapphire</td>
<td>12.35K</td>
</tr>
<tr>
<td>This work</td>
<td>2019</td>
<td>DC Reactive Magnetron Sputtering</td>
<td>350°C</td>
<td>Si</td>
<td>15.2K</td>
</tr>
</tbody>
</table>
4.0.1. Thermo-Compression Wafer Bonding

Thermo-Compression bonding is a technique to achieve wafer bonding by inter-diffusion of metal atoms with the aid of elevated temperature and pressure. It is also referred to as diffusion bonding, thermo-compression welding, solid-state welding or pressure joining. There are in general 3 distinctive mechanisms in the process of bonding [11]:

1. Solid-phase plastic deformation
2. Diffusion
3. Melting and Solidification

The three mechanisms contribute separately or in combination to the establishment of material continuity in every bonding process.

Plastic deformation is achieved by bringing two pieces of bonding materials sufficiently close to each other so that the atoms on the two surfaces can establish an equilibrium spacing as the result of atomic attraction. In this mechanism, atoms stay where they were and the only change happens at the interface of the two bonding materials.

Diffusion involves transport of atoms from one piece to another across the contact interface. Based on location and sequence, the diffusion process can be classified into:

1. Surface Diffusion
2. Grain boundary diffusion
3. Bulk diffusion

In surface diffusion, atoms may jump across or along the interface during bonding. Then the exotic atoms begin to diffuse along the grain boundary of the material in grain boundary diffusion. After the exotic atoms take hold of the grain boundary, they begin to diffuse into the grain in bulk diffusion. The whole process can be illustrated in figure 4.1. Since the bonding interface is usually also grain boundary, the process of grain boundary diffusion bulk diffusion can happen simultaneously.

Melting leads to the breaking of the crystalline order inside the bulk of the bonding materials. With the material in melted state, gross mass and atom transport is enabled without the limit of the molecular or metallic bonds. Solidification then restores the crystalline order through flow and microscopic transport. The two-step process reshuffles the atomic arrangement from both sides of the bonding material in a quick and drastic manner compared with diffusion. For solid-state bonding, which thermo-compression bonding belongs to, melting and solidification are not included as materials are turned into liquid form during the process. So solid-state bonding is also called non-fusion bonding.
Figure 4.1: Illustration of three types of diffusion processes during bonding: (a) Grain boundary diffusion (b) Bulk diffusion (c) Surface diffusion

The quality of solid-state bonding relies on plastic deformation and diffusion. In thermo-compression bonding, this is achieved with the simultaneous application of force and heat. The relative amounts of applied heat and pressure needed to create strong bonding vary in different cases, depending heavily on the surface treatment and materials to be bonded. Very high heat and little pressure can render bonding due to high diffusion rate at elevated temperatures. Little heat but with high pressure can also lead to bonding by forcing atoms together via plastic deformation. Despite the variation, the microscopic mechanism for the bond formation is more or less the same, as depicted in figure 4.2 that gives a mechanical model for the process [8].

Figure 4.2: Model for a generic thermo-compression bonding process: (a) initial contact, (b) interface bond formation and misfit accommodation, (c) bond extension and pore elimination (d) bonding completion [8].

For diffusion-dominant solid-state bonding, elevated temperature during the bonding process is highly crucial for good bonding quality. The reason is that the motion of an exotic atom diffusing into a material is controlled by an Arrhenius model where the diffusion rate is exponentially dependent on temperature. Usually a temperature of at least 0.6 $T_M$ up to 0.9 $T_M$, where $T_M$ is the material melting temperature, is required if diffusion is the main mechanism during bonding. [39].

The microscopic explanation for successful bonding is the formation of chemical bond, namely elec-
tron sharing. Atoms can travel wherever they want by diffusion, but they can not become an entity if there is no chemical bond formed. A general solid-state atomic bonding principle is presented as follows: "As A atoms and B atoms are brought within atomic distance so that they can see each other, they will bond provided that they are willing to share the outer electrons. Diffusion of A and B atoms alone does not guarantee bonding if A and B atoms do not want to share electrons. 'A' and 'B' atoms may share electrons to form $A_xB_y$ compound. The $A_xB_y$ compound may or may not bond with A or B atoms, depending on whether they are willing to share electrons." [9]

A bonding model based on quantum mechanics is brought forth in [9] to determine the minimum distance required between A atom and B atom for bonding. Based on fitting experimental data to Morse potential (see figure 4.3), a convenient inter-atomic potential energy of a diatomic molecule, the model mimics the case where an A atom on the surface of A material get close to a B atom on the surface of B material (see figure 4.4). By fitting experimental data to the model important properties of the bonding materials can be analyzed and obtained, including the breaking strength vs. atomic separation and the Young's modulus.

![Morse Potential](image)

**Figure 4.3: Morse Potential.** $r$ is the distance between the atoms, $r_e$ is the equilibrium bond distance, $D_e$ is the dissociation energy, and $\alpha$ is a parameter that relates to the force constant. The dissociation energy $D_e$ is larger than the true energy required for dissociation $D_0$ due to the zero point energy of the lowest ($v=0$) vibrational level.

In practical practice, there are several other factors that need to be taken into consideration for stronger bonding strength.

1. Surface topography variations should be controlled to the least amount possible, otherwise voids would be generated at locations of dents on the bonding surface. The fabrication technique of the film is first and foremost the factor to reduce surface roughness. Among typical metal/metal nitride deposition techniques, sputtering is already a good choice for fabrication of flat films, as opposed to electroplating that usually results in layers with higher amounts of impurities and increased surface variations. Chemical mechanical polishing (CMP) can be employed as one step further on the road to
minimum surface variations. A mature CMP process can bring the surface roughness value below 1 nm root mean square (RMS) [40]. But CMP requires specialized tools and extra treatment on the particles generated during grinding.

(2) Surface cleaning is another crucial factor for better yield of thermo-compression bonding. To ensure atomic contact during bonding, impurities and oxidation on the metal surface must be removed ahead of bonding. In general, organic impurities can be removed by concentrated nitric acid \( (HNO_3) \) or UV-Ozone exposure and metallic impurities can be removed by diluted \( HNO_3 \). To remove oxidation layer as well as to prevent re-oxidation, it requires material-dependent consideration and does not have a generic solution. For example, hydrochloric acid \( (HCl) \) is commonly used to remove copper oxides before bonding [41]. Formic acid \( (CH_2O_2) \) vapor cleaning used during the bonding process to suppress cuprous oxide \( (Cu_2O) \) and therefore prevent re-oxidation of the copper surface.

(3) During the bonding process, strong pressure is applied to bring the two wafers close into contact. The pressure needs to be strong enough to not only cause plastic deformation of tiny variations on the metal surface, but as well to reduce the warp and bow in the wafer (see figure 4.5). Less surface roughness and warp/bow values could lower the pressure applied during bonding, which reduces the risk of damaging the structures on the wafer surface.

Industrialized application of thermo-compression bonding of metals include Al-Al (400°C-450°C), Au-Au (260°C-450°C), Cu-Cu (380°C-450°C) at bonding pressure of 30-120 MPa [42]. Those are well established in the CMOS industry to realize vertical integrated devices and production of wafer level packages with smaller form factors [43]. This bonding procedure is used to produce pressure sensors, accelerometers, gyroscopes and RF MEMS [42]. Companies such as IBM and Intel have adopted this technique to reduce interconnect length in 3D ICs for processor on processor and memory-onprocessor chips using Cu bonding together with Through-Silicon Via (TSV) technology. Currently, the most popular method in industry is thermo-compression at temperatures in the range on 300°C-400°C due to its simplicity and lower costs [43].
4.0.2. Sheet Resistance Measurement

The most commonly adopted method for measuring the sheet resistance of a material is the Van der Pauw approach. Van der Pauw developed a theory [44] based on conformal mapping that enables the measurement of the resistivity of a continuous surface of arbitrary shape, as long as the following conditions are met [45]:

1. The sample must have a flat shape of uniform thickness.
2. The sample must not have any isolated holes.
3. The sample must be homogeneous and isotropic.
4. The approach requires 4 sets of probes to make contacts with the sample, with 2 of them conducting current and the other 2 measuring the voltage difference. All four contacts must be located at the edges of the sample.
5. The area of contact of any individual contact should be at least an order of magnitude smaller than the area of the entire sample.

Another big advantage of the approach is that it could almost counteract entirely the errors caused by resistance of the probes of measuring equipment.

![Figure 4.6: Schematic of 4-point probe Van der Pauw resistance measuring scheme for a sample of arbitrary shape](image)

Resistance measurement of a sample of arbitrary shape (See figure 4.6) using Van der Pauw approach in dual configuration renders equation (4.1), where $R_{sh}$ stands for sheet resistance, $R_{1243}$ is the resistance value measured by inducing current through port 1 and port 2 and deriving the voltage difference between port 3 and port 4, likewise for $R_{2341}$, and F is the solution for equation (4.2). In equation (4.2), $R_v$ is given by equation (4.3). For samples with symmetric shape (See figure 4.7), there is no difference between $R_{1243}$ and $R_{2341}$, so the resistance ratio $R_v$ is equal to 1 and equation (4.1) is simplified into equation (4.4).

$$R_{sh} = \frac{\pi}{\ln(2)} \cdot \frac{R_{1243} + R_{2341}}{2} \cdot F$$  \hspace{1cm} (4.1)

$$\frac{R_v - 1}{R_v + 1} = \frac{F}{\ln(2)} \cdot \text{arccosh} \left( \frac{1}{2} \cdot e^{\frac{\ln(2)}{F}} \right)$$  \hspace{1cm} (4.2)

$$R_v = \frac{R_{1243}}{R_{2341}}$$  \hspace{1cm} (4.3)

$$R_{sh} = \frac{\pi}{\ln(2)} \cdot R_{1243}$$  \hspace{1cm} (4.4)

The Greek cross structure shown in figure 4.7 is mostly used for the extraction of sheet resistance. Furthermore it is an easy structure to layout and define photolithographically. The measured sheet resistance is at the heart of the cross and an accuracy of better than 0.1 percent can be achieved in practice.
4. Theory of Thermo-Compression Bonding and Resistance Characterization

4.0.3. Contact Resistance Measurement

The Cross Bridge Kelvin Resistor (CBKR) is the typical pattern for determining the electrical quality of direct bonding of a material or between two materials.

Figure 4.8: The four-terminal Cross Bridge Kelvin Resistor (CBKR) for measuring contact resistance. The contact area is marked in yellow.

CBKR also adopts the Van der Pauw scheme which employs 4 taps to measure resistance (see figure 4.8). Notice that in this case the induced current goes through two opposite taps rather than two neighboring taps as in sheet resistance measurement. The other two opposite taps are for voltage measurement. Therefore the effective common part of the structure the voltage tap pair and the current tap pair share for measurement is the contact interface marked in yellow. Calculation of contact resistance $R_C$ of the structure is given in Equation (4.5).

$$R_C = \frac{V_2 - V_1}{I}$$  \hspace{1cm} (4.5)

Figure 4.9: Contact resistivity is defined as taking a short length across the contact interface to limit of bulk resistivity.

With different methods of making contacts, a standard quantity is desired as point of comparison. Contact resistance depends on the size of the contact, which makes it not a good standard for
comparison. Instead, contact resistivity can be used to set a standard. Considering a small region in
the vicinity of the contact (see figure 4.9), Equations (4.6) and (4.7) show how to calculate contact
resistivity $\rho_c$ from contact resistance $R_c$, where $A_c$ is the area of contact. So contact resistivity would
have unit of $\Omega \times m^2$.

$$R_c = \rho_c \frac{\Delta x}{A_c} \quad (4.6)$$

$$\rho_c = \lim_{\Delta x \to 0} (\rho_c \Delta x) = R_c \times A_c \quad (4.7)$$

4.0.4. Daisy Chain Resistor Pattern

Figure 4.10: A representative schematic of a daisy chain resistor pattern for
measuring DC contact resistance [10]

Figure 4.11: A Comsol simulation of current distribution around a normal corner. The
structure is consisted of two 4mm x 2mm x 1mm rectangular block. The test current
is injected uniformly from a side surface of one of the blocks

Although daisy chain resistance test is commonly used in IC packaging industry as life cycle testing,
drop testing, verifying the effects of CTE (Coefficient of Thermal Expansion), selecting the correct
amount of solder paste, evaluation of solder paste stencils, checking for voids caused during reflow, and
underfill experiments, etc [46]. In this thesis it is conveniently adopted to test the contact resistance
of the bonding interface. In a daisy chain structure, test current flows through many contact spots
and as many stripes. The sum total resistance a daisy chain depends on the length of the circuitry, the
bulk resistivity of constructing materials, and the contact resistivity at the bonding interface.
that in a common daisy chain structure (see figure 4.10), the current flow needs to take a 90 degree sharp turn before it sees a bonding interface. A Comsol simulation of how dc current is distributed when it flows through a structure with normal angle (see figure 4.11). According to simulation, there is current crowding effect at two sharp corners on the bonding interface, indicating that the contact resistivity value rendered by daisy chain approach may be different from the case where the incident current is uniform. Also the resistance of the structure can be extracted from simulation to compare with measurement data. But I am a bit lazy to write it down considering that I really need to hand in the thesis soon.
Experiment Setup and Result Discussion of Thermo-Compression Wafer Bonding of NbN films

5.1. Experimental Setup

5.1.1. AML Wafer Bonder

This system is a versatile tool capable of bonding wafers and pieces in a variety of techniques, including anodic, eutectic, direct (high and low Temperature) glass frit, adhesive, solder, iCAB, thermo-compression, and temporary wafer bonding.

For thermo-compression bonding in particular, AML bonder can produce a maximum of $550^\circ$ heating and 15kN pressure. Figure 5.1(b) gives an illustration of the working principle of the wafer bonder. There is only a heater that acts on the bottom platen. Once the both wafers get into contact during bonding, temperature of the upper platen will also rise as heat is delivered through the both wafers. So upper platen is always slower than bottom platen in temperature ramping. On the bottom of the chamber, there is a motor that controls the position of the bottom platen, with horizontal adjustment for alignment and vertical adjustment for force application. In order to align the patterns on the upper and bottom wafers, two holes are drilled through the top platen for microscope inspection. Infrared
light is employed to enable a penetrating view of the patterns that are on the opposite side of the upper wafer (See Figure 5.3 and Figure 5.4). To enhance the view quality, both wafers should be double-side polished.

![Figure 5.2: Picture of top and bottom wafers loaded on platens](image)

Figure 5.2: Picture of top and bottom wafers loaded on platens

![Figure 5.3: Four basic alignment methods used in wafer level bonding. The alignment method in AML wafer bonder adopts the IR inspection.][11]

Figure 5.3: Four basic alignment methods used in wafer level bonding. The alignment method in AML wafer bonder adopts the IR inspection.[11]

![Figure 5.4: Schematic illustration of infrared light alignment. Also shown is an example of the sub-micron IR alignment marks designed for automated alignment software.][11]

Figure 5.4: Schematic illustration of infrared light alignment. Also shown is an example of the sub-micron IR alignment marks designed for automated alignment software.[11]

As for loading the wafers, the top wafer is fixated on the top wafer by a mechanical clamp, the bottom wafer is just placed on the bottom platen (See Figure 5.2). Before the bonding process starts, the whole chamber needs to be vacuumed first, otherwise oxygen would easily reacts with metal on the wafer as high temperature is often employed during bonding. Also since the bottom wafer is placed without fixation, vacuum environment ensures that the bottom wafer will not move around or slip off the bottom platen when the bottom platen is moving. Once the chamber is vacuumed down to $10^{-4}$ mbar, the bottom platen can then be pushed up by the motor below to come into contact with the top platen, to a degree that is set by the applied force desired.
5.2. Results and Discussion

5.2.1. 4-Point-Probe Room-Temperature Sheet Resistance of NbN

Figure 5.5: Van Der Pauw Structure for characterization of the sheet resistance of 180nm-thick NbN film. Trails of underdeveloped photoresist are still attached to the pattern surface, but it does not influence the measurement.

Figure 5.5 shows the 4-point-probe structure, also known as the Van der Pauw structure, for characterization of sheet resistance of a NbN film. Probing scheme is shown in Figure 5.5(a) and the same scheme also applies to 5.5(b).

Figure 5.6: Fabrication of Van der Pauw Structure for Measuring Sheet Resistance of NbN

Illustration of the patterning process is shown in Figure 5.6 in sequence from 5.6(a) to 5.14(f). The
Experiment Setup and Result Discussion of Thermo-Compression Wafer Bonding of NbN films

substrate is chosen to be double-side polished Si wafer with 400μm thickness. NbN film is deposited on the bare Si wafer for 100s with 75 sccm \( N_2 \) flow rate and 3KW discharge power. The film thickness is measured to be 180nm. Next, the NbN film is coated with 2μm-thick positive photoresist. The photoresist is then patterned to give the Van Der Pauw structure. The patterning is a two-step process that includes exposure in AMSL PAS 5500/80 automatic wafer stepper and development in. After patterning, the wafer is dry-etched in Trikon Omega 201 to transfer the pattern from the photoresist layer down to the NbN layer. Once the etching is done, the photoresist is removed by dipping the wafer in acetone for 10mins.

Measured room-temperature NbN resistance of the patterned Van der Pauw structure is shown in Figure 5.7, given the 4-point measurement scheme depicted in figure 5.5. Since both square sizes (50μm x 50μm and 100μm x 100μm) share the same length/width ratio, one should expect to get approximately the same resistance from both structures. It turns out that all the 100μm x 100μm patterns on the wafer are a bit less resistive than the 50μm x 50μm patterns. The reason is a bit subtle, but from a rough estimation [47], one can tell the measured resistance should decrease with the center square size. The measured resistance \( R_{meas} \) is taken to be the average of the two, which gives 2.83Ω.

Calculation of sheet resistivity from measurement outcomes of Van der Pauw structure is given in Equation (5.1) and Equation (5.2). Sheet resistance is denoted as \( R_{sheet} \), sheet resistivity is denoted as \( \rho_{sheet} \). The NbN film thickness is denoted as \( t \). Calculation renders 12.83Ω of sheet resistance and 230.9μΩ * cm of sheet resistivity.

\[
R_{sheet} = \pi / \ln(2) \times R_{meas} = \pi / \ln(2) \times 2.83\Omega = 12.83\Omega \quad (5.1)
\]

\[
\rho_{sheet} = R_{sheet} \times t = 12.83\Omega \times 180nm = 230.9\mu\Omega \times cm \quad (5.2)
\]
5.2.2. Thermo-Compression Bonding of NbN Film to NbN Film

Direct bonding of NbN film to NbN film was demonstrated. Two Si substrates sputtered with 180nm-thick NbN films are first placed inside AML wafer bonder for thermo-compression bonding, with 500°C heating on both platens and applied force of 2kN. Duration of this step is 40 hours. Next, the bonded wafer pair is put into furnace for annealing. The annealing temperature is 1100°C and the duration is 3 hours.

Due to lack of specialized tool for quantitative characterization, the bonding strength could only be roughly divided into 3 levels. Table 5.1 gives an qualitative characterization of the bonding strength. Annealing at high temperature could greatly enhance the bonding strength. A plausible assumption would be that since the annealing temperature reaches almost half of the melting point of NbN, which is reported to be around 2500°C. The breaking of Niobium-Nitrogen chemical bond happens at high frequency and diffusion of Nb and N atoms across the interface dominates the bonding process, as described in 4.0.1.

Figure 5.8 shows a diced sample of NbN-to-NbN thermo-compression bonding. The sample not only survives the wafer dicing saw, but could as well withstand the shear force human hands could apply. Figure 5.9 shows what ill-bonded interface looks like. Those round shapes are small-sized voids that deteriorate the bonding quality.

Figure 5.8: Sample of successful NbN-to-NbN thermo-compression bonding after annealing

Figure 5.9: Sample of failed NbN-to-NbN thermo-compression bonding after annealing. This failure only happens at the rim of the bonded wafers.
5. Experiment Setup and Result Discussion of Thermo-Compression Wafer Bonding of NbN films

<table>
<thead>
<tr>
<th>NbN-to-NbN Direct Bonding</th>
<th>Survive transportation and tweezer handling?</th>
<th>Survive wafer dicing saw?</th>
</tr>
</thead>
<tbody>
<tr>
<td>After thermo-compression bonding</td>
<td>Sometimes</td>
<td>No</td>
</tr>
<tr>
<td>After annealing</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>

Table 5.1: Qualitative characterization of NbN-to-NbN thermo-compression bonding strength

5.2.3. Wafer-scale Daisy-Chain Resistor

Figure 5.10 shows the two wafers with respective daisy chain patterns joint together by thermo-compression wafer bonding. Both wafers are 400-μm thick and double side polished, which is required for infrared light inspection for bonding quality shown in Figure 5.10(d). The daisy chain patterns on both wafers are fabricated out of 500nm thick Al films sputtered in Trikon Sigma 204 under 350°C. In 5.10(d), the 6mm x 2mm rectangular patterns from the top wafer aligns rather perfectly with those on the bottom wafers. The presence of Newton rings only on the rim of the bonded wafers indicate that both wafers are bent at the rim during compression due to lack of support patterns. Each of the 6mm x 2mm rectangular patterns is consisted of three 2mm x 2mm squares in a row and a 2mm x 2mm square pattern is embedded in the exposure equipment because it is frequently used for exposing alignment markers on a wafer during photolithographic steps. The purpose of this wafer-scale daisy chain pattern is to easily and quickly extract macroscopic contact resistance at room temperature, saving the effort to design finer structure and fabricate customized masks. The disadvantage of this large-scale pattern is that it cannot fit into any cryogenic refrigerator, which then makes it impossible to measure the superconducting properties of the bonding interface.

The parameters for thermo-compression bonding of the two wafers are listed in Table 5.2. The platen temperature is roughly the same as the wafer temperature during bonding. The whole bonding process lasts for 7 hours in total. The two wafers are pressed into contact for over 4 hours with 4.5MPa pressure and 500°C heating to ensure a rather adequate degree of diffusion.

The purpose of the design of wafer-scale daisy chain pattern is measure the contact resistance in direct bonding on a macroscopic view. Room-Temperature resistance measurement of the Al-Al wafer-scale daisy chain pattern is also carried out in 4-point Kevin fashion, as shown in Figure 5.10(c). Other pins that stick out on the bottom wafer are initially designed to locate the area on the bonded wafer with bad bonding quality in terms of electrical connection. Result of the dc resistance measurement is shown in Figure 5.11(a). The curve is a standard straight line that goes though the origin, which indicates no parasitic resistance in the system. Therefore two points on both tips of the curve are picked to calculate the resistance. The collective 202 contact spots on the bonded wafers give a total resistance of 8.4 Ω, indicating that the contact resistivity of a single contact spot is on average not greater than 1.66×10^{-3} Ω·cm². Likewise, for NbN-to-NbN daisy chain resistor, the collective 80 contact spots on a branch of entire chain give a total resistance of 4.14 Ω, indicating that the contact resistivity of a single contact spot is on average not greater than 2.36×10^{-3} Ω·cm².

<table>
<thead>
<tr>
<th>Timeline</th>
<th>Pressure</th>
<th>Upper Platten Temperature</th>
<th>Bottom Platten Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>0h00min</td>
<td>0 MPa</td>
<td>95°C</td>
<td>46°C</td>
</tr>
<tr>
<td>0h25min</td>
<td>4.5 MPa</td>
<td>491°C</td>
<td>500°C</td>
</tr>
<tr>
<td>4h46min</td>
<td>4.5 MPa</td>
<td>491°C</td>
<td>500°C</td>
</tr>
<tr>
<td>7h00min</td>
<td>0 MPa</td>
<td>200°C</td>
<td>205°C</td>
</tr>
</tbody>
</table>

Table 5.2: Parameters for the thermo-compression bonding of Al-Al wafer-scale daisy chain pattern
5.2. Results and Discussion

(a) Trimmed top wafer
(b) Bottom wafer
(c) Bonded wafers
(d) Infrared light inspection of bonded wafers

Figure 5.10: Al-Al wafer-scale daisy chain pattern

(a) Resistance of Al-Al wafer-scale daisy chain pattern over 202 contact spots.
(b) Resistance of NbN-NbN wafer-scale daisy chain pattern over 80 contact spots

Figure 5.11: Measurement results of daisy chain resistors
5.3. Miniaturized pattern for contact resistance measurement in cryogenic environment

![Diagram showing steps of fabrication process](image)

**Figure 5.12: Fabrication of contact resistance pattern on the bottom wafer**

Illustration of the process for patterning the bottom wafer is shown in Figure 5.12 in sequence from 5.12(a) to 5.12(h). The substrate is again chosen to be double-side polished Si wafer with 400μm thickness and 1000Ω·cm resistivity. 180nm-thick NbN film is deposited on the bare Si wafer for 100s with 75 sccm \(N_2\) flow rate and 3KW discharge power. 40nm thick SiO\(_2\) is deposited by PECVD on top of NbN to perform as a hard mask, mainly to separate NbN from photoresist and other sources of potential residue. Then 2μm thick of positive photoresist is coated for patterning of alignment marker that will later be used during bonding. The alignment marker is etched about 2μm deep into the silicon wafer by \(SF_6/O_2\) mixed plasma that has a etching rate ratio of about 25:1 for Si versus positive photoresist (neglecting the 180nm-thick NbN and 40nm-thick SiO\(_2\) because they are etched away fast). Therefore during bonding, the difference between 400μm and 398μm of Si wafer thickness would make a vision contrast as infrared light shoots from the backside of the wafer. Besides, the size of the alignment marker for wafer bonding is the basically the maximum accuracy that can be achieved during bond-
ing. It is a totally equipment-dependent parameter and in this case the accuracy is $10 \mu m$. After the alignment marker is etched, bonding patterns on the bottom wafer is exposed and developed and then etched by $HBr/Cl_2$ mixed plasma. With all the patterning ready, the “soft” photoresist mask layer is removed by $O_2$ plasma and the “hard” $SiO_2$ mask layer is removed by immersing buffered HF solution. Figure 5.12(i) gives a bird view of the surface of the bottom wafer after patterning. Alignment marker is not shown.

![Figure 5.12: Illustration of the process for patterning the top wafer](image)

(a) In the first step silicon is etched by $SF_6$. The brown layer is the mask, which could be photoresist or $SiO_2$.

(b) In the second step the side wall is passivated by fluorine carbon polymer $C_4F_8$.

(c) In the third step $SF_6$ is employed again to etch deeper into the silicon wafer. There will be $C_4F_8$ residue left on the side wall.

(d) $C_4F_8$ is again used to passivate deeper side wall.

**Figure 5.13: Illustration of a cycle in Bosch DRIE process**

Illustration of the process for patterning the top wafer is shown in Figure 5.13 in sequence from 5.14(a) to 5.13(p). The substrate is again chosen to be double-side polished Si wafer with 400$\mu m$ thickness and 1000$\mu cm$ resistivity. From figure 5.14(a) to figure 5.14(g), it is all the same patterning procedure as those done on the bottom wafer. After alignment marker and structure for bonding are successfully patterned on the top wafer, an 8$\mu m$-thick layer of $TEOS$ is deposited to perform as hard mask for through silicon etching. Then photoresist is coated and patterned to create the opening for etching. The 8$\mu m$ of $TEOS$ and 180nm of NbN are etched away by buffered HF solution and $HBr/Cl_2$ plasma respectively, the result of which is depicted in figure 5.14(l). In 5.13(o), the silicon wafer is etched all the way through to provide a window for probing in electrical measurement. The through silicon etching is achieved by Bosch process. Bosch process is a deep reactive-ion etching (DRIE) process that provides highly anisotropic and high-aspect-ratio etching to create deep penetration, steep-sided holes and trenches in wafers/substrates. The process consists of the cyclic isotropic etching and fluorocarbon-based protection film deposition by quick gas switching. The $SF_6$ plasma cycle etches silicon, and the $C_4F_8$ plasma cycle creates a protection/passivation layer (see figure 5.13). A stopping layer is often needed at the back side of the wafer to prevent damage on the chuck of the machine from $SF_6$ etchant when the silicon wafer is etched through in the final cycle. This is achieved by gluing another Si wafer to the back side of the targeted one before etching. It usually takes hours to etch through a 400$\mu m$ thick silicon wafer; heat can accumulated since etching consists to a large extent of physical bombardment. Solution to the problem is clamping the wafer on its rim and blowing He onto the back side during etching, instead of placing the wafer on a chuck. Figure 5.12(l) gives a bird view of the surface of the bottom wafer after patterning. Alignment marker is not shown.

Contact resistance measurement in cryogenic environment is yet to be carried out next week in July. The preparation for the measurement is almost done (see figures 5.13, 5.14, 5.15). If the bonding interface could show superconducting electrical conduction, this would be a step towards compacter integration of quantum chips without the need of extra layer of indium for adhesion.
Experiment Setup and Result Discussion of Thermo-Compression Wafer Bonding of NbN films

(a) Bare Silicon Wafer
(b) NbN, SiO₂ and positive photoresist are layered on Si wafer
(c) Alignment markers for AML wafer bonder is patterned on the photoresist layer
(d) Etching of AML alignment marker 2μm deep into the Si
(e) Top part of the contact resistance structure is patterned on the photoresist layer
(f) Top part of the contact resistance structure is transferred down to the NbN layer after dry etching
(g) The photoresist layer is removed by high-power O₃ plasma etching
(h) 8μm thick PECVD TEOS is deposited on the wafer to perform as hard mask for through silicon etching. The contact resistance pattern is enveloped by the TEOS layer
(i) A new layer of positive photoresist is coated on the top wafer
(j) Window for through silicon etching is patterned on the new layer of photoresist
(k) The window pattern is transferred down to the NbN layer after dry etching, and silicon surface is exposed
(l) The new layer of positive photoresist is removed by high-power O₃ plasma etching
5.3. Miniaturized pattern for contact resistance measurement in cryogenic environment

(o) Bosch DRIE process is employed to etch through the silicon substrate. Another bare silicon wafer is glued to the backside of the top wafer as stopping layer, which is not shown in the graph.

(p) The TEOS layer is removed by dipping in buffered HF solution.

(q) A bird’s view of the contact resistance pattern on the top wafer. Contact area to be bonded is marked in yellow. Alignment marker is not shown.

Figure 5.13: Fabrication of contact resistance pattern on the top wafer

Figure 5.14: Complete schematical view of the total structure for measuring contact resistance
Figure 5.15: Illustration of real mask design for the structure shown in 5.14. The pattern on bottom wafer is shown in purple, top in green. The trapezoid window on the top wafer is shown in black dotted line.
6

General Conclusions and Outlook

6.1. Conclusion and Summary

The direct bonding of superconducting material is important for integration of 3-D superconducting chips, quantum processors in particular. The research into this topic is so far not abundant. In this thesis, fabrication and measurement as well as direct bonding of superconducting NbN film have been demonstrated. The fabrication of NbN is achieved by DC magnetronsputtering, with highest measured $T_c$ as 15.6K. The approach to fabricating high-$T_c$ NbN film is optimized by controlling the nitrogen flow rate to argon flow rate ratio during sputtering. Besides, direct bonding of NbN films is demonstrated by thermo-compression bonding at 500°C and 2kN applied force for 40 hours, and later annealed at 1100°C for 3 hours. More details of major achievements are summarized below within this chapter:

- **Optimization of $T_c$ of NbN films** is achieved in Chapter 3 by correlating with the curves of discharge voltage v.s. $N_2$ flow rate and the chamber pressure v.s. $N_2$ flow rate during magnetron sputtering deposition in Trikon Sigma 204. The highest $T_c$ measured is 15.2K, which is 2K lower than highest record (17.3K) reported in literature that was also done by magnetron sputtering.

- **Wafer-Scale Daisy Chain pattern** is designed and fabricated in an attempt to fast derive room-temperature contact resistance from thermo-compression bonding. Both Al and NbN daisy-chain resistors are fabricated and the contact resistance are extracted in Chapter 5.

- **NbN-to-NbN thermo-compression bonding** is achieved in Chapter 5, which shows good bonding strength as it could survive the force from handling and transportation and wafer dicing saw, as well as from the shear force a human hand could generate.

6.2. Recommendations for Future Work

- **Low Temperature Thermo-Compression Bonding of NbN films**
The current approach for direct bonding of NbN films include 1100°C annealing for stronger bonding strength. Since wafer bonding is among the last steps in many applications, there is usually not sufficient thermal budget for an 1100°C operation. For example, this would cause redistribution of doping profile in silicon chips or Nitrogen loss in NV-Center. A low-temperature process for equal bonding strength needs to be developed before this bonding technique can be put into practical use. Potential solution includes more careful surface treatment of NbN film ahead of bonding so that the bonding can be surface-diffusion dominant instead of bulk-diffusion dominant.

- **Quantitative Characterization of Wafer Bonding Strength**
Shear force test is an usually adopted method to measure the strength of die-to-die or die-to-wafer bonding (see figure 6.1). The test will give a quantitative reading of the maximum shear force required to split the bonding interface between the top die and the bottom die.

- **Towards 3-D integration of Superconducting Chips with Qubit involved**
To achieve 3-D integration of superconducting chips, directing bonding is not enough. There
are Superconducting TSV and Ball-Grid Array for superconducting connection between chip and PCB, integrated in one structure as shown in figure 6.3. There are already works done by others concerning these topics mentioned above (see figure 6.2). An interesting step forward would be integrating these sub-structures with qubits.

Figure 6.1: Schematic of a setup for die shear force test

Figure 6.2: Examples of prior works done on integration of superconducting chips

Figure 6.3: Conceptual Schematic of a two(multi)-layer superconducting structure for 3-D qubit integration
Bibliography


[2] *Ibm q:the future is quantum,*.


