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Pure Dopant Deposition of B and Ga for Ultrashallow Junctions in Si-based Devices

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Envisioning wide future relevance, work is reviewed here on the pure dopant deposition of boron (PureB), gallium (PureGa) and the combination of the two (PureGaB), as used in the fabrication of nanometer shallow p^+n Si and/or Ge diodes. Focus is placed on the special properties that have put these diodes in a class apart: their ideal electrical behavior together with their electrical, optical and chemical robustness have lead to cutting-edge application as photodiodes for detecting low-penetration-depth beams, as for example in EUV lithography and low-energy electron SEM imaging. Of key importance is the effectively high Gummel number of the p^+-region that provides low saturation currents despite the shallowness of the junctions. Based on experimental evidence it is proposed here that this is related to the formation of a practically complete surface coverage of acceptor states as an interface property of PureB on Si and PureGa on both Si and Ge.

Introduction

The last half decade has seen a rapid development and adaptation in production of PureB photodiode technology for application in extreme-ultraviolet (EUV) lithography and Scanning Electron Microscopy (SEM) systems using low-energy (down to 200 eV) electron detection [1]. In this technology, chemical-vapor deposition (CVD) of pure boron is used to create the p^+-region of shallow, less than 10-nm deep, silicon p^+n junction diodes. In the first applications, a nm-thin amorphous boron (PureB) layer is deposited selectively on silicon through openings in an oxide isolation layer at a temperature of 700ºC. This technology has several attractive properties: the junction formation is damage-free, the PureB layer is chemically robust in many situations, there is a high compatibility with Si IC-processing, and the diodes have saturation currents almost as low as that of conventional deep diodes. The fabricated detectors surpassed the performance of other existing technologies on points such as internal/external quantum efficiency, dark current, and degradation of responsivity. For example, for the detection of the above mentioned beams that only penetrate a few nm into the Si, 2-nm-thick PureB-layers have reliably been implemented as the front-entrance window [2, 3].

As a further development of the PureB work, the last couple of years have seen investigations on more low-temperature processes, down to 400ºC, also using pure gallium (PureGa) depositions. This was made possible by the availability of a standard Si/SiGe ASMI CVD reactor that was specially equipped for merging GaAs and Si epitaxial growth in the one system [4]. The main goal has been to develop new processes that would be compatible with CMOS, preferably in a fully-processed form. In this context, a high-quality p^+n Ge-on-Si diode was developed using a PureGa layer capped with PureB to form the p^+-region [5]. This pure-dopant layer-stack has been christened “PureGaB”.

In all these diodes, PureB/Ga Si diodes and PureGaB Ge-on-Si diodes, the excellent electrical characteristics can be ascribed to an effectively high Gummel number of the p^+-region. The injection of electrons from the n-region into the p^+-region is suppressed resulting in a low saturation current [6, 7]. This is not seen in other ultrashallow diodes produced by techniques that only aim at damage-free doping of the semiconductor, for example epitaxy of doped Si or Ge, or doping from a gas [8]. Therefore the terms PureB/PureGa/PureGaB have been introduced to underline that a solid layer of pure dopant material has been deposited. It has in the past been suggested that the bulk properties of the PureB layer should be responsible for the high Gummel number [6, 9] but the overall experimental evidence that now is available, and is discussed here, suggests that it is in fact a property of the interface between the pure dopant layer and the underlying semiconductor.

PureB Si Diodes

PureB Deposition Conditions

An extensive characterization of PureB Si diodes has been performed for a deposition temperature of 700ºC using diborane as precursor and H_2 as carrier gas. As it turns out, this now appears to be the ideal conditions for achieving extremely uniform, reproducible layers. For example, it has been possible to control pattern dependency and loading effects to such a degree that 2-nm-thick layers can be deposited uniformly with only a few angstrom variation in thickness over a 100 mm wafer and roughness of the order of one angstrom [3]. The diffusion lengths of the boron on both oxide and Si surfaces are found to be in the order of centimeters which means that the loading effect in micron sized windows will not lead to thicker layers than those deposited in the larger windows. In this respect PureB can also be attractive for use in small dimension devices such as CMOS transistors.

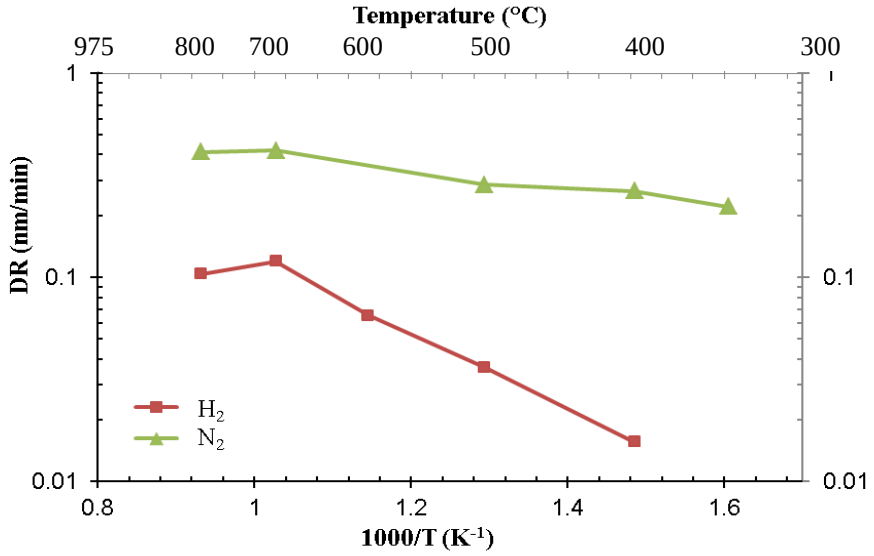


Figure 1. Deposition rate (DR) of PureB layers on B-covered Si as a function of temperature for a carrier gas of either H_2 or N_2 [10].

For lower deposition temperatures, down to 400ºC, investigations have shown that as the temperature decreases the deposition rate and also the mobility of B along the surface decreases. This entails an increase of the surface roughness up to several angstroms. As illustrated by Fig. 1, the deposition rate increases significantly by switching to N_2 as carrier gas but here the much lower concentration of H at the surface lowers the B mobility and also gives a less smooth surface [10].

Electrical Behavior

Electrical measurements that show the very low saturation current of PureB diodes are displayed in Figs. 2 and 3. From the bipolar measurements it can be concluded that the electron injection currents are as low as a few 10^{-20} A/μm^2 which is comparable to those achieved in deep heavily-doped junctions [6]. This corresponds to a Gummel number, G_E, of the order of 10^{14} - 10^{15} atm/cm^2, which is decades higher than what would be expected of nm-shallow junctions formed by bulk doping of the silicon [11]. In the 700ºC PureB diodes the actual doping of the Si-substrate is very limited by the low solid solubility and diffusivity of the B and gives a contribution to G_E of about 10^{12} atm/cm^2, as is documented in [6]. In diodes that are formed solely by such a doping of the Si-substrate, the total current would approach Schottky-diode-like values and abnormalities often appear in the I-V characteristics due to depletion of this the thin, lightly-doped p-region [12]. From the figures it is seen that the PureB current levels are decades lower than those of the corresponding Schottky diode and they decrease somewhat as the deposition time, i.e. PureB thickness, is increased. In earlier work, it was suggested that the increasing PureB layer thickness was directly responsible for this behavior. Bulk properties of the amorphous boron layer itself that could explain the suppression of the electron injection include (i) a very short electron diffusion length and low electron mobility that could cause quenching of the electron transport [6] or (ii) a wider bandgap than the Si as proposed and supported by simulations in [9]. However, even for a 1 s PureB deposition where not even a monolayer of boron is deposited, an equally high hole injection is observed both for 700ºC and 500ºC depositions and abnormalities in the I-V characteristics have not been found. Also, the PureGa results described and discussed in the next section do not support the idea that the bulk properties should be playing a decisive role. All in all, it seems much more plausible that high hole concentration is related to properties of the interface between the pure-dopant layer and the Si-substrate that induce the creation of acceptor states. For G_E in the 10^{14} - 10^{15} atm/cm^2 range this would fit well with the picture that most of the B/Ga atoms at the interface are activated since monolayer coverage corresponds to about 6.78×10^{15} atm/cm^2. The increasing G_E with increasing PureB could plausibly be related to several effects that increase the hole concentration: the progressive doping of the Si up to the solid solubility level (~ 2×10^{19} cm^{-3} at 700ºC but much lower at 500ºC) or the activation of more and more acceptor states at the interface. Both effects will set the depletion region edge further from the surface to also give a lower influence of the surface recombination of injected electrons. With respect to the activation of acceptors states at the interface, it could well be that the mechanical pressure exerted by PureB/Ga capping layer plays a role.

For photodiode applications it has also been demonstrated that the very high hole gradient right up to the surface, without roll-off, is very important for securing low leakage currents and high responsivity [13]. This gradient repels electrons from the surface where they would otherwise recombine. Even when the PureB layer is driven-in by thermal annealing at temperatures above 700ºC, a high gradient is maintained up to

the surface and, together with the damage-free nature of this doping technique, a high responsivity is maintained.

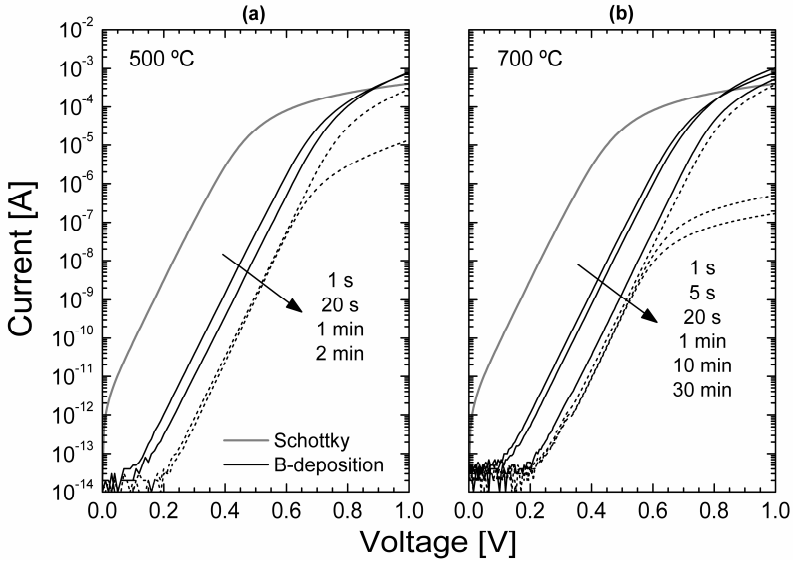
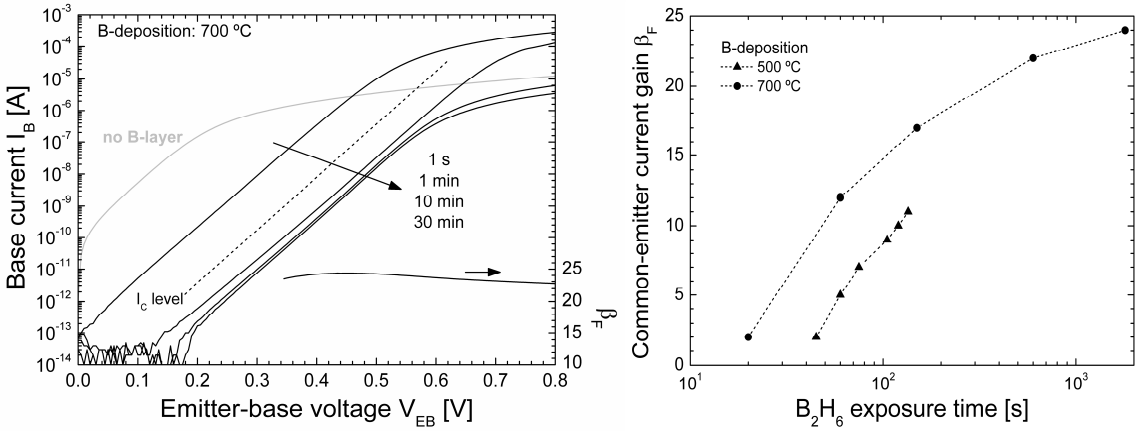


Figure 2. PureB diode I-V characteristics for various deposition times at either (a) 500 ºC or (b) 700 ºC. The anode area is 2 × 1 μm^2. For comparison, the I-V curve of a Schottky diode is also included [14].



(a) (b)

Figure 3. Electrical characteristics of pnp bipolar transistors with PureB p$^+$-emitters deposited at either 500 ºC or 700ºC for different deposition times. (a) Gummel plots showing the base current for each deposition time. The collector current level is also shown as a reference. The common-emitter current gain (right axis) is reported for a device formed with a 30 min deposition time. The emitter area is 40 × 40 μm^2. (b) The common-emitter current gain as a function of deposition time at V_{EB} = 0.45 V for an emitter area of 40 × 10 μm^2 [6].

Integration of PureB in photodiode detectors

The best example of the versatility with which the PureB diodes can be integrated in detectors is the low-energy electron detectors developed for SEM imaging. A schematic cross-section of such a detector is shown in Fig. 4. The front-entrance window is formed with the photosensitive depletion layer only being covered by a nm-thin p$^+$-anode under an equally thin PureB layer. This has resulted in a record-high electron-signal-gain for

electron energies below 1 keV down to 200 eV. Moreover, the PureB does not oxidize and is chemically resilient in many ways [2].

Going to lower deposition temperatures than the 700ºC used in the applications up until now, is particularly interesting for increasing the integration flexibility. Below about 450ºC it even becomes feasible to add the PureB to a fully-processed CMOS wafer. Although equally good diode I-V characteristics have been obtained at temperatures down to 400 ºC there are more issues to be dealt with than for the 700ºC deposition such as higher surface roughness, more pronounced loading effects, higher sheet resistance and probably also higher series resistance because effectively thicker layers must be used. Moreover, the optical responsivity and robustness as well as electrical degradation still need to be characterized.

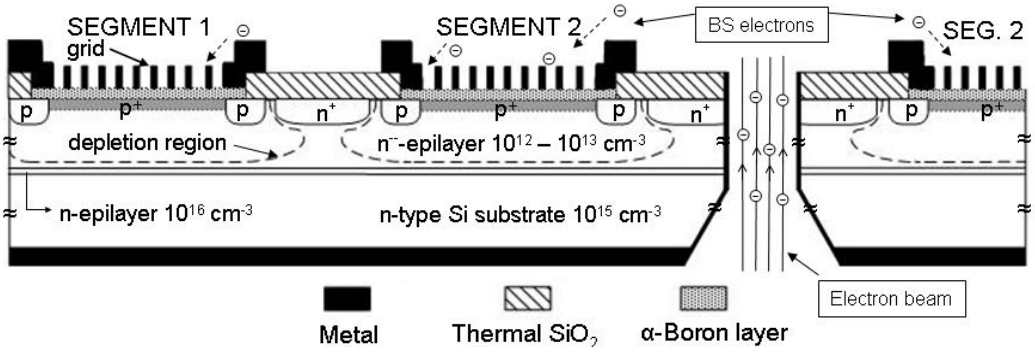


Figure 4. Schematic cross-section of two neighboring photodiode segments of a PureB back-scatter detector designed for use in SEM imaging with high scanning speed. A through-wafer hole has been etched to form an aperture for the electron beam. Low capacitance is achieved by depletion of a 40 µm deep n^{--} epitaxial layer. To lower the series resistance a fine grid has been etched in aluminum metallization placed directly on the PureB layer covering the p^+ anode regions. This gives less than 2% loss of responsivity [15].

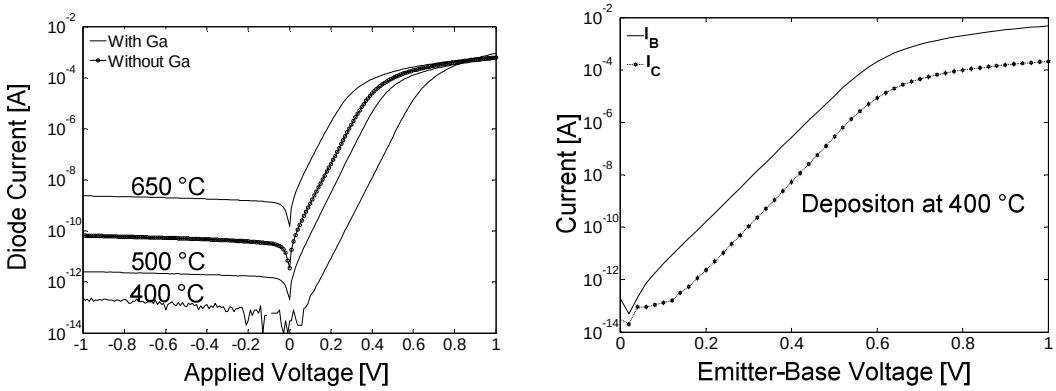


Figure 5. (a) I-V characteristics of PureGa Si diodes formed with and without first depositing Ga at a temperature of 400ºC, 500ºC or 650ºC. (b) Gummel plots measured on lateral pnp transistors with PureGa emitters deposited at 400ºC. The hole injection (~ I_C) from the p^+ PureGa-emitter region is separated from the electron current (~ I_B) by collecting the hole current at the collector terminal. A high I_C is observed only for the case of Ga-deposition at 400ºC, corresponding to a high hole injection from the emitter [7].

PureGa Si Diodes

For Ga, the reaction temperature with Si is much lower than for B and only a small process window at 400ºC was found to give a selective thin-layer deposition in windows to the Si and diodes with properties comparable to those of PureB diodes were fabricated. An example of the low diode saturation current is given in Fig. 5a while the strong hole injection from a PureGa emitter can be seen in Fig. 5b. Since Ga is a metal with material properties very different from B, it seems unlikely that the bulk properties of these pure dopant layers are responsible for the effectively high Gummel number of the p^+-regions formed by their deposition.

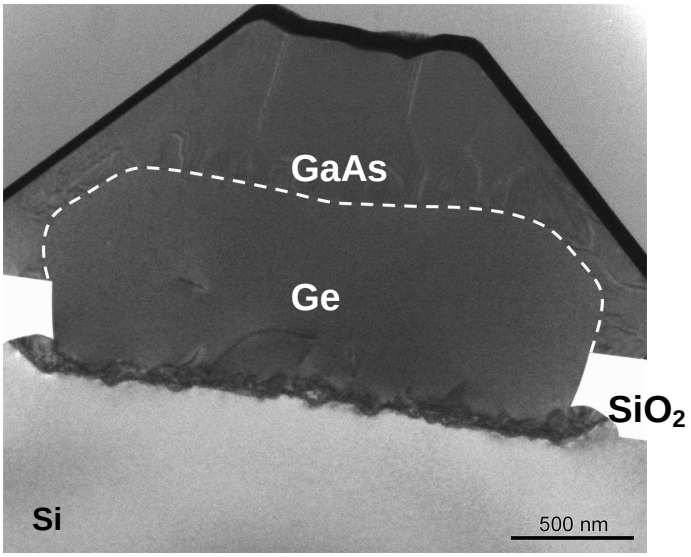


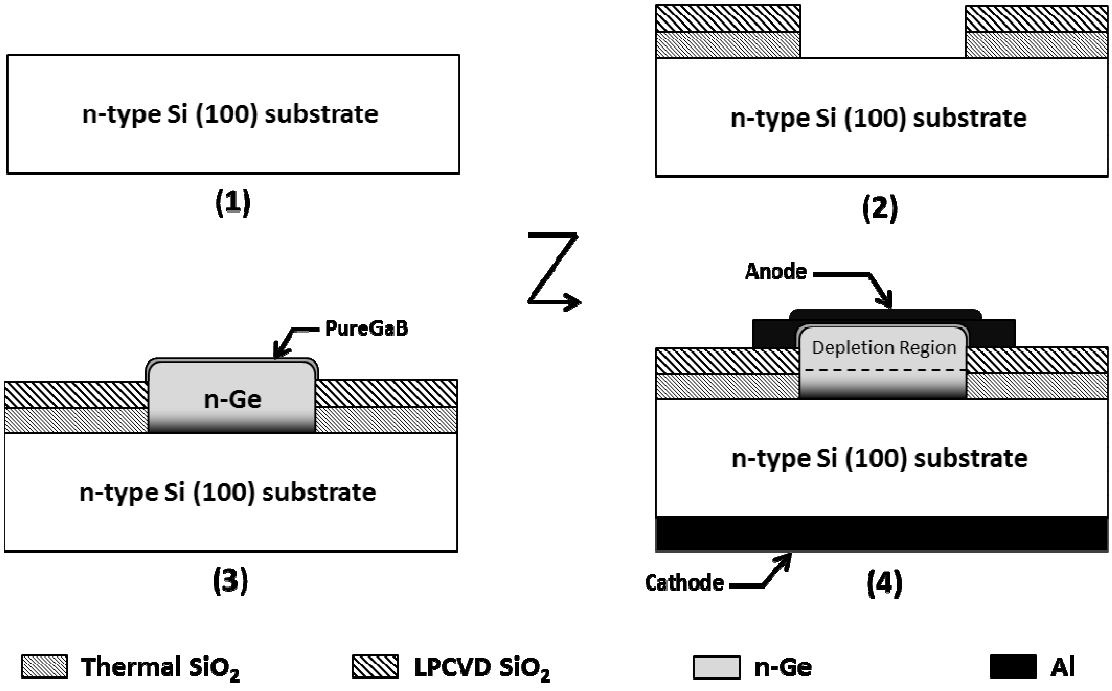
Figure 6. Cross-sectional TEM images of selective Ge epitaxy grown on pattened Si followed by in-situ growth of a GaAs layer at a temperature of 700˚C in line-shaped window sizes with a width of 2 µm [16].

PureGaB Ge-on-Si Diodes

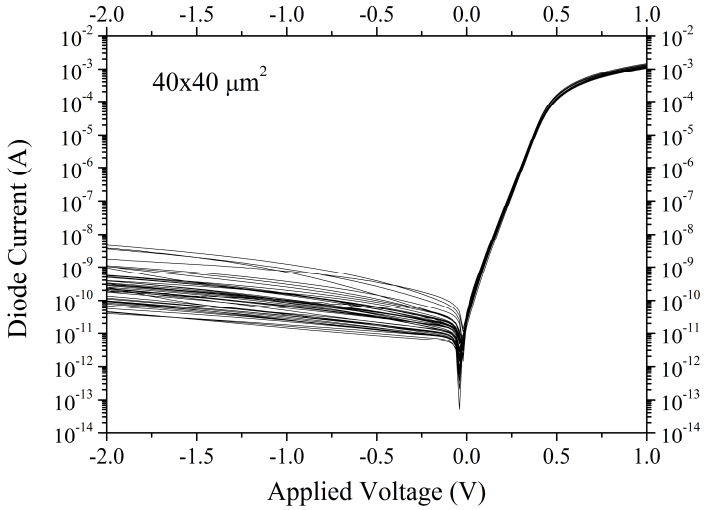
The PureGaB Ge-on-Si diodes are noteworthy in that they combine two novel processing techniques. For the first, a high-quality c-Ge is grown in tens-of-micron large windows to the Si with only a 300 nm transition region to getter misfit dislocations. An example is shown in Fig. 6 where also the growth of c-GaAs on the c-Ge is displayed. Second, when the window is filled with Ge, a nm-thin layer of PureGa is deposited at 400ºC and capped with a layer of PureB as schematically shown in Fig. 7. Under the applied conditions, directly depositing PureB did not provide the desired p^+ interface layer but as a capping layer it is instrumental in forming a barrier layer to the Al-metallization. To our knowledge the resulting I-V characteristics have uniquely low values of reverse current, series resistance and ideality factors as well as a good uniformity over the wafer, as illustrated by Fig. 8. The success of this PureGaB/Ge-on-Si combination may well be dependent on the fact that the whole diode fabrication is performed in one deposition cycle which has given the surprising result that no extra steps were needed to get good passivation of the diode perimeter.

These first PureGaB Ge-on-Si diodes have also been tested as infrared photodiodes and photon counting capabilities in Ge were demonstrated for the first time

[16]. An additional attractive feature is the quite planar surface after Ge-growth, as seen in Figs. 6, which makes this a straightforward add-on to standard Si technology. Nevertheless, the diode structure is many times more complex than the planar PureB Si diodes because loading effects are very prominent during the Ge deposition and the n-doping of the Ge. This makes the implementation in applications much less flexible.



Fgure 7. Schematic process flow for the fabrication of PureGaB p^+n Ge diodes [5].



Fgure 8. I-V characteristics of PureGaB Ge-on-Si diodes measured over the wafer for devices with an area of 40×40 μm^2 [5].

Conclusions

The combination of precursors for growing both Si/SiGe and GaAs doped layers in one and the same CVD reactor have provided a powerful tool for forming pure-dopant-deposition p^+n junctions. The originally investigated PureB deposition, performed at 700ºC and in H_2 carrier gas, has been very extensively investigated and is optimized for integration in photodiode detectors for low-penetration-depth beams. Besides the attractive electrical characteristics, the layer itself excels in physical properties like uniformity and robustness during processing and optical exposure. The door to many more applications has been opened by introducing low-temperature deposition, down to 400ºC, of either B or Ga, both of which have been demonstrated to deliver Si diodes with the equally good electrical characteristics. This fact has lead to the proposition that the effectively high Gummel number of the resulting p^+-regions is related to the creation of acceptors states at the interface rather than being a property of the bulk dopant material. Similarly, on Ge, PureGaB has delivered diodes with exceptionally good I-V characteristics.

However, the physical properties of these newer deposition techniques are not immediately as attractive that those of PureB. Some of the trade-offs appear to be:

- low-temperature PureB is more readily integrated in CMOS but as a drawback a lower surface mobility of the B gives a higher surface roughness and poorer uniformity over the wafer,
- PureB deposits more readily in N_2 than in H_2 carrier gas, particularly at low temperatures, but here also the surface mobility of the B is much lower,
- The higher the PureB surface roughness, the more difficult it will be to achieve closed layers with the sub-3-nm thickness, compromising series resistance and optical transparency as well as the ease with which protection layers can be removed,
- PureGa effectively dopes Ge, unlike PureB, but is less robust with respect to oxidation and alloying with the Ge or metallization layers. A PureB capping layer can compensate for this but adds resistance.

All in all, we can conclude that while the fast commercialization of the PureB photodiodes fabricated at 700ºC in EUV and low-energy electron detectors has resulted in well-documented production-ripe PureB deposition and integration techniques, the full potentials of low-temperature PureB and Pure(Ga)B in either Si or Ge diodes have still to be determined. Nevertheless, the first results show that the potentials are enormous and no doubt the necessary research will be driven by applications as infrared Ge detectors, detector integration in CMOS and possibly also source/drain engineering in advanced CMOS.

Acknowledgments

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