A CMOS Temperature Sensor with a 49fJ·K2 Resolution FoM

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A CMOS Temperature Sensor with a 49fJ·K^2 Resolution FoM

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Abstract

This paper presents the most energy-efficient CMOS temperature sensor ever reported, with a resolution FoM of 49fJ·K^2, 2.7× better than the state-of-the-art. It consists of a Wheatstone bridge made from poly-silicon resistors, which is readout by a 2nd-order Continuous-Time Delta-Sigma modulator (CTDSM). This approach leads to a high resolution (160µK in 10ms) and a low supply-voltage sensitivity (< 20mK/V at room temperature).

Introduction

Temperature compensation schemes are essential parts of high-performance frequency references [1, 2]. To obtain low jitter and low power consumption, the associated temperature sensors must achieve both high resolution and energy efficiency. These requirements can be met by resistor-based temperature sensors, typically consisting of either Wheatstone [1, 3] or Wien bridges [4, 5].

Wheatstone bridges can be built from resistors with temperature coefficients (TCs) of opposite polarity, and so are more sensitive, and hence, more energy-efficient than Wien bridges, which employ a single type of resistor and a stable capacitive impedance. Moreover, unlike Wien bridges, which require a known reference frequency, Wheatstone bridges are self-referenced. In terms of energy efficiency, however, the state-of-the-art is defined by a Wien bridge sensor, which achieved a resolution FoM of 0.13pJ·K^2 [4]. This paper presents a Wheatstone bridge sensor whose resolution FoM is 2.7× better.

Proposed Design

As shown in Fig. 1a, the proposed temperature sensor consists of a Wheatstone bridge made out of a silicided p-poly (s-p-poly) resistor (R_p=105kΩ, positive TC) and a non-silicided n-poly resistor (R_n=95kΩ, negative TC). Compared to diffusion resistors [3], the s-p-poly resistor has a larger TC and a near-zero voltage dependency. To investigate the performance of the p-poly resistor, a bridge made from s-p-poly and p-poly resistors was also realized. Its resistances (R_p=67.5kΩ, R_n=64kΩ) are chosen to match the sensitivity of the s-p/n-poly bridge over the industrial temperature range -40°C to 85°C.

Current readout of a Wheatstone bridge, however, suffers from systematic non-linearity (NL). In the case when $R_p(T) = R_p(T_0)\cdot(1+\alpha\Delta T)$ and $R_n(T) = R_n(T_0) = R_p(T_0)$, i.e. the TC of R_n is much smaller than that of R_p, the bridge's output current will be given by:

$$I_{out} = \frac{V_{DD}}{2}\left(\frac{1}{R_p(T_0)\cdot(1+\alpha\Delta T)} - \frac{1}{R_n(T_0)}\right),$$

For an s-p/p poly bridge, simulations based on the TC specified by the foundry then result in a systematic NL of about 13°C after a 1st-order fit, (Fig. 1b).

As in [3], the Wheatstone bridge sensors are read out by connecting them to the virtual ground of the 1st integrator of a CTDSM (Fig. 2). The modulator's resistive DAC (R_{DAC}=140kΩ) will then null their output current. In this read-out scheme, the bitstream average is only determined by the ratios between R_p, R_n and R_{DAC} (same type as R_n) and so is independent of the supply voltage. To minimize its input impedance, the 1st integrator is based on an Opamp rather than an OTA. For energy-efficiency, the modulator employs a 2nd-order feedforward topology, with the feedforward factor implemented by R_{ff} (Fig. 2).

In this work, in contrast to [3], the offset and 1/*f* noise of the 1st integrator are suppressed by chopping. To avoid aliasing high-frequency quantization noise at the chopping transitions [6], the chopping frequency is the same as the sampling frequency (500kHz).

The opamp of the 1st integrator is a two-stage design consisting of a telescopic OTA and two PMOS source followers, while the 2nd integrator consists of a telescopic OTA with a source-degenerated NMOS input pair. From simulations, the 1st and 2nd integrators dissipate 100µW and 7µW, respectively, from a 1.8V supply. The bridges dissipate 32µW (s-p/n-poly) and 25µW (s-p/p-poly).

Measurement results

The two Wheatstone bridge sensors were fabricated side-by-side in a TSMC 180nm process (Fig. 3). They share the same clock and constant-g_m biasing circuits and each occupy 0.72mm^2, which is dominated by the large capacitors (2 × 180pF) of the 1st integrator. For flexibility, the sinc^2 decimation filter is realized off-chip.

Twenty samples from one wafer were characterized in ceramic packages from -45°C to 85°C in a temperature-controlled oven. For stable measurements, the samples are placed inside an aluminum block, which reduces temperature fluctuations to the 1mK level. The bitstream averages of the two sensors are shown in Fig. 4. After a 1st-order fit, the measured NL agrees well with simulations (Fig. 1b), indicating that it is indeed mainly due to the current readout scheme. After removing this systematic NL, the resulting spread is below 0.07°C (3σ) for the s-p/p-poly sensor, and below 0.10°C (3σ) for the s-p/n-poly sensor. In a conversion time (T_{conv}) of 10ms, the s-p/n-poly sensor achieves a thermal-noise limited resolution of 164µK (Fig. 5). The observed 1/*f* noise is mainly due to the non-silicided poly resistors [4], resulting in a 10Hz corner frequency for both sensors. At room temperature, the power supply sensitivities of both sensors is less than 16mK/V (Fig. 6).

In Table I, the performance of the proposed temperature sensor is summarized and compared to the state-of-the-art. Its 49fJ·K^2 resolution FoM is 2.7× better than that of [4], and is similar to that of a recent MEMS-based sensor [2]. Also, its power-supply sensitivity is close to a state-of-the-art BJT-based sensor [7].

References

[1] M. H. Perrott *et al*., *JSSC*, Jan. 2013.
[2] M. H. Roshan *et al*., *JSSC*, Jan. 2017.
[3] C. H. Weng *et al*., *JSSC*, Nov. 2015.
[4] S. Pan *et al*., *ISSCC*, Feb. 2017. in press.
[5] P. Park *et al*., *JSSC*, Apr. 2015.
[6] S. Billa *et al*., *ISSCC*, Feb. 2016.
[7] B. Yousefzadeh *et al*., Circ. Symp *VLSI*, June. 2016.

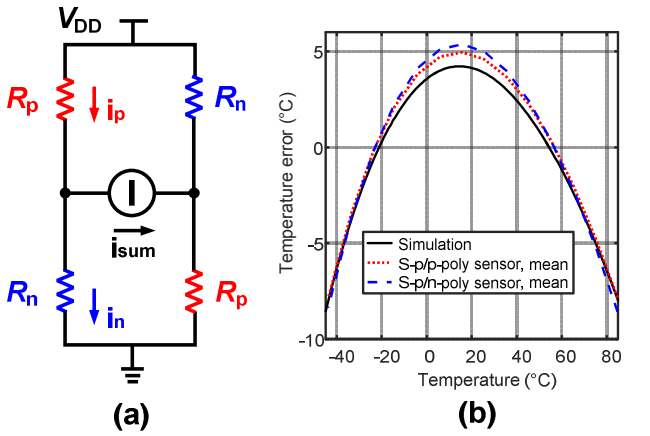

Fig. 1. (a) Wheatstone bridge sensor front-end with current readout scheme; (b) Measured and simulated NL for the two current-readout Wheatstone bridge sensors, after a 1st-order fit.

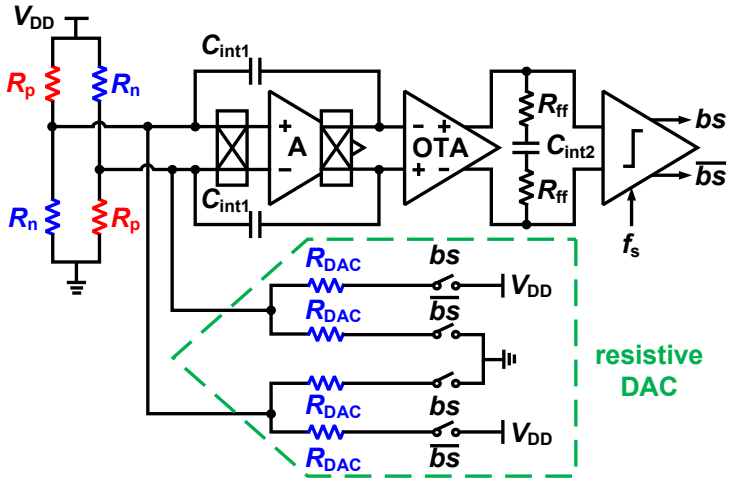

Fig. 2. Full system block diagram.

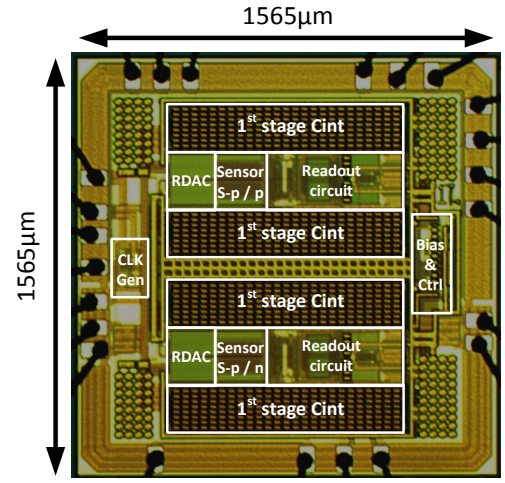

Fig. 3. Die micrograph of two side-by-side sensors.

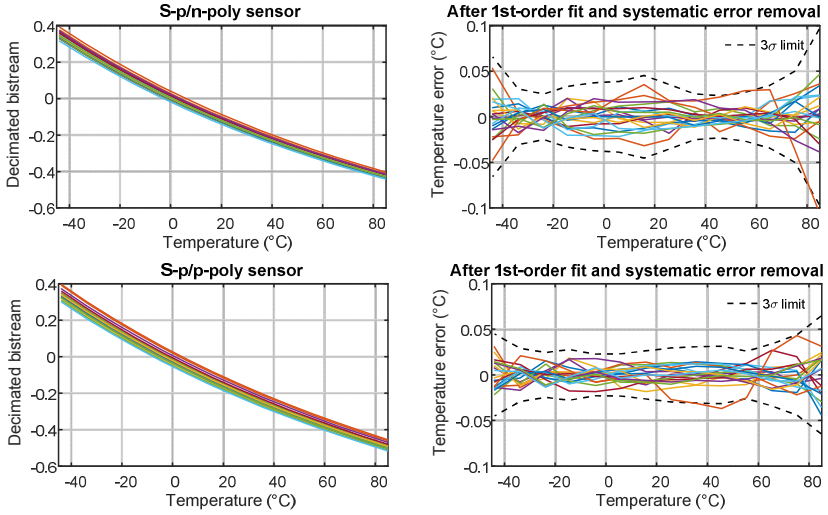

Fig. 4. Decimated bitstream vs. temperature (left) and temperature error (right) after 1st-order fitting and systematic NL removal for s-p/n-poly (top) and s-p/p-poly (bottom) sensors.

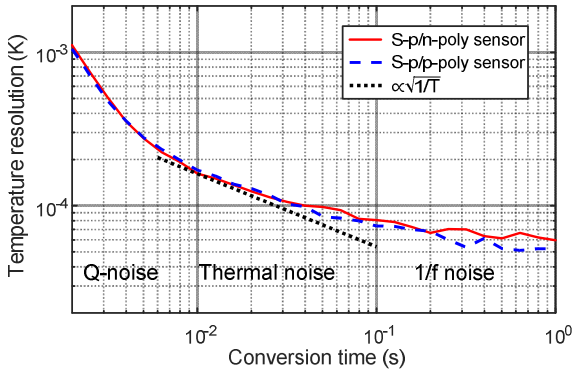

Fig. 5. Resolution vs. conversion time at room temperature.

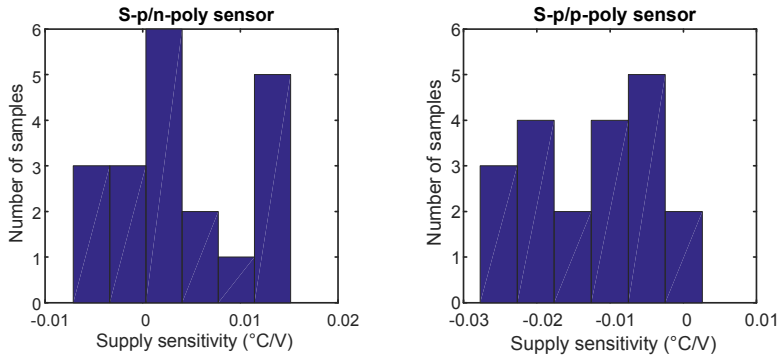

Fig. 6. Power supply sensitivity at room temperature.

TABLE I. Performance summary and comparison with the state-of-the-art

	Sensor type	Tech (µm)	Area (mm²)	Power (mW)	T. Range (°C)	Resolution (mK)	T_{conv} (ms)	Trim points	Inaccuracy (±3σ error)	PSS (°C/V)	Res. FoM (pJ·K²)
This work	Resistor	0.18	0.72	0.18	-40—85	0.16	10	2[a]	±100mK	0.016	0.049
[4]	Resistor	0.18	0.72	0.16	-40—85	0.41	5	2[a]	±70mK	-0.17	0.13
[1]	Resistor	0.18	0.18	13	-40—85	0.1	100	6	±15mK[c]	--	13
[3]	Resistor	0.18	0.43	0.065	-40—125	10	0.1	2[b]	±400mK	0.4	0.65
[5]	Resistor	0.18	0.09	0.031	-40—85	2.8	32	3	±120mK[c]	-0.4	8
[7]	BJT	0.16	0.16	0.007	-70—125	15	5	1	±60mK	0.01	7.3
[2]	Dual-MEMS	0.18	0.54	19	-40—105	0.02	5	--	--	--	0.04

[a] 1st-order fit. [b] 1-point trim with 1st-order curve fitting. [c] Min or Max.