Encapsulated thermopile detector array for IR microspectrometer

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ABSTRACT

The miniaturized IR spectrometer discussed in this paper is comprised of: slit, planar imaging diffraction grating and Thermo-Electric (TE) detector array, which is fabricated using CMOS compatible MEMS technology. The resolving power is maximized by spacing the TE elements at an as narrow as possible pitch, which is limited by processing constraints. The large aspect ratio of the TE elements implies a large cross-sectional area between adjacent elements within the array and results in a relatively large lateral heat exchange between micromachined elements by thermal diffusion. This thermal cross-talk is about 10% in case of a gap spacing of 10 μm between elements. Therefore, the detector array should be packaged (and operated) in vacuum in order to reduce the cross-talk due to the air conduction through the gap. Thin film packaging is a solution to achieve an operating air pressure at1.3 mBar, which reduces the cross-talk to 0.4%. An absorber based on an optical interference filter design is also designed and fabricated as an IC compatible post-process on top the detector array. The combination of the use of CMOS compatible materials and processing with high absorbance in 1.5 - 5 μm wavelength range makes a complete on-chip microspectrometer possible.

Keywords: Microspectrometer, Thermopile, IR detector array, Interference IR absorber

1. INTRODUCTION

Optical microspectrometers based on IC-compatible MEMS technologies offer significant benefits due to: small sample volume, fast response, small dimensions, weight and integrated circuits for signal pre-processing[1]. Spectroscopy in the Infrared (IR) spectral range has applications in agriculture, the food industry, soil biology, remote sensing and the chemical industry. The structure of the IR microspectrometer discussed in this paper comprises slit, planar imaging diffraction grating and TE detector array[2]. The dispersed IR spectrum is projected onto a 1-dimensional detector array. Therefore, the position of a spectral component within the IR spectrum is determined by the position of the element in the array. The response in terms of generated heat due to absorbed IR radiation at that particular element is a measure of the optical power within that part of the spectrum. The resulting localized increase in temperature is available as temperature difference relative to ambient temperature, which can conveniently be measured directly using a thermopile between the suspended absorber and the bulk silicon. The characteristic feature of a thermocouple of measuring temperature difference rather than temperature makes the integrated system insensitive to variations in the temperature of the bulk of the chip. High-sensitivity of an element in the thermopile-based IR detector requires minimum thermal conductance between absorber and heat sink. Micromachining technologies are generally employed for the removal of the thermal shunt of any bulk silicon or oxide underneath the TE detector for maximum sensitivity. These techniques and their effect on the sensitivity of IR detectors have been extensively studied[3].

Micromachining technologies are mainly divided into two categories: bulk and surface micromachining. Wafers are subjected to a CMOS process and are subsequently etched from either front or backside of substrate to realize free-standing MEMS structure in bulk micromachining. The chemical etchant often utilized in the backside etching is KOH. The device has free spacing to the end of substrate in the vertical direction. This backside etching is an advantage for fabrication of thermally isolated on-chip devices. However, the long etching time is needed due to the thick substrate. Another issue is that a large footprint is unavoidable due to the anisotropic etching of KOH along a crystal plane. Thi disadvantage is avoided in surface micromachining. The shorter etching time makes this technique suitable for realizing inertial sensors (e.g. accelerometer or gyroscope) for the mass production application. However, the narrow gap between the MEMS structure and the substrate significantly decreases the performance of thermal, because of the increased air conduction. The resulting heat loss greatly decreases sensor performance. As a result, most MEMS-based thermal are realized using bulk micromachining.

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This paper reports on an IR thermal detector array fabricated using a CMOS compatible MEMS process using surface micromachining with subsequent encapsulation by thin film technology. Thin film encapsulation technology is applied to achieve low pressure inside the array cavity, which hugely reduces thermal diffusion cross the air gap to heat sink[4]. The surface micromachining limits process complexity and reduces etch time, during which the already integrated microelectronic devices should be protected. The thermal cross-talk analysis is presented in section 2 and shows it is reduced to 0.4% due to the low pressure inside the cavity. Polysilicon is selected as the thermoelectric material for reasons of CMOS compatibility. Although neither Polysilicon nor SiN, which is used as support structure, absorb IR in the 1.5 - 5 μm wavelength range, a thin-film PolySi/SiN based interference filter has been designed and fabricated to act as efficient IR absorber to improve the IR absorptance. This part of the detector is described in section 3. The simulation result shows that more than 80% of IR is absorbed.

2. CROSS-TALK REDUCTION BY THIN FILM ENCAPSULATION

2.1 Background

Conduction, convection and radiation are the three mechanisms of loss in thermal and IR thermal sensor. The thermal transfer due to these three mechanisms acting on the TE element is described in detail in literature[5]. An array of 20 TE elements, each on a bridge structure of 650×36 μm^2 is designed and fabricated. The volume around an element is small and the effect of gas pressure on the performance of detector has to be considered. The gas conductivity determines the residual thermal cross-talk and, consequently, the lower limit of what can actually be achieved by the optimised design of the support structure and the structural separation of the elements. For typical MEMS-based detectors the expression for thermal conductivity of air between two plates within an enclosed cavity as a function of pressure and temperature can be approximated as:

$$\kappa_{air} = \kappa_o \times \frac{1}{1 + \frac{7.6\times10^{-5}}{p \times \frac{D}{T_{avg}}}}. \qquad (1)$$

where κ_o, p, D, T_{avg} denote: the thermal conductivity of air at room pressure and temperature, the pressure, the distance between the plates and the average temperature of the plates respectively. When assuming a plate spacing of 10 μm, an average temperature of 300K and κ_o= 0.0284 Wm^{-1}K^{-1}, a pressure-dependent thermal conductivity of air results as shown in the Fig 1(a).

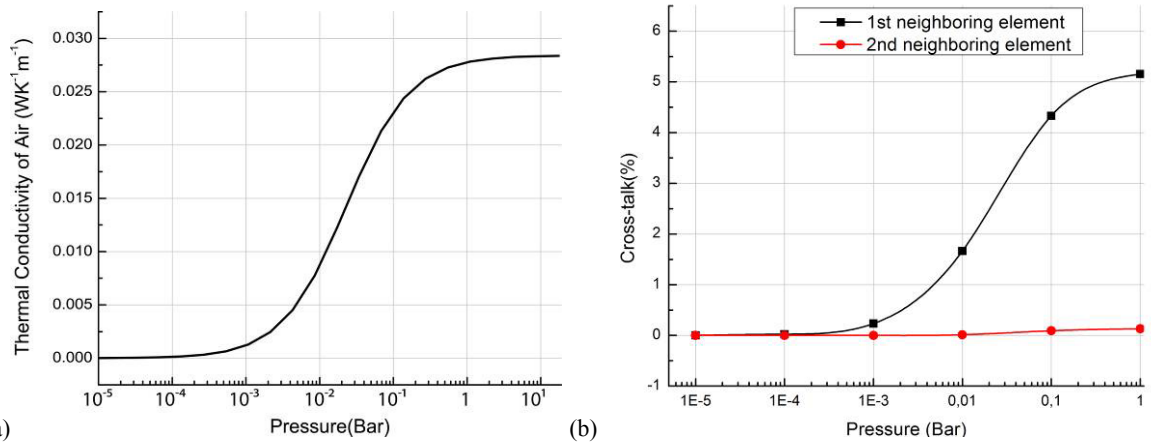

Figure 1. (a) Air thermal conductivity as a function of pressure. (b) FEM simulation of cross-talk on three TE elements.

Several layers are stacked during fabrication of the meander-shaped thermopile deposited on top of supporting membrane. This is a 2-dimensional problem with heat flux between several objects. Therefore, numerical methods are required. The commercially available Finite Element Method (FEM) software, COMSOL[6] has been used to solve the

heat transfer equation. One element is given the constant heat flux in the middle position (the absorption area) of the bridge to create the temperature difference between the absorber to the bulk silicon where the temperature is constant. The temperature difference of the thermopile sensing area of the heated element is taken as the reference, while the temperature difference of two successive neighboring elements indicates the cross-talk. The simulation result of cross-talk as a function of pressure, while assuming a constant ambient temperature at 300K, is shown in Fig 1(b). The overall cross-talk in air pressure is 10% by taking two times of single side simulation result. Assumed the device is operated in 0.1 mBar pressure, the cross-talk is further reduced to 0.4%. The thin film encapsulation technology is applied with PECVD which has the process chamber around 0.1 mBar. Therefore, the cross-talk can be reduced.

3. INTERFERENCE BASED IR ABSORBER

3.1 Introduction

The sensitivity of the thermal detector critically depends on the absorber, which determines the efficiency in which impinging IR radiant flux is converted into localised heat at the hot junction. Traditional IC-compatible materials, such as Si, SiO_2 and SiN, are not efficient absorbers in the near-IR spectral range. Therefore, alternative absorbing coatings with opportunities for IC-compatible deposition have been investigated. Thin-film metals and polymers are within this category. Consequently, black polymer absorbers or black (porous) gold[7] or silver layers have been used in thermopile detectors for absorption of IR radiation.

Black polymer materials introduce too much stress in the 36 μm wide bridges in the thermopile array. Black gold and silver are marginally IC-compatible materials, since these introduce significant process complications. The use of interference absorbers for IR have been theoretically proposed and practically verified in previous works[8-9]. However, the concept has not been implemented in a surface micromachined thermopile array. Figure 2 shows the processing steps for the fabrication of the thermopiles including the interference absorbers. Interference absorbers include two Ti layers with a dielectric spacing. A SiC layer deposited on top of the metallic based absorber protects these layers in the subsequent sacrificial etching step.

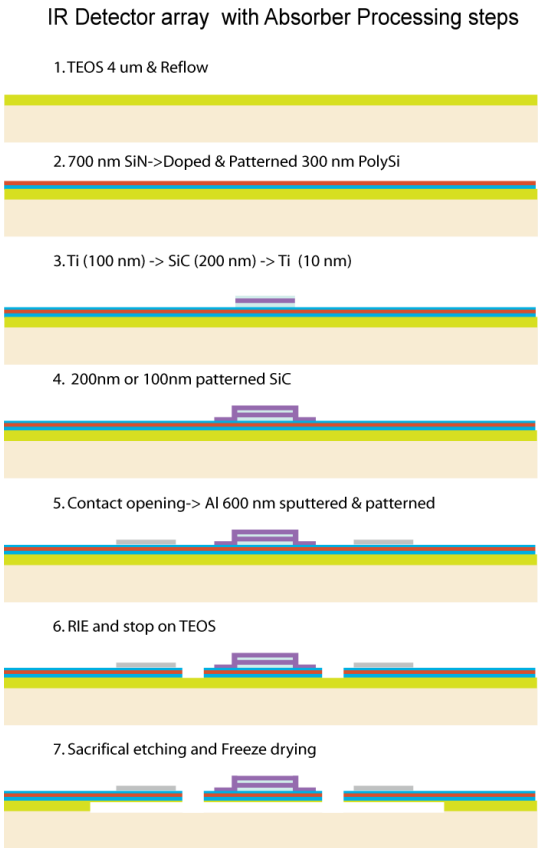

Figure 2. Processing steps for the IR thermopile array.

The interference absorber consists of a thick Ti layer, a dielectric cavity layer and a thin Ti layer. Another dielectric layer is deposited on top of the 3-layered interference filter to protect the layers during the sacrificial etching step. SiC is preferred to SiN for this purpose, because of the good resistance during high concentration HF etching and acceptable optical properties in the IR. As it is shown at step 6 in Fig. 2, the protective layer is covering the area of absorber layers. In the mask, the protective layer is designed to overlap the absorber area 2 μm out of it. Al is sputtered to make contacts before the sacrificial etching. Since Al is unprotected, high concentration HF is used for sacrificial etching, which etches Al very slowly, rather than BHF[10-11]. RIE is used to separate the bridge structures as shown in step 8 followed by sacrificial etching. Freeze drying is performed to avoid stiction of the released structures.

3.2 Design of the absorber

The thin-film optical software package TFCalc 3.3 has been used to simulate and design the interference based absorbers. Ti is chosen as the metallic layer of the absorber. The optical properties of Ti are measured using ellipsometry on a test sample. Optical properties were measured up to 1.2 μm wavelength by ellipsometry. Figure 3 shows the refractive index and extinction coefficient of Ti for wavelengths up to 1.2 μm.

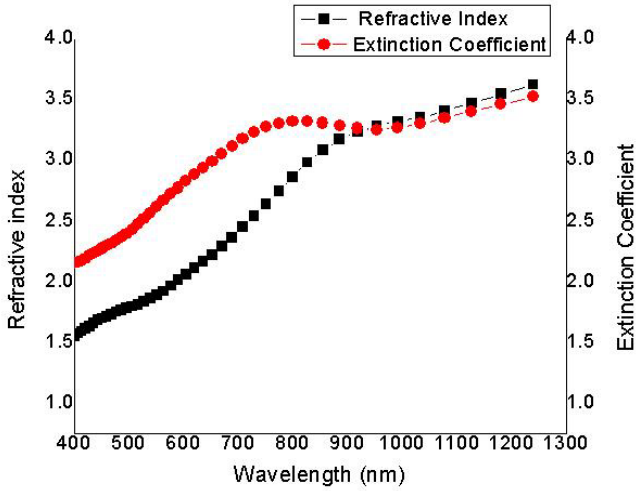

Figure 3. Measured optical properties of sputtered Ti.

The absorber consists of one dielectric centre layer with thin-film Ti layers on either side. PECVD SiC has been used as the dielectric spacing layer. SiC is to be preferred because of the high resistance to HF etching. Another advantage of using SiC for the spacing layer is the decreased process complexity, since it is also used for the protective coating. Prior to the design, the optical properties of PECVD SiC have been measured by ellipsometry. Figure 4 shows the measured optical properties of PECVD SiC, which are in agreement with the values reported in literature[12].

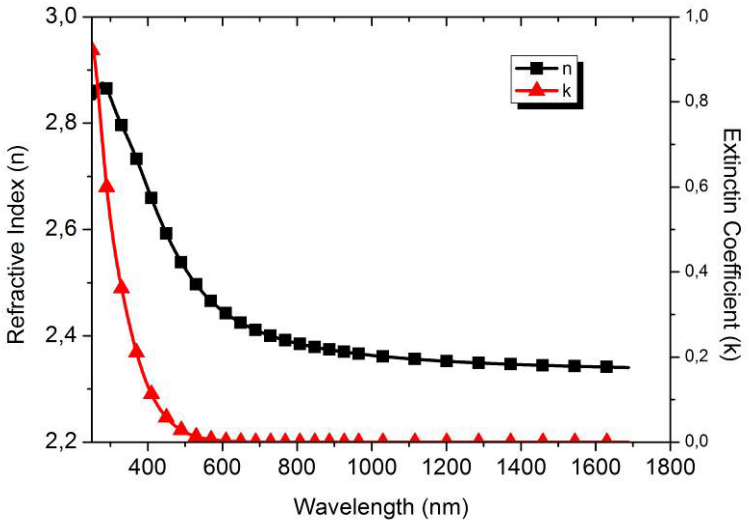

Figure 4. Measured optical properties of PECVD SiC.

The Ti (100 nm)/SiC (200 nm)/Ti (30 nm) three stacks interference absorber with additional SiC (200 nm) protective layer are purposed. It results a 4-layered Ti/SiC/Ti/SiC stack as the IR absorber. Optimal absorber design on the layer thickness is achieved in Fig. 5 by also taking the bridge layers into account. The relatively high absorptance covers from 1.5 μm to 5 μm wavelength range. This wide spectral range could be applied to some targets for gas spectroscopy application.

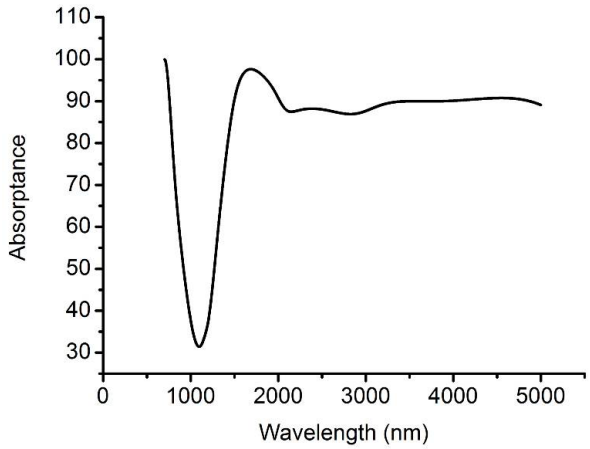

Figure 5. Simulation result of optimum design of IR absorber on Ti /SiC stacks.

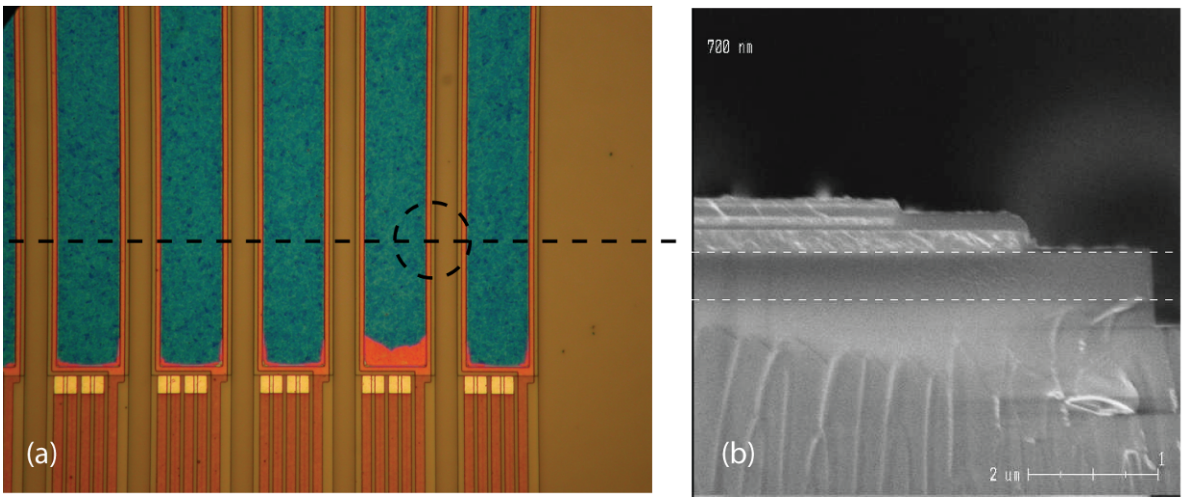

Figure 6. (a) Zoom-in photo of fabricated detector array with absorber stack. (b) SEM of cross-section of bridge before structural release.

3.3 Fabrication of the absorber

The fabrication of thermopile detector array starts with a 4 μm PECVD TEOS as the sacrificial layer. The process used for the fabrication of the uncoated TE elements has been described in detail in previous work[2]. This section is focused on the fabrication of absorber and realizing of bridge structure. The CMOS compatible bridge fabrication stops at the second SiN layer and is followed by deposition of the layer stack used for the absorber. The contact hole etching and metalization are completed prior to sacrificial etching. The process steps for the absorber are: The first 100 nm Ti is sputtered followed by the patterning step to define the thin film in the middle position of the bridge. SiC with 200 nm thickness is deposited with PECVD process. Next, the second 30 nm Ti is sputtered and patterned on top of SiC layer. Second 200 nm SiC is deposited on top of layers to form SiC/Ti/SiC/Ti four-layer stacks. Two SiC layered are etched and patterned, followed by contact hole and metallization process. Reactive ion etching is implemented in a final step to form the bridges in the detector array out of membrane. The fabricated device before sacrificial release is shown in Fig. 6(a). This zoom-in figure shows the absorber and part of the thermocouples. Excess under etch is found at the rim of absorber and is indicated by the color difference. The SEM photo has been taken to show the cross section of absorber in Fig. 6(b). Two Ti layers together with a 200 nm SiC layer forms a sandwich structure. The thickness of the upper SiC layer is below the target design value and fails to act as protection layer. The insufficient coverage by the protection layer is examined at the sidewall. As a result underetching is observed at the rim of the absorber, due to partly removal of the thin Ti layer.

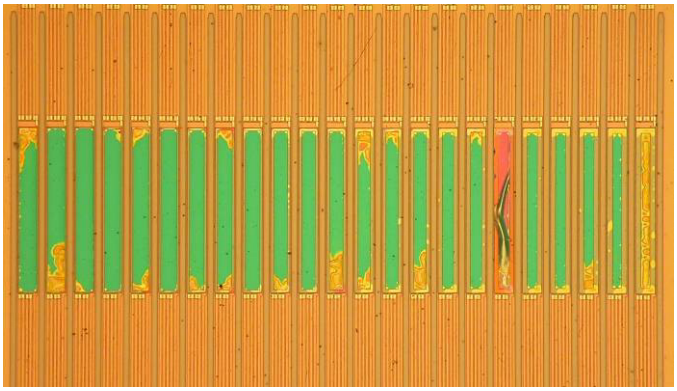

Figure 7. A photograph of the fabricated TE array.

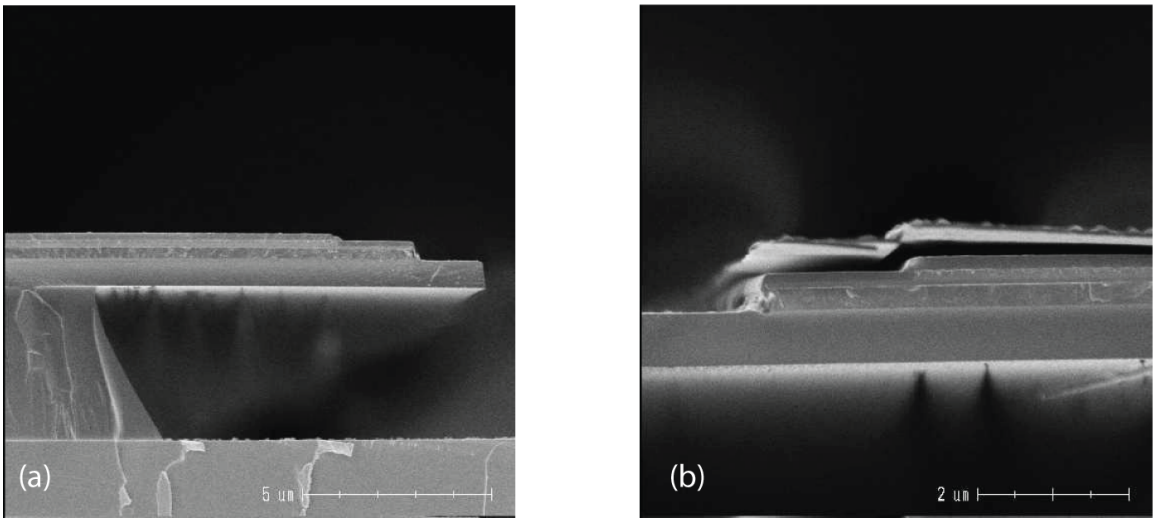

Figure 8. (a) SEM of cross-section of bridge after releasing. (b) SEM on the sixth of bridge elements from the left of Fig. 7.

Sacrificial etching is performed to realize structures with reduced thermal diffusion in the direction normal to the plane in which the TE elements are integrated (i.e. vertical). The width of a bridge is 36 μm with spacing of 10 μm. HF at 73% was used as the etchant due to the relatively slow etch rate of aluminium. The etch rate is determined by initial tests and was found to be 1740 nm per minute. The total etching time is set to 10 min and 30 sec by considering the etching rate and the width of the bridge. After that the die is rinsed in IPA for several times to remove HF. To prepare for freeze drying, the die is immersed in Cyclohexane solution for 10 minutes. Freeze drying is performed to avoid stiction of the released structures. Figure 7 shows a photograph of fabricated TE array. The photo clearly shows the color difference compared to the array before sacrificial etching. Therefore, SEM is utilized to check the cross-section of the absorber on the bridge. Figure 8(a) shows that the top SiC and the thin Ti layer are removed after sacrificial etching. Figure 8(b) is taken on the sixth of bridge elements from the left of Fig. 7. The top SiC layer is floating, since the thin Ti layer underneath is removed during etching. Consequently, the absorber is incomplete after the sacrificial etching.

Another test was performed to check the cause of the Ti attack. Two samples were etching in HF in different but shorter time as shown in Fig 9. The first sample was etching 30 seconds and examined under microscope. The thin Ti layer is etched starting from sidewall and some pinholes of SiC were found. Second samples were etched in HF for 60 seconds. Side etching of thin Ti layer is more prominently and more pinholes are verified. The top SiC layer is floating at the parts where the Ti layer was attacked.

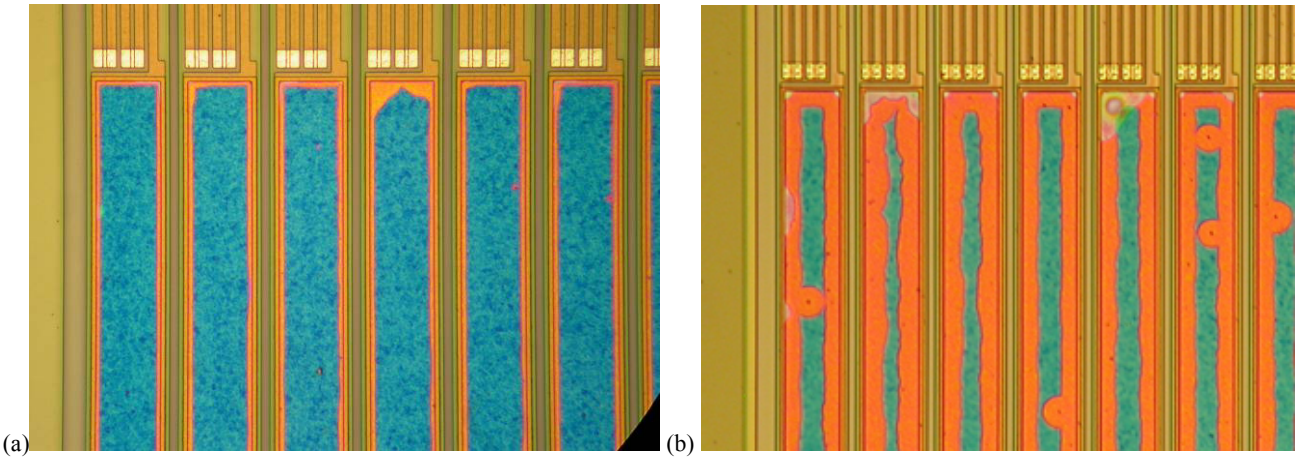

Figure 9. (a) HF etching for 30 seconds. (b) HF etching for 60 seconds.

3.4 Measurements

The measurement of device from section 2 has not been achieved due to the side wall and pin holes problems. Instead, thin-film SiC(200 nm or 100 nm)/Ti (10 nm)/SiC (200nm)/Ti (100 nm) absorber layers have been deposited by sputtering on two different silicon wafers. A LAMBDA 950 spectrophotometer has been used for the measurement. The reflectance from the wafers and transmission through the wafers have been measured. Transmission through the wafers is measured to be negligible for all the wafers and the absorptance can be easily calculated. Figure 10 shows the comparison between the simulation and reflectance measurements. These are in reasonable agreement, hence, the experiments validate the simulation results. Considering the non-zero throughput in the stack, absorptance is calculated and shown in Fig. 11.

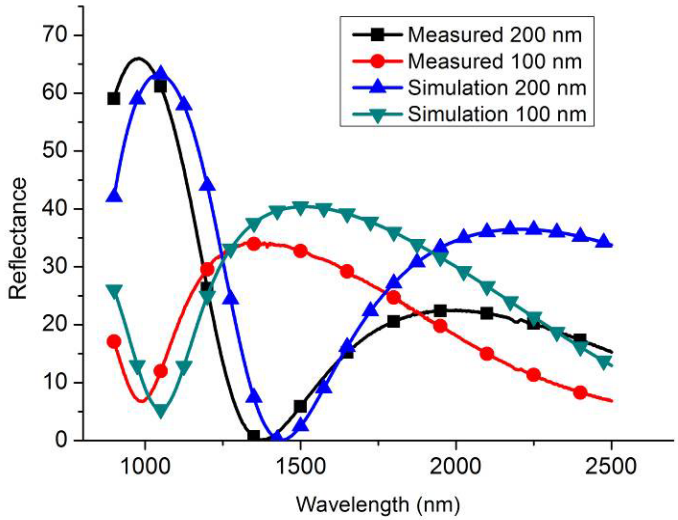

Figure 10. Comparison between the measured and simulated reflectance for SiC-based interference filters.

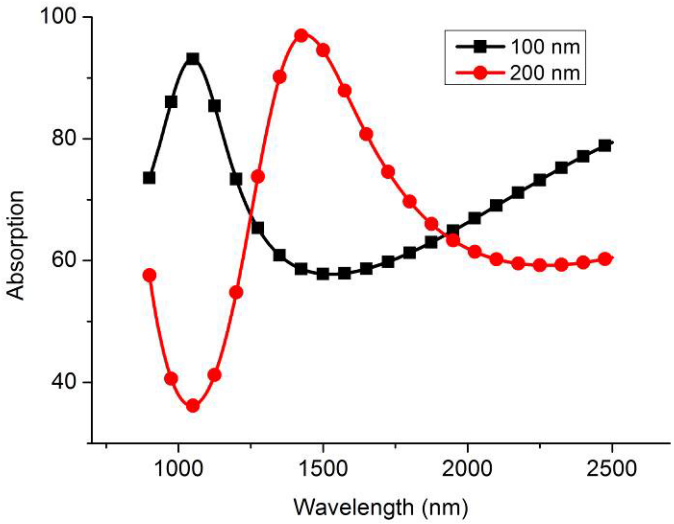

Figure 11. Measured absorptance of SiC-based interference absorbers.

4. CONCLUSIONS

The design and fabrication of a CMOS compatible thermopile array for use in a miniaturised infrared microspectrometer has been presented. The dimensions of the thermopile detector array are dictated by the optical properties of the imaging grating. The design is categorized into two aspects: detector array and single TE element. Thin film encapsulation technology is implemented to reduce the pressure of cavity of device which results the minimum cross-talk between TE elements and to improve sensitivity. The cross-talk of array is estimated to be 0.4% due to the low pressure (1m Bar).

The second aspect is to design and fabricate the CMOS compatible interference filer based absorbers for single TE element. Although interference filter based absorbers introduce a spectral dependence in the response, the stress introduced by techniques based on black polymer absorbers is avoided. Therefore, the interference filter based approach presented here can be used on the narrowly spaced and thin micromachined bridges that are typically used in high sensitivity MEMS thermopile detectors. SiC has been used as the spacing layer in the interference absorbers stacks, together with Ti to form the sandwich structure. SiC is relatively resistant to HF etching compared to SiO_2. However, side wall and pin holes issues are addressed and needed to be taken into account during design phase. The experiments validate the simulations, which implies that the simulation tools and our material data can be used in future designs.

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