Delft University of Technology
Faculty of Electrical Engineering, Mathematics
and Computer Science
Electronic Instrumentation Laboratory

MSc Thesis

Design of High-Resolution Photodiode Readout Circuitry for a Bio-Implantable Continuous Glucose Sensing Chip

Umanath R Kamath

Dr. David San Segundo Bello
Senior Design Engineer,
IMEC,
Belgium.

Dr. ir. Michiel A.P Pertijs
Associate Professor,
Delft University of Technology
The Netherlands.

Members of Thesis Defense committee

Dr. ir. Michiel A.P Pertijs,

Associate Professor, Electronic Instrumentation, TU Delft

Dr. ir. Reinoud F. Wolffenbuttel,

Associate Professor, Electronic Instrumentation, TU Delft

Prof. dr. ir. Edoardo Charbon,

Professor, Circuits and Systems, TU Delft

Dr. David San Segundo Bello,

Senior Design Engineer, IMEC

Design of High-Resolution Photodiode Readout Circuitry for a Bio-Implantable Continuous Glucose Sensing Chip

by

Umanath R Kamath

Submitted to the Department of Electrical Engineering, Mathematics and Computer Science on November 28, 2012, in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering at Delft University of Technology

Glucose sensors are useful for monitoring and control of blood-sugar concentration for diabetic patients. There are many challenges in their wide-spread use and effectiveness in control of the disease. This work is a step towards achieving in vivo continuous long-term glucose monitoring using the optical near-infrared based glucose sensing principle.

The thesis investigates and arrives at an architecture for the readout circuitry of such a sensor system. The goal is that the realized CMOS chip together with the optical sensing devices realized in Silicon-on-Insulator technology will form a single-implantable solution. The advantage is the long-term monitoring due to non-usage of chemical reagents. The thesis work addresses the read-out circuit requirements for a photodiode as part of such a sensor. The design of a high-resolution current-input sigma-delta ADC is discussed which targets to achieve 16-bit resolution for a photo-diode signal in the range of 100nA-10μA. Various optimizations for specifications such as noise, accuracy and energy-efficiency both at circuit and system level are addressed.

The chip has been realized in a TSMC 0.18μm process. The initial measurements show the functionality of the ADC and its performance using the test set-up devel-

oped. A proof of concept of the optical-electrical interface with a photodiode shows the application of the circuit.

Thesis Supervisors: Dr. David San Segundo Bello* and Dr. ir. Michiel A.P Pertijs**

Title: *Senior Design Engineer, IMEC and **Associate Professor, TU Delft

Contents

List of Figures

List of Tables

1

Introduction

Continuous glucose monitoring sensors are an effective solution to the problem of diabetes control. In vitro methods such as the finger prick method provide a useful and accurate solution at the cost of discomfort to the patient,while existing continuous in-vivo sensors such as those based on electro-chemical techniques have a short operational period due to the requirement of replenishment of sacrificial reagents thus requiring periodic surgical procedure. Thus there has been no comprehensive solution to this problem.

Near-infrared based sensing has been shown to have strong sensitivity to glucose in fluids and is the principle of glucose determination in our sensor. The target sensor will be used for in vivo monitoring, which can reach long operational efficiency as the optical method is reagent free. The required optical devices have been developed by Ghent University under the framework of the Glucosens project [3] which involves many collaborating research groups in Belgium. This thesis work contributes towards the design and realization of a CMOS chip that interfaces with the optical devices.

The transmission spectrum at near-infrared wavelengths decreases with increasing glucose concentration. The absorption properties of water and glucose are important for near-infrared spectroscopy in biological organisms. The spectroscopic information in near-infrared region corresponds to harmonics known as overtones and combinations of fundamental vibrations of the chemical bonds [4]. The ab-

sorption bands can be defined into a set of three spectral windows namely the short-wavelength near-infrared (14,285-8500 cm^{-1}), first-overtone (7500-5500 cm^{-1}) and combination (5000-4000 $cm^{-}1$) spectral ranges [5]. It can be seen from literature [6] [4] that glucose has a noticeable spectral signature which is characteristic in the first-overtone and combination bands. This has been confirmed by experiments at Ghent University(Appendix B). These characteristic spectrum together with a multi-variate calibration post-processing can effectively determine the glucose concentration in the fluid channel [7].

1.1 Organization of the thesis

The contribution of the thesis towards the sensor system is shown in figure 1.1.

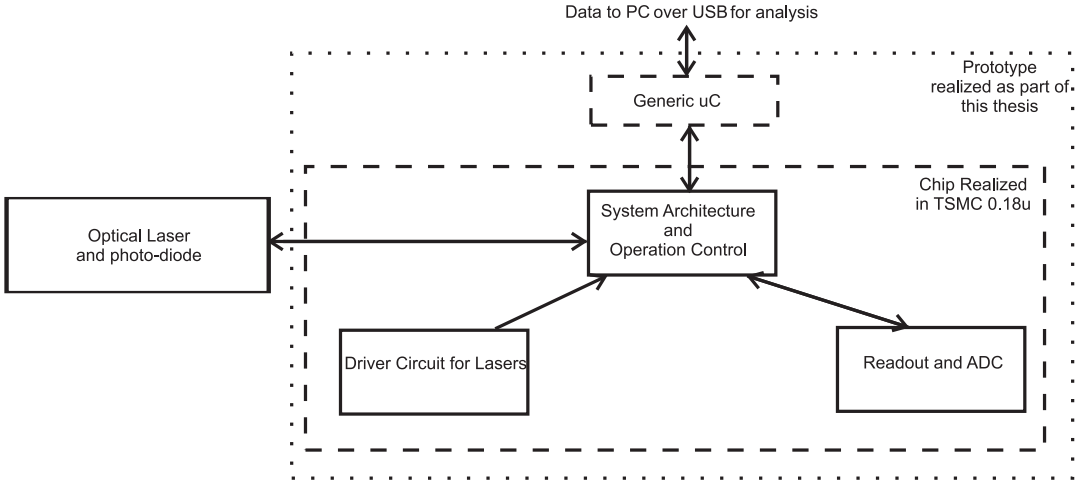

Figure 1.1: Contribution of this thesis towards final bio-sensor

In order to efficiently design the CMOS electronics, we need to understand the sensor and its characteristics, which forms Chapter 2. Given the various specifications derived from the signal, we move to the realization of the read-out architecture in Chapter 3, which explains the $\Sigma\Delta$ topology and its motivation. Subsequently system optimization for energy-efficiency is described and the final architecture model is verified by simulations. Chapter 4 describes the transistor level implementation,including the chopped first integrator, g_mC second integrator, clocked comparator and current DAC which form the sub-blocks of the ADC. Subsequently the

overall chip realization including the digital control and layout is shown in the same Chapter. Chapter 5 explains the test set-up used for evaluating the realized chip. This comprises of an interface to a generic micro-controller for configuration of registers and data transmission to the PC. Finally, section 5.1 gives the experimental results obtained for both electrical and optical tests. Chapter 6 concludes the work by analyzing the results and bench-marking our sensor realization with a similar read-out circuit.

2

System level design of the glucose sensor chip

This chapter begins by describing the architecture and operation of the overall sensor system. Subsequently we analyze the signal and its noise characteristics which set the requirements for the read-out channel and will form the basis for the derivation of the ADC architecture.

2.1 System architecture

The system architecture as defined in the Glucosens project for the prototype CMOS chip is shown in figure 2.1. The system can be divided into a transmitter and a receiver part. The optical part is implemented in Silicon-on-Insulator technology,which will be wire-bonded with the electronics on CMOS. The optical transmitter consists of thirty laser diodes (in both first overtone and combination band) which emit thirty different wavelengths to implement the spectrometer. Their output power depends on the driving current. The wavelengths of the lasers are chosen by design and is fixed apart from a small tuning range. The receiver consists of thirty photo-diodes whose sensitivity is wide-band across the spectrum of transmitted wavelengths. This principle of sensing is known as the evanescent method [6].

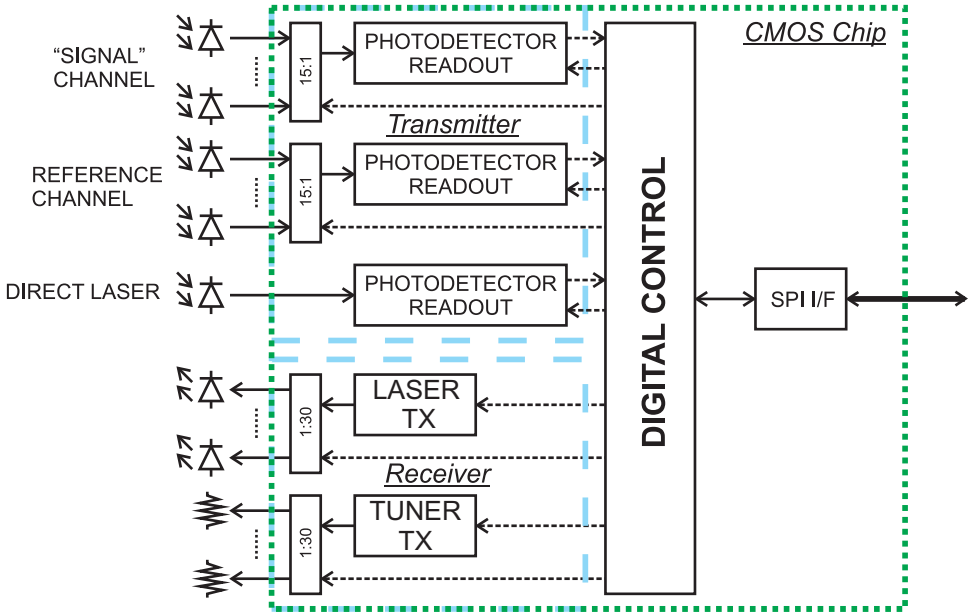

Figure 2.1: System Level description of the overall sensor system

The two parts of the target CMOS chip consist of the current driver for the lasers and the read-out electronics for the photodiodes. In addition to the current driver for laser, an identical driver is provided called the Tuner TX. This is used to dissipate heat across a resistor near the laser to be able to fine tune the output wavelength [1] in the first prototype system.

The power levels required for the current lasers are in the order of tens to hundreds of mW. The output current to the lasers is sourced by the LASER TX block in figure 2.1. This consists of a sourcing current DAC with a 10-bit current steering topology and a range selectable between 10mA and 100mA, which is re-used from an earlier work at IMEC. The control word to the DAC is configured by an SPI interface from an external micro-controller. The receiver part, which is the focus of this work, consists of thirty photo-diodes which are divided into two groups of fifteen each for detecting the glucose (signal channel) and water (reference fluid channel). The photodiodes of each group are multiplexed to one read-out circuit. An additional photodiode channel is provided for measuring the direct incidence of power from the laser source. The various controls such as the timing of the laser, output power from the laser, operation of the ADC are controlled by setting the corresponding

registers. In total there are fifty configuration bits, concerning the transmitter and receiver channel which are set by an external micro-controller via SPI communication explained in Appendix A.

2.2 Photodiode signal and noise characteristics

The output current from the photodiode depends on the fluid channel through which the incident power (P_{in}) from the laser passes and sets the dynamic range required from the read-out channel. This also depends on the operation of the photo-diode. The photo-diode can be operated either in photo-voltaic mode (zero bias condition) or in photo-conductive mode (reverse bias condition). In both these modes, the output signal consists of the signal current generated and an associated typical dark current offset.

The plot in figure 2.2 shows the V-I characteristics of the photo-diode under different light intensities. We choose to operate the photo-diode in the photo-voltaic mode because of the associated lower dark current. This can be attributed to the absence of excess dark current due to zero voltage bias across the parasitic shunt resistance of the photo-diode [8].

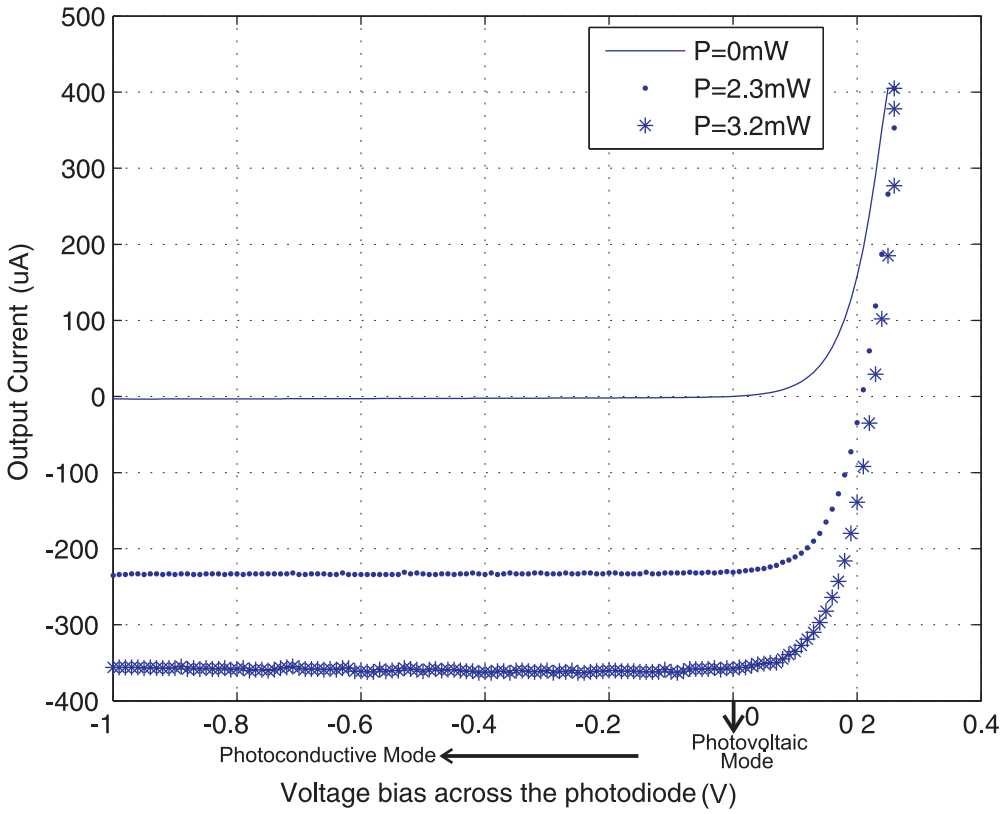

Figure 2.2: Measured response of the photo-diode for various incident power [1]

The photo-diodes operated in photo-voltaic mode, used in our design provide a current output of 100nA to $10\mu A$ with a typical dark-current offset of 1 μA. Any absolute signal measurement involves taking the difference of two readings i.e. signal plus dark-current, and dark-current.

In a photo-diode, the main noise is components are shot noise (P_{sn}) and Johnson noise (P_{jn}). Shot noise is related to the statistical fluctuations in both the photo current and the dark current whose power spectral density is signal dependent and given by $P_{sn} = \sqrt{2 * q * (I_{ph} + I_d)}[A/\sqrt{Hz}]$

Johnson noise is due to the associated shunt resistance R_{sh} of the photo-diode and given by $P_{jn} = \sqrt{\frac{4 * k * T}{R_{sh}}}[A/\sqrt{Hz}]$

Shot noise is the dominant noise source when the carrier generation (output

current) in the photo-diode is large. The total noise is given by

$$P_{noise} = \sqrt{P_{sn}^2 + P_{jn}^2}[A/\sqrt{Hz}] \tag{2.1}$$

The noise calculated based on our photodiode model is shown in figure 2.3. The maximum noise Power Spectral Density (PSD) is $2.1pA/\sqrt{Hz}$ at the maximum range of the input signal.

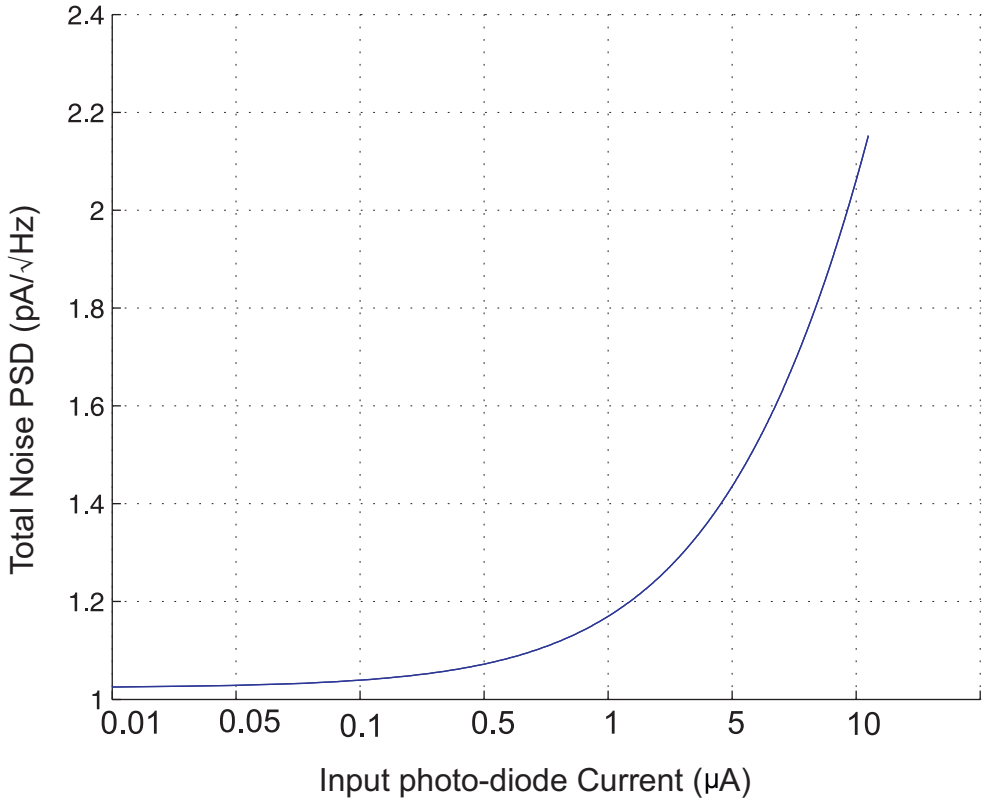

Figure 2.3: Power Spectral Density of photo-diode noise

2.3 Specifications of the readout circuit

The readout circuitry has to be designed to meet the required resolution as well as the rate at which the analog-to-digital conversion should take place from the application stand-point while minimizing power consumption.

2.3.1 Resolution and conversion time

The input signal to the read-out circuit is a current between $100nA$ to $10\mu A$ with an approximate offset of $1\mu A$ due to dark current.This signal has to be resolved with 16 bits of resolution i.e. the SNR to be achieved is greater than 98dB at $10\mu A$. The glucose concentration is determined by comparison of digitized value at successive instants and hence linearity is important.

From the glucose determination requirement, the thirty different responses to different wavelengths incident on the photo-diode need to be resolved within five seconds. This translates to an effective maximum conversion time per wavelength of at most 167ms.

2.3.2 Energy consumption

The total energy consumption of the sensor system depends on the transmitter and the receiver. The total power consumption in the transmitter can be between a few mW to few tens of mW which is an order of magnitude higher than the expected power budget for ADCs from literature which achieve comparable performance [9]. The total energy consumption is given by

$$E_{tot} = (I_{tx} + I_{rx}) * V_{supply} * T_{conv} \tag{2.2}$$

where I_{tx} and I_{rx} are the current consumption of the transmitter and receiver. Since I_{tx} can be expected to be much larger than I_{rx}, the readout circuit should be designed to have the least conversion time to make it energy-efficient. As per the system requirement, the maximum time for the laser to be ON is fixed at 167ms while there is no specified minimum time. The turn ON time of a laser diode is a few μs while the transmission time through the fluid is negligible. Therefore, the absolute minimum is fixed by the time required to achieve the required signal-to-noise ratio based on the photodiode noise characteristics.

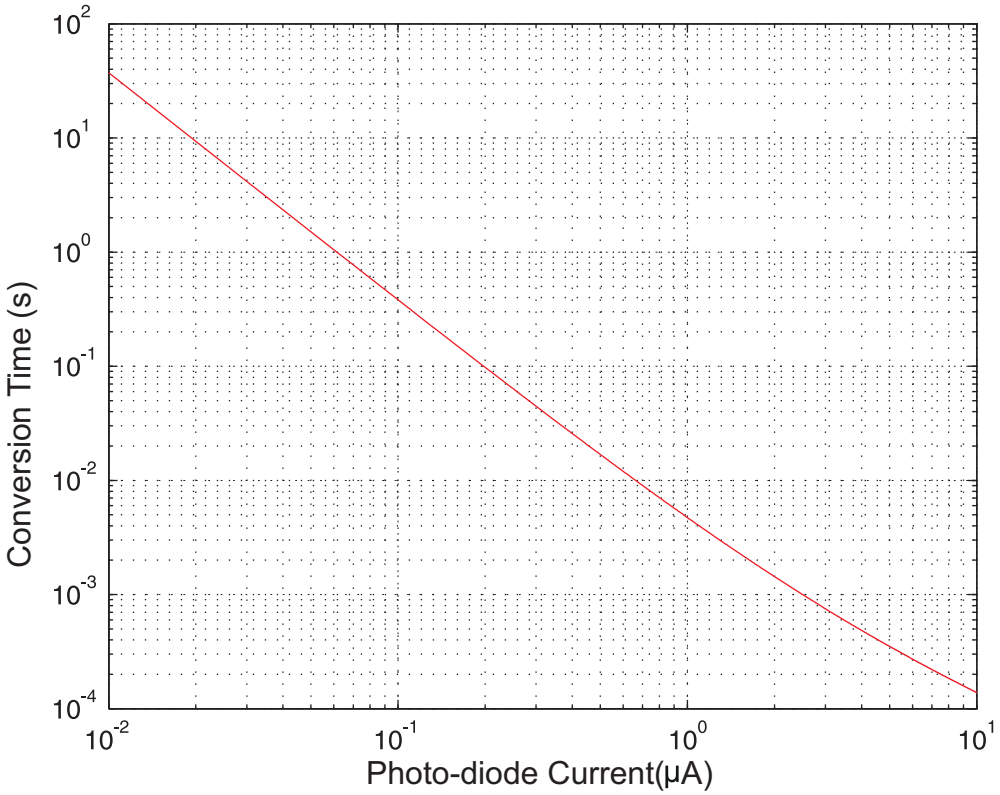

Figure 2.4: Measurement time for achieving 98dB SNR for various inputs

Figure 2.4 shows the conversion time needed to obtain 98dB at various photo-diode currents based on equation (2.3). The noise is assumed to be only contributed by the sensor.

$$SNR = 20 * log_{10}(i_{signal}/(P_{noise} * \sqrt{f_b})) \tag{2.3}$$

where i_{signal} refers to the input signal, P_{noise} refers to the total noise PSD from the sensor and f_b is equivalent bandwidth given by $\frac{1}{2 * T_{conv}}$, where T_{conv} is the time required for the conversion of the signal.

Our application demands a 98dB SNR at the maximum input signal and as a result we find the minimum conversion time of $T_{conv} = 126\mu s$ from the noise simulation in figure 2.4.

Based on the minimum conversion time, we can estimate a maximum equivalent

bandwidth f_b of the photodiode signal as 3.97kHz. Therefore the resulting integrated noise in the signal bandwidth is given by the maximum PSD over this bandwidth and results in 126pA. Based on this noise, the SNR can be calculated at various signal inputs using equation (2.3) as shown in figure 2.5.

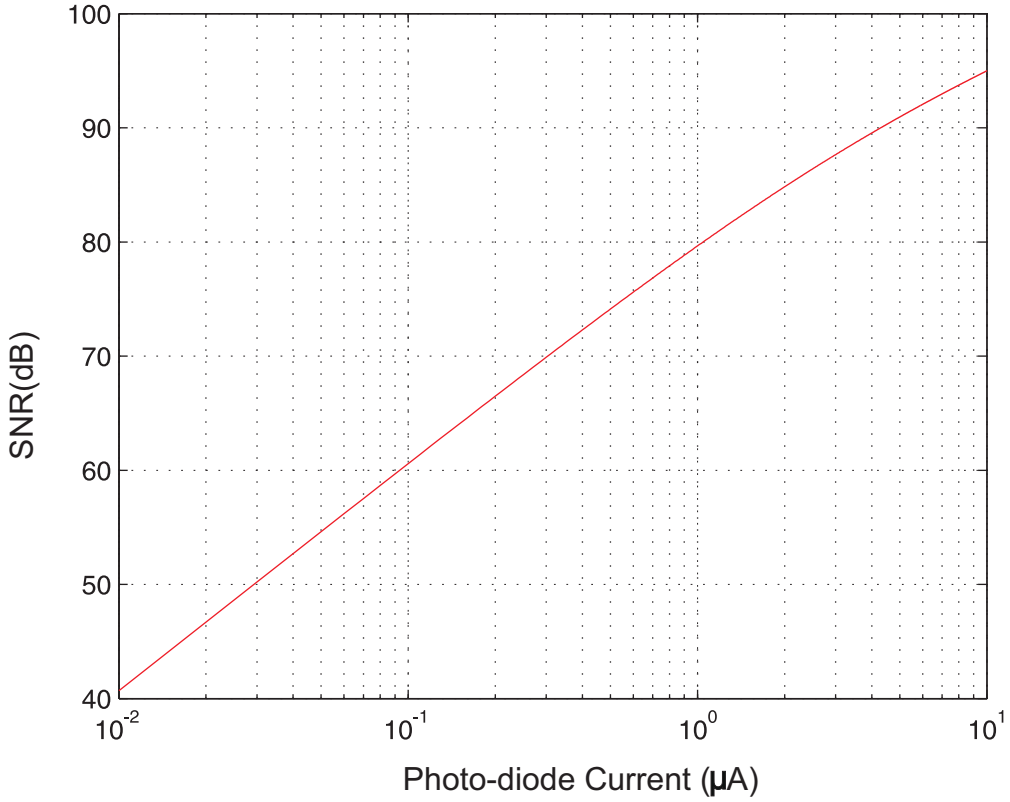

Figure 2.5: SNR versus Input Signal

In order to have the shortest conversion time and still achieve 98dB resolution, we need the integrated noise contributed by the readout to be negligible compared to 126pA. The factor by which the integration time increases as a function of additional noise contributed by the readout is shown in figure 2.6. The new conversion time T^*_{conv} required as a result of additional noise contribution by read-out is given by

$$T^*_{conv} = \frac{10^{SNR/20} P^*_{noise}}{i_{sig}} 0.5; \tag{2.4}$$

$$P^*_{noise} = \sqrt{P^2_{noise} + P^2_{readout}} \tag{2.5}$$

The y-axis is the fraction of the minimum conversion time, i.e $\frac{T^*_{conv}}{T_{convmin}}$.

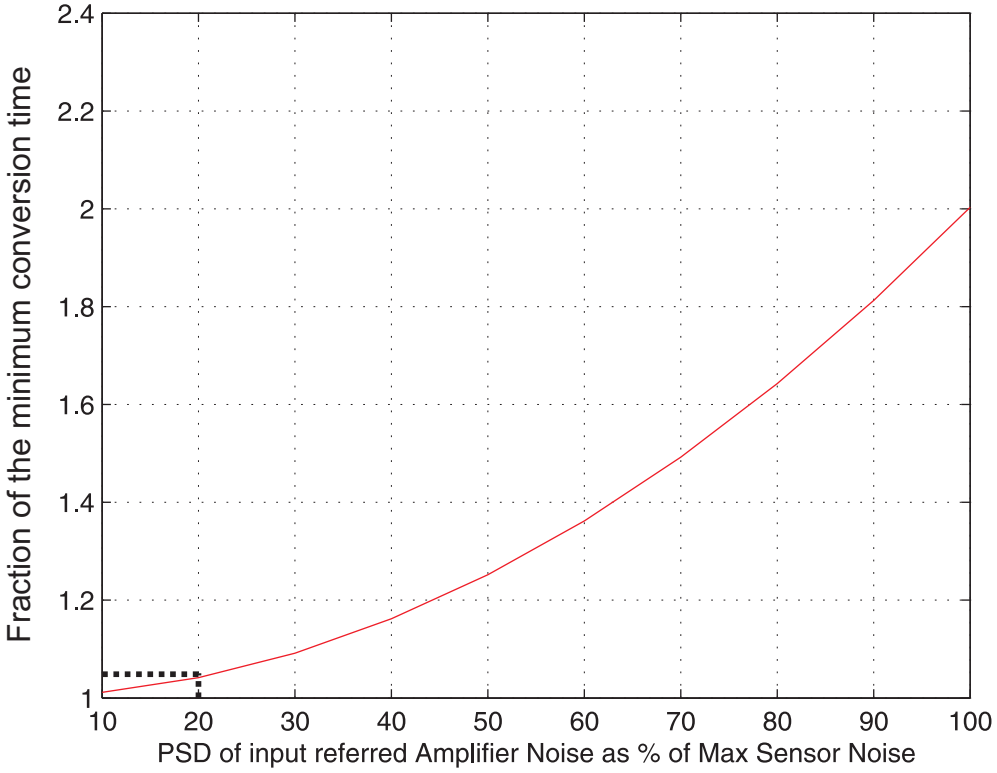

Figure 2.6: Increase in time as a function of Read-out Noise Contribution

We see in figure 2.6 that the increase in conversion time is less than 10% for an effective noise contribution of 20% by the read-out. We choose this as a reasonable estimate because an absolute increase of 20% in the photodiode noise only increases the total density by 2%, given by equation (2.5). Therefore the requirement from the circuit level implementation of the read-out is that the input referred noise is less than 20% of the total sensor noise, i.e. $0.2 * 126pA = 25.2pA$, thus increasing the conversion time required to $138\mu s$. This conversion time is three orders of magnitude lower than that required from the application(167ms). This optimization was targeted because any subsequent improvement in lasers (reduction in I_{tx}) can still re-use the read-out electronics in an energy-efficient manner, during subsequent iterations of the system.

2.4 Conclusion

The characteristics of the photodiode have been described. Based on this, various specifications for the CMOS chip sensor have been analyzed as well as a system architecture proposed. The derived specifications for the read-out are summarized in table 2.1.

Specification	Value	Units
Conversion Time for each sample	138	μs
Equivalent Bandwidth of sensor signal	3.623	kHz
Integrated sensor noise	126	pA
Desired integrated read-out noise	25.2	pA
Operation of photo-diode	Photovoltaic	-

Table 2.1: Photo-diode signal and noise characteristics

3

Analog-to-Digital converter architecture

We have discussed in the previous Chapter the sensor characteristics as well as the requirements for the read-out. In this Chapter we will evaluate different ADC architectures which satisfy these requirements. We motivate the use of a specific architecture and its features for our system. The ADC architecture will be modeled and simulated to verify the proposed solution. The various non-idealities will be included in the model to arrive at specifications for the circuit-level implementation.

3.1 Acquisition of the photodiode signal

The current from the photodiode can either be converted to the voltage domain before feeding to the ADC, as shown in figure 3.1(a), or the current can directly be acquired by the ADC, as shown in figure 3.1(b). The trans-impedance amplifier is an additional stage to the converter which makes the overall performance in terms of noise, input current dependent. In comparison, figure 3.1(b) forms a compact interface where the linearity and noise concerns are moved within the ADC loop. We therefore choose to directly interface the current output from the photodiode.

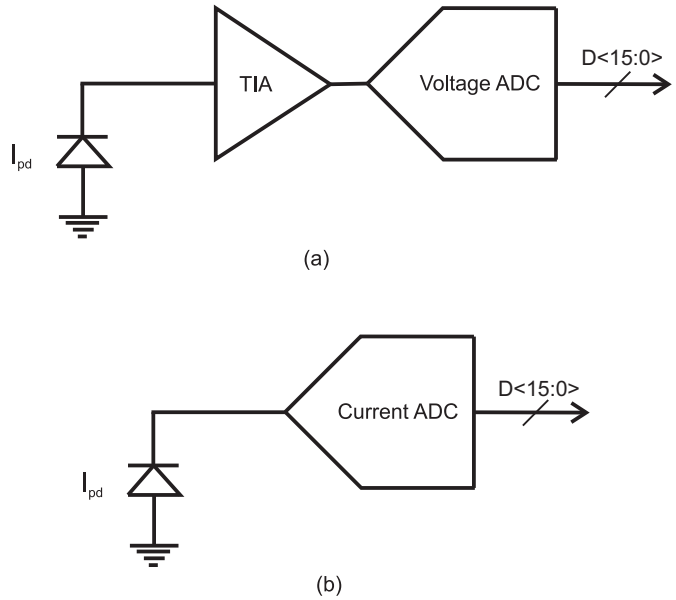

Figure 3.1: Front-end interface with the photo-diode

In the following sections, we will investigate the details of this architecture. The electrical model of the photodiode consists of a current source with a parasitic capacitance (120fF) and resistance (21,600Ω). The current output divides between the input impedance of the read-out and this parasitic shunt resistance. In a current-input ADC, an additional stage can be used for conveying the current from the sensor to the ADC with high efficiency. Efficiency refers to the percentage of current output from the sensor, that enters the ADC. One such method is the current mirroring direct injection (CMDI) [10] which provides close to zero input impedance by means of positive feedback and thus conveys most of the current to the ADC. But the drawback is the requirements for high linearity for this stage, as any mismatch results in an error in the signal being measured besides careful consideration to avoid the circuit to oscillate. Therefore we do not include such methods in our proposed architecture and instead implement a low input impedance front-end for the read-out.

In our design, we need a high resolution conversion (16 bits) for the photo-diode signal. Two well known techniques for achieving high resolution is using dual-slope and $\Sigma\Delta$ ADC architectures. The main motivation for the decision to choose $\Sigma\Delta$

architecture over dual-slope ADC is that the integrating capacitor required for the latter is large due to the dynamic range of the input signal. This can be intuitively understood because in a ΣΔ topology, the integration and feedback (deduction) is inter-weaved in time while in dual-slope there is a continuous integration for a certain period of time [11]. The feedback current balances out the input overtime in case of ΣΔ thus requiring a smaller integration capacitor compared to that of dual-slope.

3.2 ΣΔ modulator

ΣΔ modulators are suitable to realize ADCs which target medium-high resolution(> 16 bits) and can suit a wide range of bandwidth requirements. They are based on the principle of oversampling and shaping of quantization noise. In a ΣΔ modulator, the sampling f_s is done at a rate which is much higher than the Nyquist frequency $2f_B$; i.e. it is operated at an oversampling ratio of $(f_s/2f_B)$. As a result of this oversampling, the quantization noise is spread over a wider range of frequency, which reduces the effective PSD of noise. A loop filter shapes the noise away from the signal bandwidth which further reduces the integrated noise within the signal bandwidth, thus achieving a large SNR.

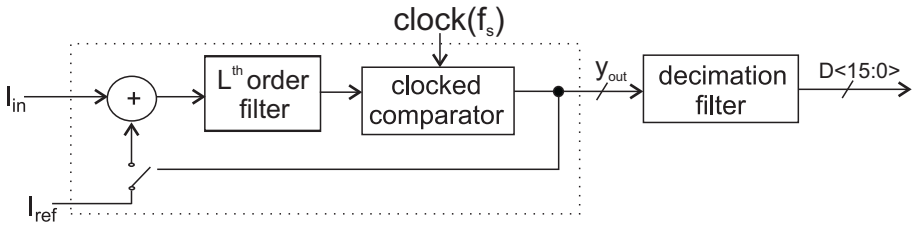

Figure 3.2: ΣΔ Converter followed by decimation

A simplified block diagram in figure 3.2 shows the general structure of a ΣΔ modulator with a L^{th} order filter. The over-sampled bit-stream (y_{out}) is decimated by a digital low-pass filter to get the final digital code ($D < 15 : 0 >$).

The dynamic range of an L^{th} order modulator with n bit quantizer and an over-

sampling ratio OSR can be obtained by [12]:

$$DR = 10 * log_{10}\left(\frac{3}{2}(2^n - 1)^2 \frac{(2L+1)OSR}{\pi^{2L}}\right) \tag{3.1}$$

We see that there are two knobs to improve the dynamic range: either by increasing the oversampling ratio (OSR) or the order of the shaping. Figure 3.3 shows the combined effect of varying the OSR and the order of the filter on the dynamic range of the ΣΔ modulator.

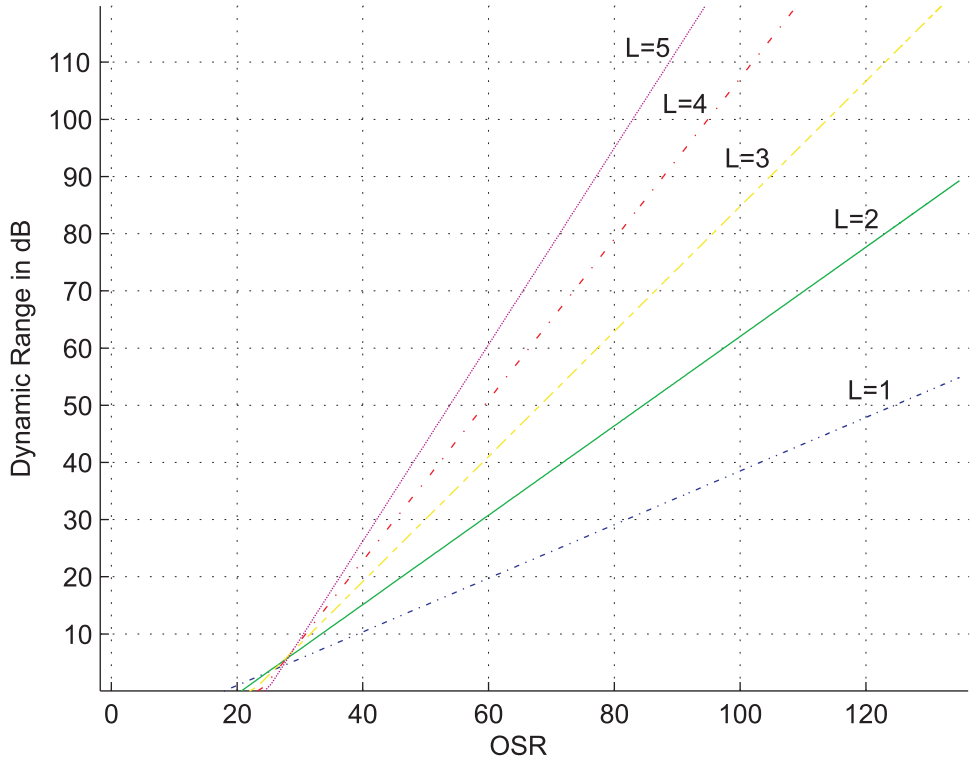

Figure 3.3: Relation between Dynamic Range and OSR of the ΣΔ modulator

In our design, we have an equivalent input signal bandwidth which is low. This allows us to use a large oversampling ratio and as a result we choose to use a single loop modulator topology. In a single loop topology, the analog power (which depends on the transconductance value) dominates the digital power (which depends on OSR choice) [13].

Our choice of order is motivated by two aspects. First, the desire not to make

the oversampling rate extremely high, and second to satisfy the system specification requirements. Choosing a first-order filter results in a very large OSR while choosing a third-order filter reduces the required OSR at the cost of design complexity, while both satisfy the specifications. We therefore choose a second-order modulator, which balances the factors discussed.

3.2.1 Incremental ΣΔ modulator

The application we target is for instrumentation, which does not require the modulator to operate continuously. Rather, it is operated for a finite conversion time T_{conv} which begins after resetting the ΣΔ modulator. The equivalent bandwidth of the input signal is decided by this conversion time and is given by $\frac{1}{2T_{conv}}$. This is also known as the one-shot operation or the incremental operation [14]. The performance revolves around static accuracy parameters such as linearity, gain and offset in such modulators. Henceforth in the thesis the term ΣΔ modulator implies that the modulator is operated in the incremental mode.

The first stage of the modulator consists of the integrator for the input current which can be either continuous or discrete time. One of the discrete time implementations is the switched-current (SI) integrator [15]. The other possibility is to integrate the current directly onto a capacitor in continuous mode. For our case, the implementation of a continuous-time integrator is simple for the first stage while also it provides inherent anti-aliasing filtering since the sampling happens after the integration [16]. Therefore, we choose a continuous-time incremental ΣΔ modulator and a second order single loop implementation as a possible architecture which satisfies our application. A generic block diagram is shown in figure (3.2).

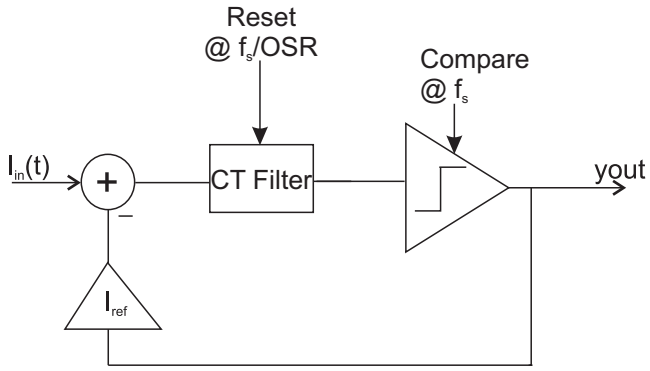

Figure 3.4: Block Diagram of continuous-time incremental ΣΔ modulator

3.3 Modeling of the continuous-time incremental ΣΔ modulator

We will derive a model for such an architecture. A second order Cascaded Integrator Feedback (CIFB) modulator is chosen for its simplicity as shown in figure 3.5.

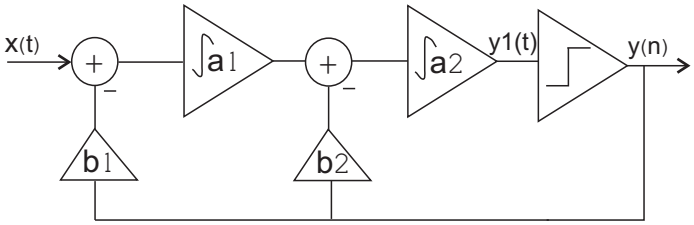

Figure 3.5: Cascaded Integrator Feedback Type ΣΔ modulator

The coefficients are chosen such that the integrator outputs are bound to ensure stability. In figure 3.6, we add a feed-forward path to decrease the output signal swing of the first integrator [17]. This reduces the output swing and slew requirements for the amplifier, thus lowering the power required.

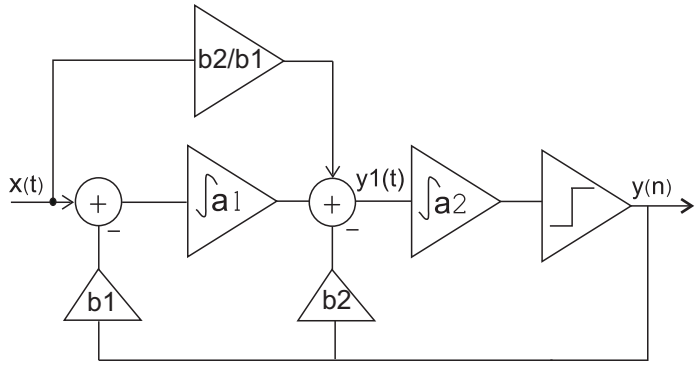

Figure 3.6: Second Order ΣΔ modulator with feedforward path

Referring to figure 3.6, we move the feed-forward path after the summation node. This helps remove the feedback DAC 'b2' at the second node which is shown in an equivalent structure in figure 3.7.

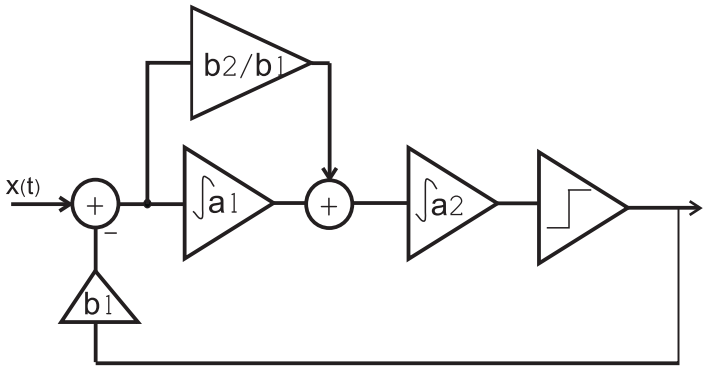

Figure 3.7: Modified Second Order ΣΔ modulator with feedforward path

We have derived the architecture in figure 3.7 for the modulator. We will now determine the required coefficients. The approach followed to find the coefficients of the architecture in figure 3.7 is to first find the Noise Transfer Function (NTF) for an equivalent discrete time implementation with the required resolution, order and OSR. Knowing these specifications and using the ΣΔ toolbox [16] we find the desired discrete time NTF as $\left(\frac{z-1}{z-1/3}\right)^2$. For the continuous-time model to give the same NTF, its impulse response should be same as that of the discrete time model. This is done by applying an impulse invariant transformation on the state space representation of continuous-time model and thus we arrive at the required normalized values of coefficients $a_1 = 0.444$ and $\frac{b_2}{b_1} = 1.33$. In our case the fed

back quantity is a reference current of value i_{ref}, therefore these coefficients (which were derived for normalized feedback) are suitably divided by magnitude(i_{ref})[18]. The choice of a_2 is decided by the maximum swing allowed for output of second integrator, since it is followed by non-linear element (comparator).

The resolution achieved by a second order incremental ΣΔ modulator is given [17] by equation (3.2)

$$n_{bit} = 2log_2N - log_2\left(\frac{2 * b2}{3 * b1 * a1}\right) \tag{3.2}$$

For this architecture, the theoretical oversampling ratio (N) required to achieve n_{bit}=16 bits resolution is approximately 363.

3.4 Decimation filter

In this section, we will determine the type of decimation filter for our specific case. For an L^{th} order incremental ΣΔ modulator, the order of decimation filter should be equal or greater than L to be able to effectively remove the noise from the output bit stream. Our design is a second order ΣΔ modulator so we will evaluate a $sinc^2$ and a $sinc^3$ decimation filter. The architecture of figure 3.7 has been simulated in Simulink together with these decimation filters to arrive at the required values for the length of these filters.

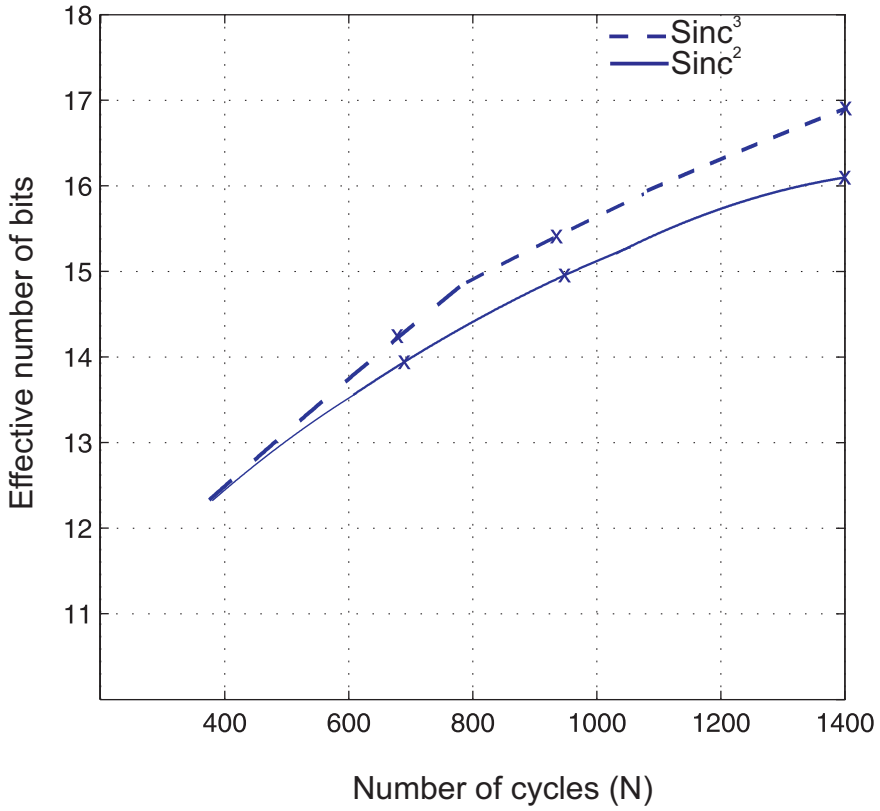

Figure 3.8: Effective number of bits for ΣΔ modulator obtained after decimation

We choose a length of 1400 for our case as it gives the required resolution using both triangular and sinc^3 filtering.

3.5 Inclusion of non-idealities in the ΣΔ architecture

A Simulink model of the ΣΔ modulator was implemented as shown in figure 3.9.

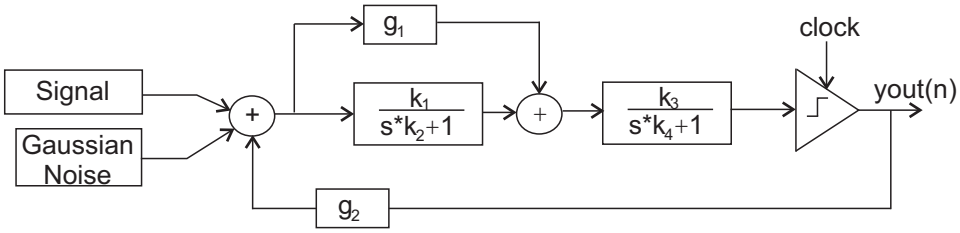

Figure 3.9: Model implemented in simulink for the proposed architecture

The various blocks used have been modeled with non-idealities. Consider the amplifiers which are used to implement the integrators in the ΣΔ modulator. These have a finite dc gain, bandwidth and slew rate. The limited gain moves the amplifier

pole to left of unit circle and hence reduces the benefit of shaping of the quantization noise which increases the in-band noise [11].

The finite dc gain of the integrator can be modeled as charge leakage in the integrator. Considering A_{01} as the dc gains of the amplifier, we can show that the leakage can be included by feeding back a part of the integrator's output as shown in figure 3.10.

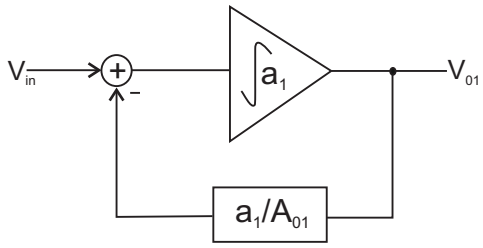

Figure 3.10: Model of finite gain integrator

For a 16-bit resolution, the loop has to be able to accurately balance the charge due to input current with that due to the feedback current over many cycles. For this to be ensured, there should be no charge loss and hence the gain provided by the cascade of integrators should be greater than $98dB$ to achieve 16 bit resolution.

For the amplifier of the first integrator, the relationship between the increase in quantization noise in the signal bandwidth, the oversampling ratio and the open loop dc gain is given by [19]

$$\frac{\Delta S_B}{S_B} = \frac{5}{\pi^4}\left(\frac{OSR}{A_o}\right)^4 + \frac{10}{3*\pi^2}(\frac{OSR}{A_o})^2 \tag{3.3}$$

This is plotted in figure 3.11.

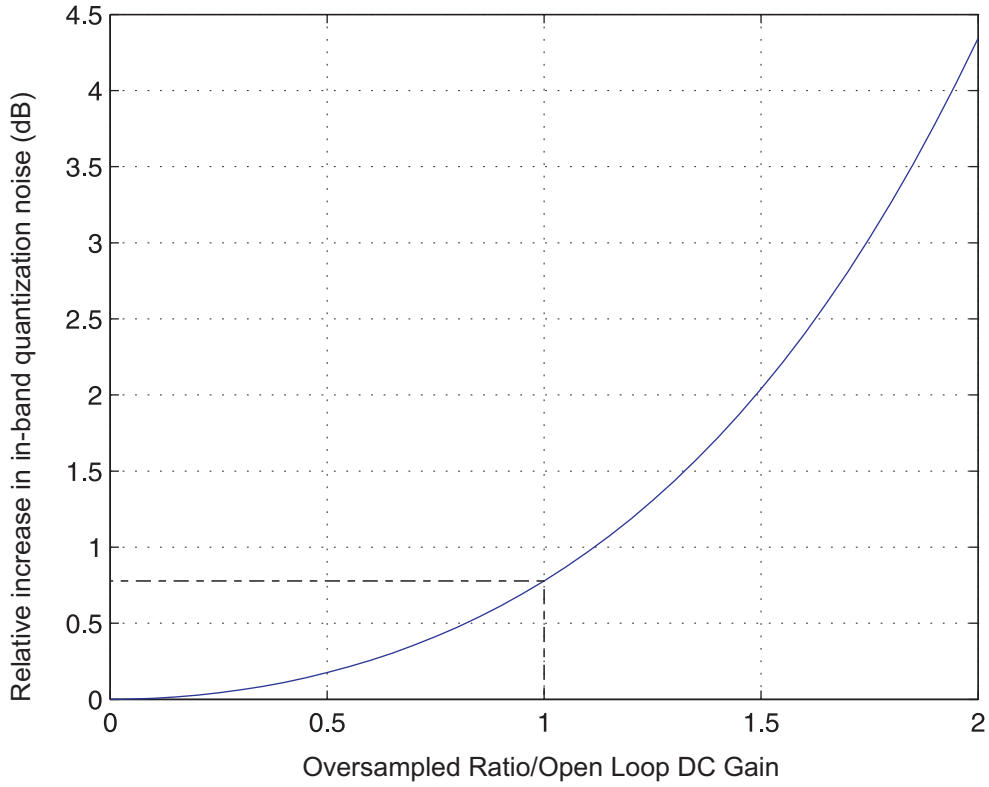

Figure 3.11: Effect of finite dc gain of amplifier on increase in noise

As seen in figure 3.11, this ratio should be smaller than 1 in order for the loss to be insignificant ($< 1dB$). Therefore the first amplifier needs a dc gain in the order of the OSR. Therefore in our case the minimum gain for the first amplifier is $20 * log_{10}(1400) = 63dB$ while the remaining 98-63=35 dB is required from the second stage so that the overall gain across the loop is equal to the targetted SNR of the modulator.

The modulator has been simulated with different dc gain settings for the first integrator and the bit stream has been decimated using triangular filter to find the resulting quantization error as shown in figure 3.12. We find that this validates our analytical derivation of the dc gain(>63dB) requirement for the first integrator.

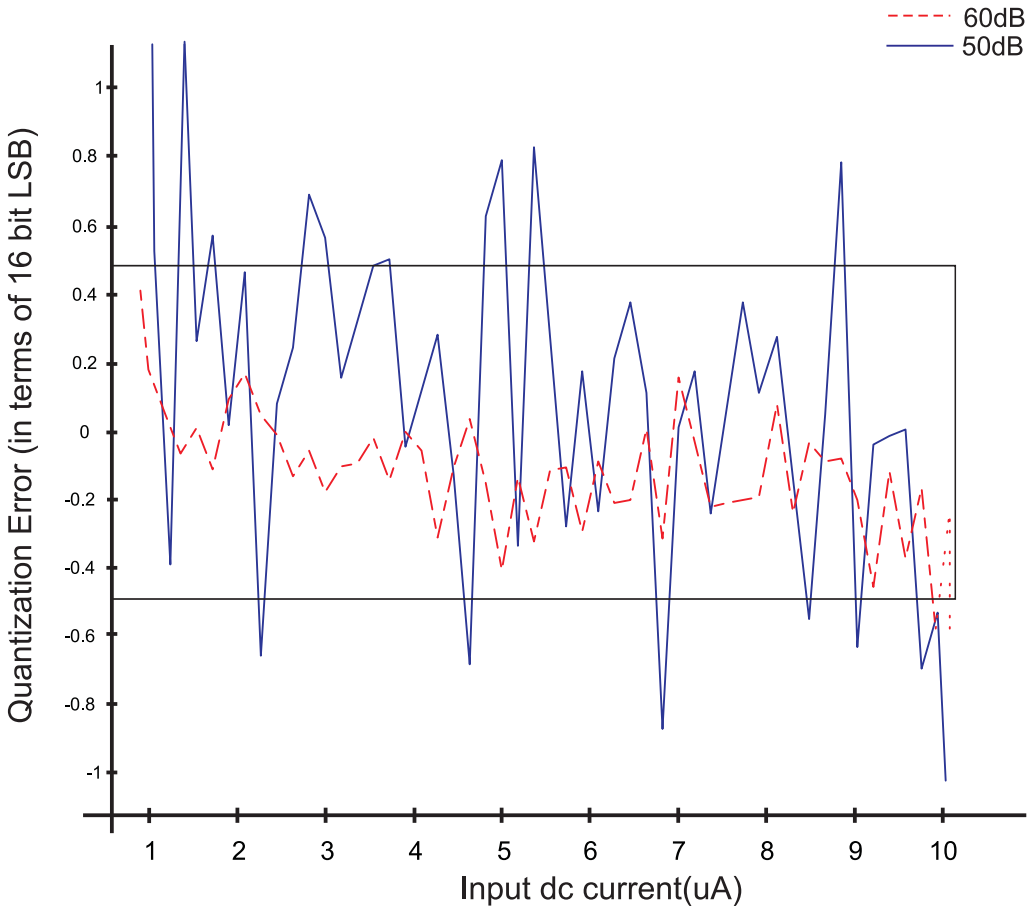

Figure 3.12: Effect of finite dc gain of amplifier on quantization error

It has been shown that a gain-bandwidth close to the sampling frequency of the modulator can be used if the settling is linear[19]. For our modulator, it has been shown in earlier sections that a conversion time of $138\mu s$ is needed and a decimation filter length of 1400 cycles are required. These together lead to a sampling frequency of 10.145MHz.

We can note that while there is a requirement on the bandwidth (>10.145MHz), the actual bandwidth given by g_m/C_L will be high, as the requirement on g_m is large due to the required low input impedance(discussed in section 4.1.1) while the internal load capacitance for the amplifier is low.

All these parameters derived for the various non-idealities have been included in the simulink model in figure 3.9. The resulting simulated bit-stream was decimated using sinc^2 and sinc^3 decimation filters to arrive at the quantization error plots as

shown in figure 3.13 and 3.14

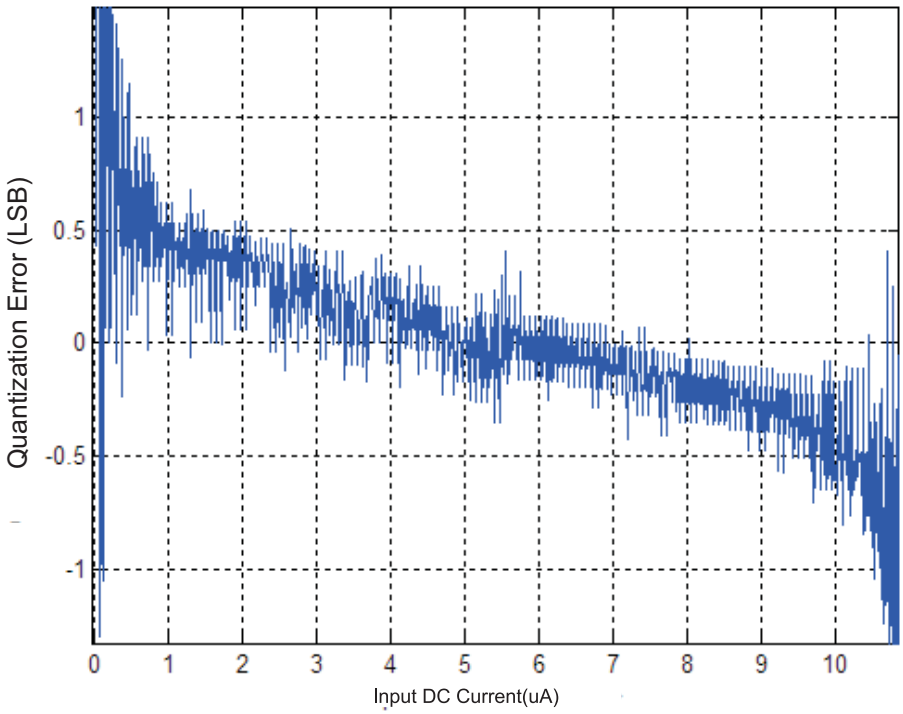

Figure 3.13: Quantization error result with $sinc^2$ Filtering

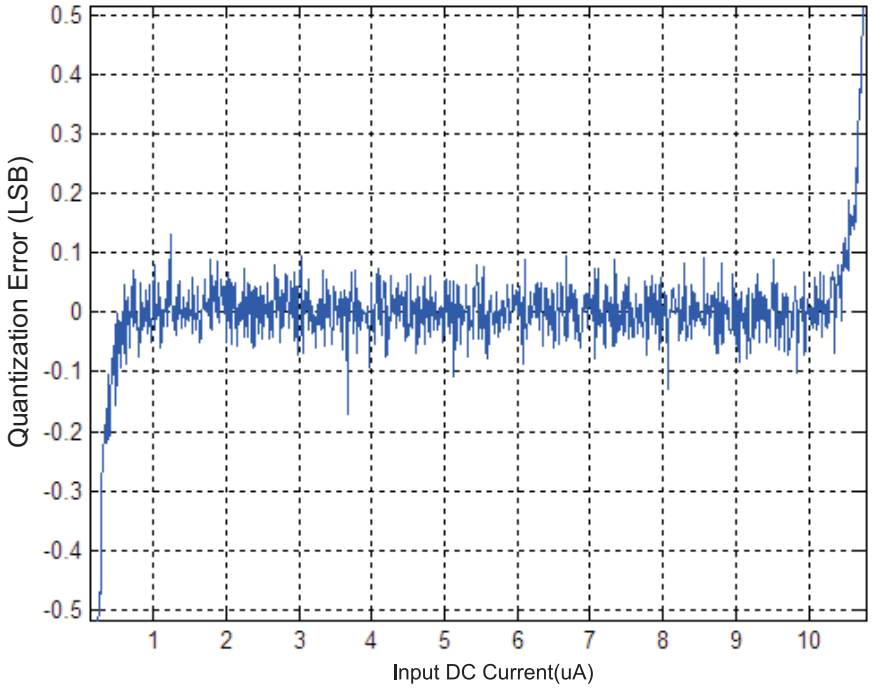

Figure 3.14: Quantization error result with $sinc^3$ Filtering

3.6 Dynamic selection of DAC reference

This section explains a technique proposed by us as addition to the final derived architecture in section 3.5 to improve the SNR across a wider dynamic range of input. The motivation for this comes from the fact that the actual input current is a wide dynamic range signal (100nA to 10μA) which in the present photodiode is reduced by the relatively large offset of 1μA associated with dark current. There is a continuous effort by the device group to bring down this value, which also reduces the associated shot noise, in future fabrication of the photodiodes. A reduction in dark current would result in a larger dynamic range of input-current than currently targeted and thus the performance of present implementation degrades. One simple way to overcome such reduction in dark current is to add a constant current of 1μA which brings the signal to the range for which the ADC was designed. An alternative technique we propose is to choose dynamically the feedback reference based on the input signal, thus bringing the input signal within the fraction of the reference current and improving the performance. This is illustrated in figure3.15. Another method in literature[20] involves determination of window (2 finer references inside the full scale) to improve dynamic range for voltage inputs. While [21] and [22] have used the concept of changing references for first order $\Sigma\Delta$ modulator. A literature search showed that there was a recently filed patent [23] in similar direction for photodiode interface circuits.

We include a mode in the $\Sigma\Delta$ modulator to dynamically selecting the reference currents depending on the input current range. As a proof of concept, we include four equal sub-divisions of $i_{ref} = 11.7\mu A$ in the feedback, whose selection is decided during the initial test cycles of operation before the actual start of conversion and remains fixed for that conversion. The number of conversion cycles (i.e. oversampling ratio) is kept the same in all cases.

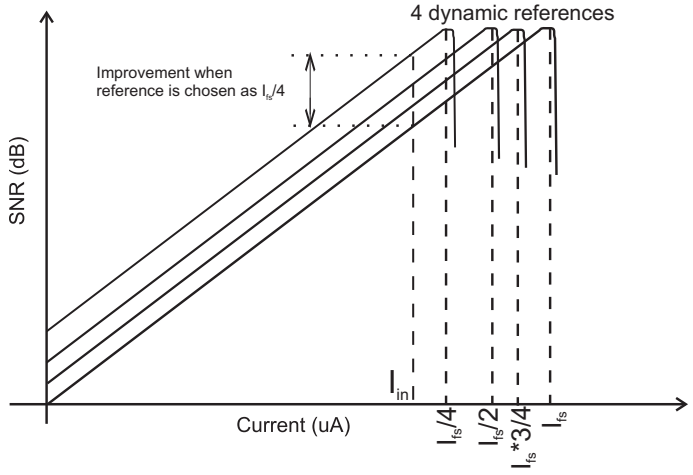

Figure 3.15: Concept of dynamic reference selection based on input

The maximum performance of the ΣΔ modulator occurs close to the corresponding reference current. In our implementation of a dynamic reference, the control to tune the reference DAC is based on the first 8 output bits when the reference DAC is completely ON (all switched closed). The counter (in an external micro-controller) gives us a coarse 2-bit code which then configures the reference (as one of four levels) via the SPI to control the four branches of the reference DAC.

It has to be noted here that figure 3.15 only shows improvement under the assumption that the total noise is dominated by quantization noise. In a thermal noise dominated system, the effect of choosing a closer reference to the input signal does not improve the SNR as the overall noise is largely dominated by thermal noise.

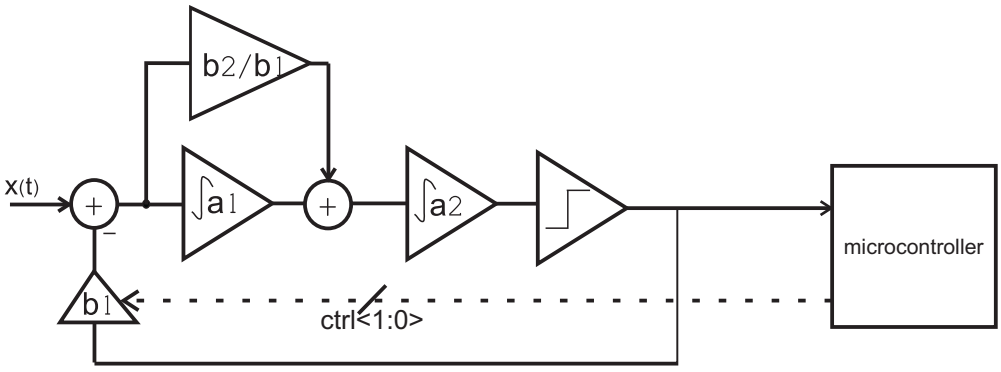

Figure 3.16: System level implementation for inclusion of dynamic reference

A simulation of the above method was done using the model in figure 3.16. During the first eight cycles of feeding the input signal, the bit-stream is decimated

(counter) in the microcontroller and the choice of reference determined. This is fixed by ctrl$< 1 : 0 >$ which sets the reference DAC current (b1) in the model. Figure 3.17 shows the improvement in the resulting quantization noise plot even at the lower range of input currents. We can see distinct four regions represented by the four different sized red boxes. We see that the quantization error improves when the reference level of feedback DAC is chosen closest to the input signal to be quantized.

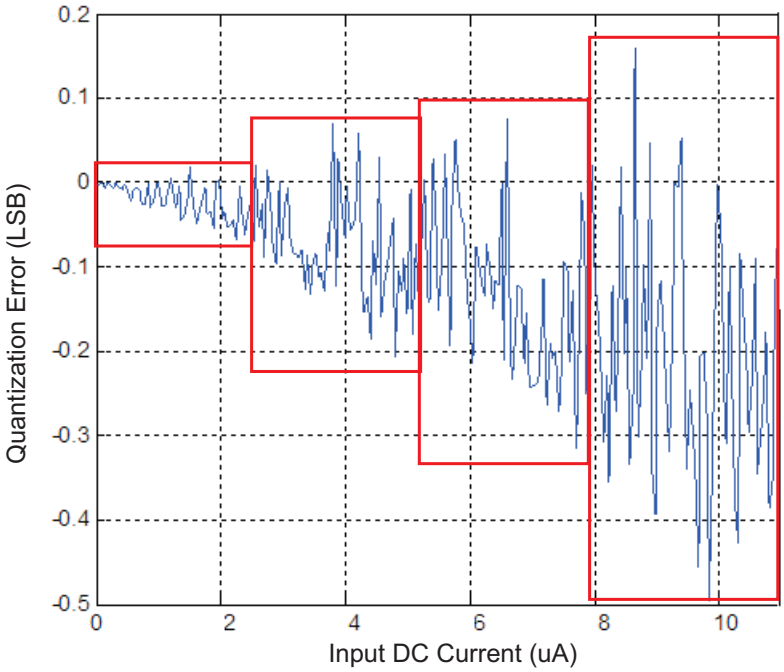

Figure 3.17: Performance improvement due to dynamic choice of references

Thus the functionality of the concept is verified by simulation as the performance now can be seen at lower current values. A zoomed plot in figure 3.18 shows that with the reference set to lowest value i.e. $\frac{fullscale}{4}$, the quantization error is within bounds up to tens of nA. Below the tens of nA input current, the amount of current required is much lower($<$1%) than this lowest reference.

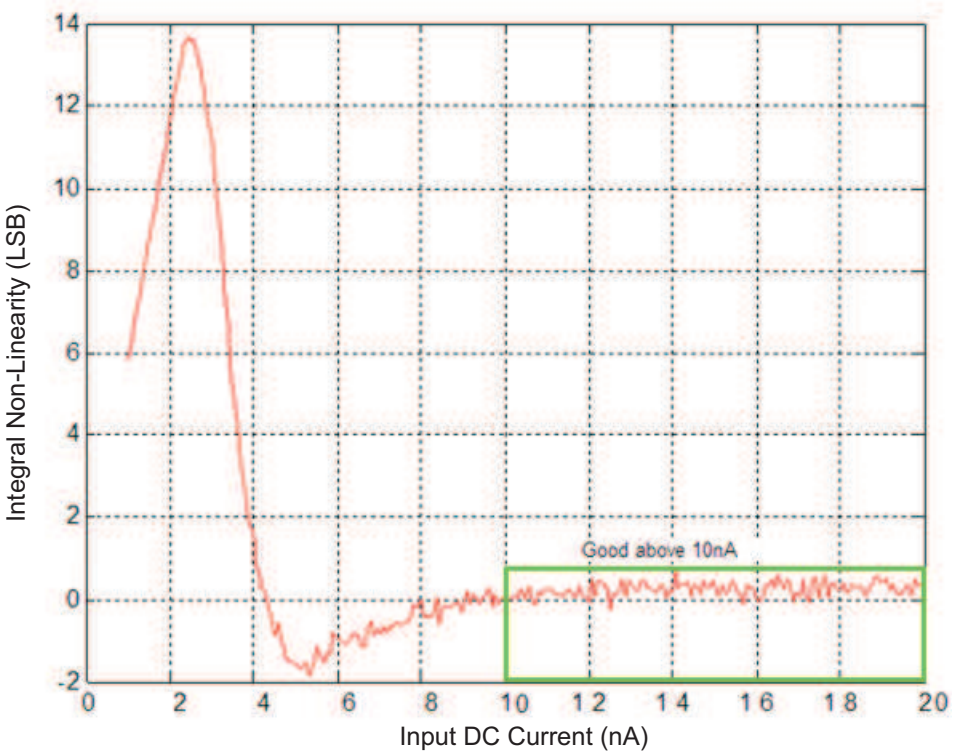

Figure 3.18: Improvement in performance at lower values of current input

3.7 Conclusion

The architecture of the second-order continuous-time incremental $\Sigma\Delta$ modulator that takes current input has been presented. The modulator has been simulated by including non-idealities associated with the circuit implementation to arrive at the required specifications for the circuit blocks. These specifications form the basis for our transistor level design in the next chapter and are presented in table 3.1.

Parameter	Specification	Units
Oversampling Ratio	1400	-
Reference Current	11.7	μA
Gain Bandwidth of the Amplifiers	> 12	MHz
DC Gain of the first OTA	> 63	dB
DC Gain of the second OTA	> 35	dB

Table 3.1: Architectural Specifications for the ADC Design

4

Circuit design of the ΣΔ modulator

This chapter focuses on the implementation of a current-input continuous-time incremental ΣΔ modulator based on the architecture and specifications described in Chapter 3. The transistor-level design of its building blocks is derived in terms of optimum noise, accuracy and power consumption from both circuit as well as system perspective.

As discussed in the architecture of the ΣΔ modulator the blocks to be designed consist of the first and second integrators, a comparator and a current DAC.

4.1 Design of the first integrator

The first integrator of the ΣΔ modulator is an important block as it is directly interfaced to the photodiode and also dominates the noise contribution from the read-out. Any subsequent noise contributions are attenuated by the gain of this integrator.

Let us dimension the passive elements required to implement the first integrator. Figure 4.1 shows a model of the first stage of the ΣΔ modulator, whose transfer function is given by

$$V_o(t) = \frac{a_1}{s} * i_{in}(t) + \frac{b_2}{b_1} * i_{in}(t) \tag{4.1}$$

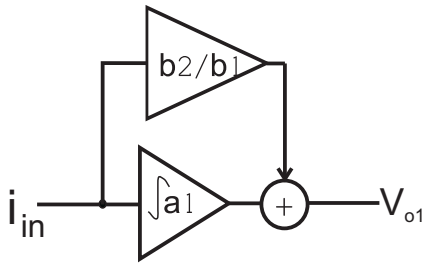

Figure 4.1: Model of the proportional plus integral stage for ΣΔ modulator

$i_{in}(t)$ is the current which is integrated.

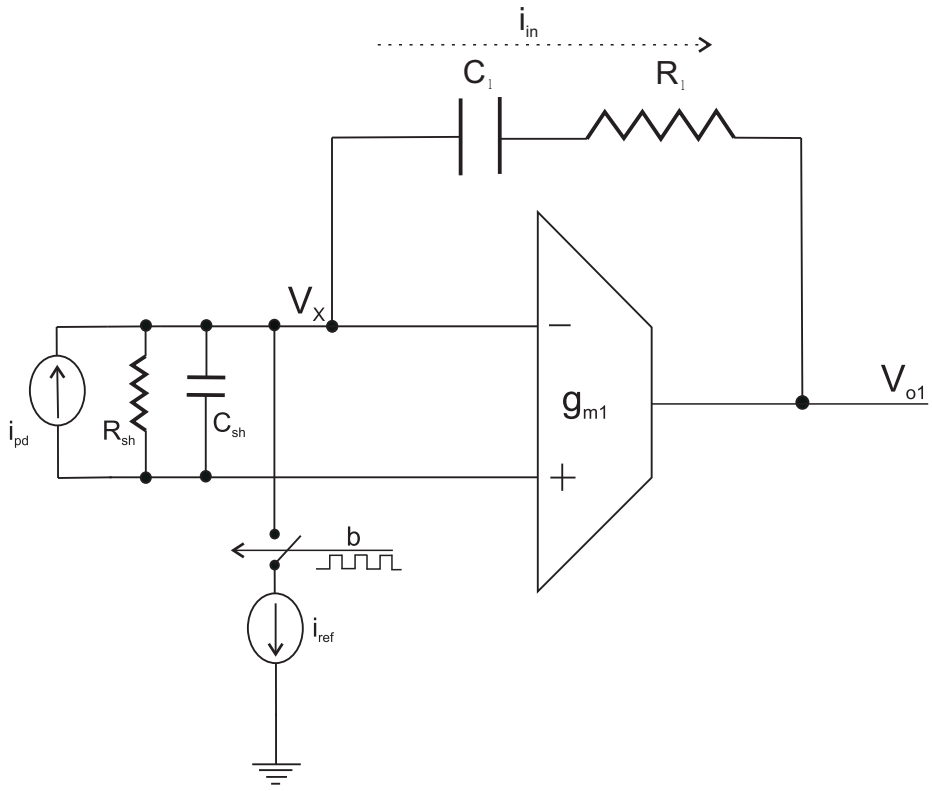

Figure 4.2: Realization of the first stage for ΣΔ modulator

An implementation of this first stage consists of a feedback capacitor and an additional series resistor to provide a feed forward path as shown in figure 4.2. The transconductor(g_m) is required to ensure that the bias voltage across the photodiode does not change.

The model of the photodiode is included in figure4.2. b refers to the modulator bit-stream which controls the fed back reference current. The photodiode output current and the fed back current undergo a current division and only a fraction(α)

passes into the modulator. Therefore (1-α)*($i_{pd} + b * i_{ref}$) flows through the shunt resistance(R_{sh}) while the rest α*($i_{pd} + b * i_{ref}$) flows into the integrator. The output voltage is given by

$$V_o(t) = \frac{1}{C_1} * \int i_{in}(t)dt + R_1 * i_{in}(t) \tag{4.2}$$

The choice of passive elements is done to match the transfer function of the first integrator.

$$V_{o1}(t) = V_o(t) * \frac{1}{10} \tag{4.3}$$

We use a scaling factor (1/10) which results in a moderate output swing(200 mV) requirement.It can be seen from Eq. (4.3) and Eq. (4.2) , that this swing reduction is at the cost of increasing the value of the capacitor while reducing the resistor value.

Comparing equation (4.1) and equation (4.2),we can relate the capacitance and resistance with their modeled co-efficients (a_1 and $\frac{b_2}{b_1}$) (see section 3). We arrive at the required capacitance from equation (4.4).

$$C_1 = \frac{1}{a_1 * f_s} \tag{4.4}$$

The coefficients a_1 and $\frac{b_2}{b_1}$ have the units of $[\frac{1}{F * Hz}]$ and [Ω] respectively.

where a_1 is $\frac{0.444}{magnitude(i_{ref}) * dfrac110}$ and $\frac{b_2}{b_1}$ is $\frac{1.33}{magnitude(i_{ref})}$ (the term magnitude is used to indicate that the coefficient's unit is same as that of a_1), while conversion time and the OSR together give us the sampling frequency f_s. This leads to

$$C_1 = \frac{T_{conv} * i_{ref}}{OSR * 0.444} / \frac{1}{10} = 25.9pF \tag{4.5}$$

Similarly the resistance is sized as

$$R_1 = \frac{b_2}{b_1} * \frac{1}{10} \tag{4.6}$$

where $\frac{b_2}{b_1}$ is $\frac{1.33}{magnitude(i_{ref})}$ [Ω] (see section 3).
This leads to

$$R_1 = 11.37k\Omega \tag{4.7}$$

4.1.1 Input impedance

The transconductance of the OTA is an important parameter as it determines the input referred noise as well as the input impedance of the OTA.The input impedance for the integrator is given by $R_{in} = \frac{1}{g_{m1}}$.The total current divides into two paths: the shunt resistance of the photo-diode and the input resistance as seen into the OTA. This division is shown in figure 4.3.The parasitic resistance of the photo-diode from characterization is approximately 21.6kΩ.

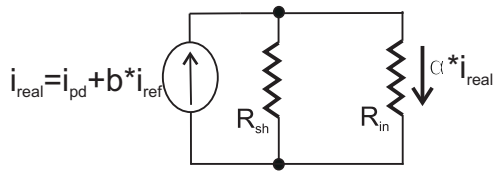

Figure 4.3: Model for current division between sensor and integrator

An important aspect of the current division between the parasitic resistance and the input impedance is that, due to the $\Sigma\Delta$ modulator architecture, the feedback current also undergoes the same division. Therefore the current division, to first order, does not affect the transfer function of the modulator as long as the fraction of current into the loop is considerable enough to provide the required resolution.

Let us find these boundary values next and decide on the final value of g_m. An ideal modulator loop was simulated in Spectre. Based on the different g_m values used for simulation of the first integrator, it was concluded that the current input into the modulator should be at least 85% of the total current to be able to convert the

analog current input with the required accuracy. This can be understood because the ADC assumes a defined minimum input range and the current division has to make sure it does not reduce the current into the ADC below certain level. This translates to minimum value of g_m (with the photodiode shunt impedance of 21.6kΩ) as 262μS derived from

$$\alpha = \frac{R_{sh}}{R_{sh} + (1/g_m)} = 0.85 \tag{4.8}$$

To accommodate for tolerances upto $\pm$ 20% in shunt resistance in equation (4.8) due to fabrication processes of photo-diode,we arrive at a minimum value of g_m of 325μS.

4.1.2 Noise

In Chapter 2 we have argued that, the noise contribution from the read-out circuit has to be below 20% of the total sensor noise integrated in the signal bandwidth.This translates to an increase in conversion time less than 10% resulting in a conversion time of 138μs. The main noise contributor in the $\Sigma\Delta$ converter is the first integrator. The contributions by subsequent stages are attenuated by the gain and hence do not significantly contribute to the overall noise floor. Let us understand the contribution of the g_m to the input-referred noise of the $\Sigma\Delta$ converter. We assume a differential pair provides the transconductance of g_m with output noise PSD of $4kT\gamma g_m\ A/\sqrt{Hz}$. The resulting input current PSD obtained from simulation as shown in figure 4.4. We find that a transconductance greater than 200μS is sufficient to keep the overall noise contribution of read-out below 20% (<26pA).

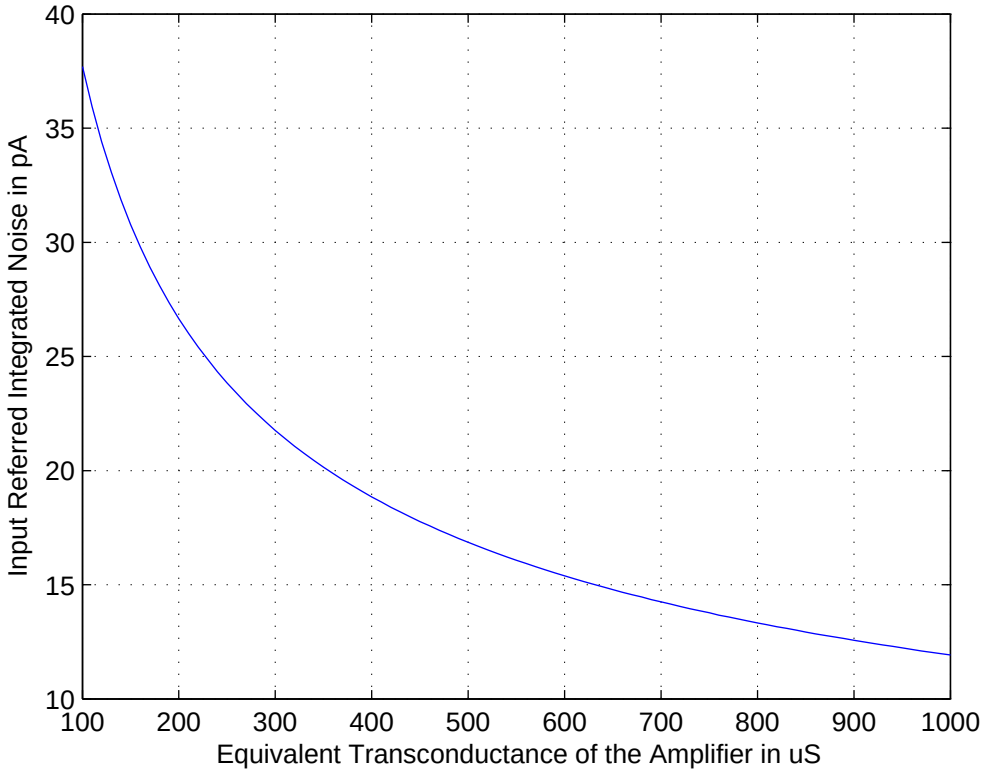

Figure 4.4: Transconductance required for various noise contribution from read-out

We find that a value of g_m >325μS satisfies both conditions discussed.

Table 4.1 summarizes the specifications required for the OTA and are derived from the model of $\Sigma\Delta$ modulator.

Parameter	Value	Units
Transconductance	>325	μS
Open Loop DC Gain	>63	dB
Unity Gain Bandwidth	>12	MHz

Table 4.1: Specifications for the OTA

4.1.3 Linearity

The transconductance should be approximately constant across the differential voltage developed at the input of OTA when integrating a given input current since any variation can change the amount of current input between cycles, affecting the performance of the modulator for that range of current. Without any additional techniques, a simple differential pair shows linearity upto $\sqrt{2} * V_{overdrive}$ which is

very low when operating the transistors in the sub-threshold region.

In our design, the maximum current to be integrated is $\pm 11.7\mu$A. The transconductor develops a differential voltage of $\frac{11.7\mu A}{g_m}$ at its input terminals and therefore its transconductance should be maintained for this range of input voltages. For a g_m of $325\mu S$, this translates to $\pm$ 36mV. We use a source degeneration R_{sd} to linearize the OTA and obtain a transconductance of

$$G_m = \frac{g_m}{1 + g_m R_{sd}} \tag{4.9}$$

Eq. (4.9) shows that for large $g_m R_{sd}$, the resulting transconductance depends only on the source degeneration resistance R_{sd}. In our design, degeneration resistor is chosen to be 1.5kΩ so that the resulting transconductance is greater than $325\mu S$.

$$g_m \approx \frac{2}{R_{sd}} \approx 335\mu S \tag{4.10}$$

4.1.4 Transistor-level implementation

Based on the requirements from the OTA specified in table 4.1, we find that a telescopic configuration will be an efficient implementation. The transistor level implementation is shown in figure 4.5.

The overall gain of the OTA is $g_{m2} * (g_{m4} r_{04} r_{02} || g_{m6} r_{06} r_{08})$. We have kept the transistors(M2, M3, M4, M5, M6, M7) in sub-threshold region in order to have a large g_m/I_D[24] while the load transistors(M1, M8, M9) are placed in saturation with large overdrive greater than 150-200mV for reducing the effective noise factor. We use a load capacitor of 2pF to limit the open-loop bandwidth to achieve good stability. Table 4.2 includes the sizing of the transistors used for the design. The implementation consumes $\approx 112\mu A$ from a $1.8V$ supply.

MOSFET	W(in μm)/L(in μm)
M1	48/0.5
M2,M3	80/0.18
M4,M5	28/0.5
M6,M7	40/0.5
M8,M9	10/0.5

Table 4.2: Sizing of MOSFET for the OTA

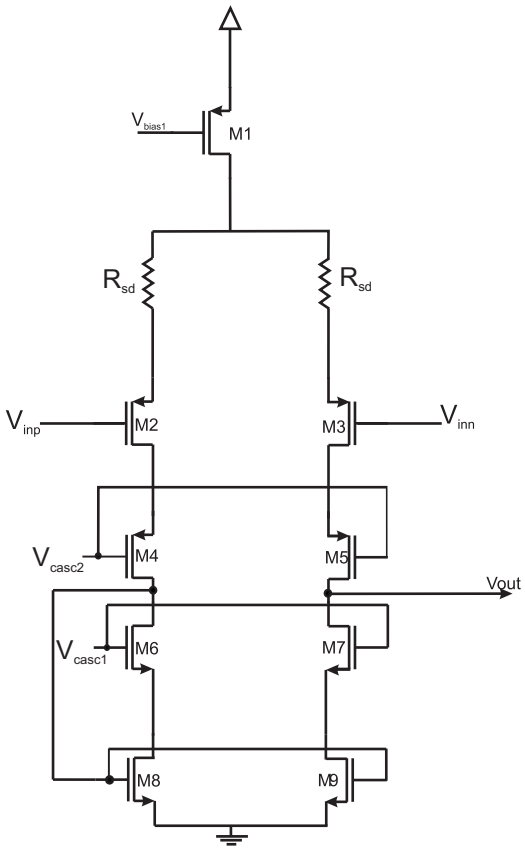

Figure 4.5: Telescopic Amplifier Design for the First Integrator

The simulation results have been included in table 4.3

Parameter	Specification	Simulation	Units
Transconductance	>325	350	μS
Open Loop DC Gain	>63	66	dB
Unity Gain Bandwidth	>12	24	MHz
Phase Margin	>60	80	degrees

Table 4.3: Simulation Results for OTA realization

For the ac simulation, feedback(β) of R_1,C_1 is used with the amplifier gain(A). Figure 4.6 shows a Bode plot of the open-loop gain with the gain and phase margin annotated.

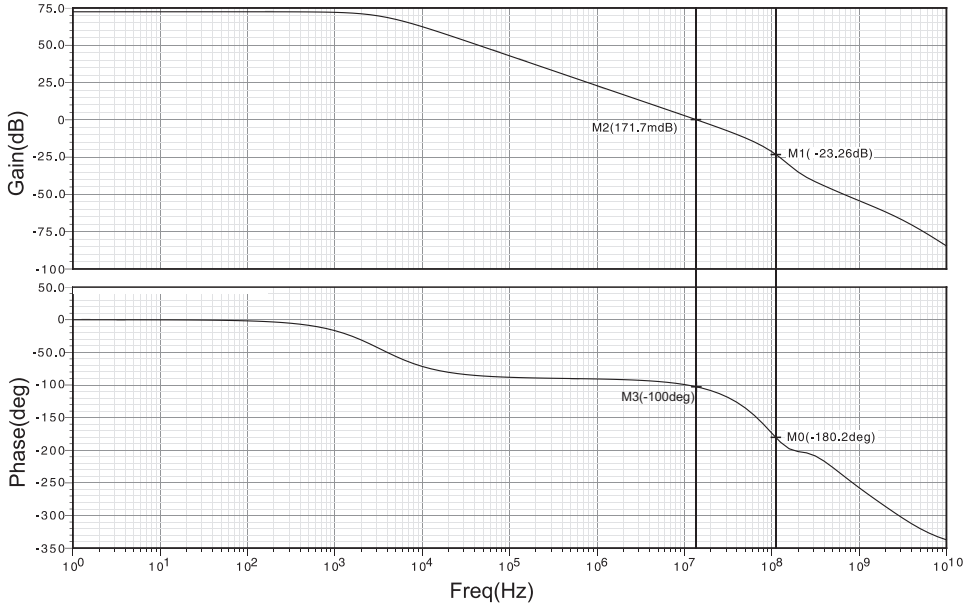

Figure 4.6: Stability Plot for the OTA

4.1.5 Chopping

From noise simulation of the OTA, we find that the dominant contribution to the total noise is the flicker noise(1/f) of the transistors as shown by figure 4.7, which was not taken into account in preceding noise analysis.

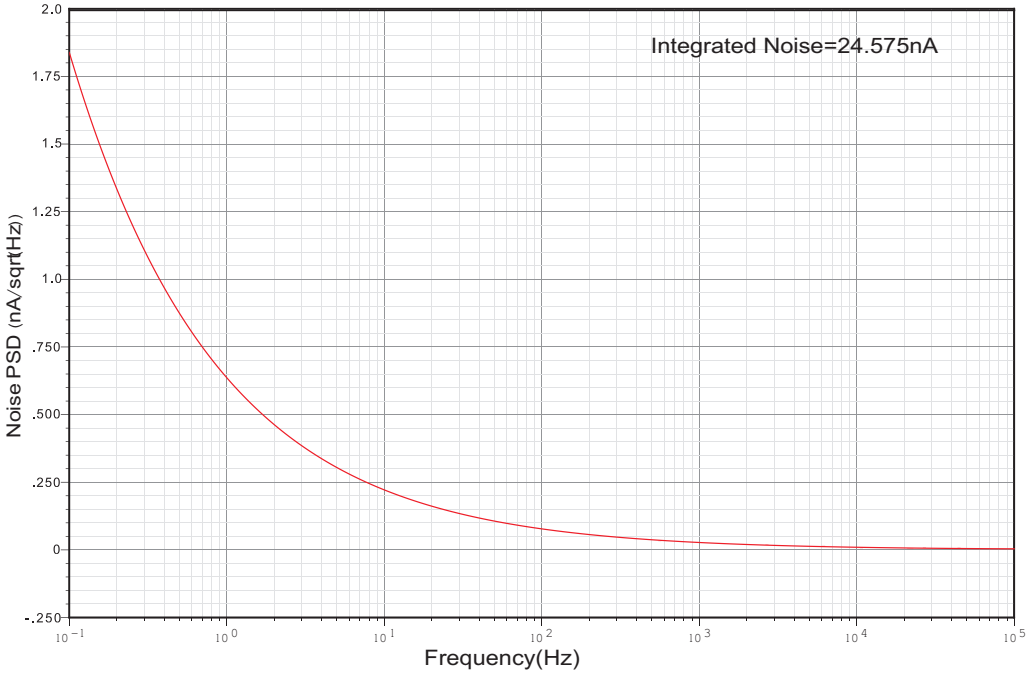

Figure 4.7: Input referred noise power spectral density of the first integrator

The total integrated noise in the signal bandwidth of $3.6kHz$ is $24.58nA$ which is much higher than the required $80pA$ from the system architecture derivation in Chapter 2. Therefore we remove the 1/f component by chopping [25].

The chopper is realized by cross-coupled switches which are controlled by opposite phase pulses as shown in figure 4.8. The clocks are realized to have no overlapping as shown in figure 4.8. The frequency of chopping (100kHz) is chosen such that it is higher than the 1/f corner frequency.

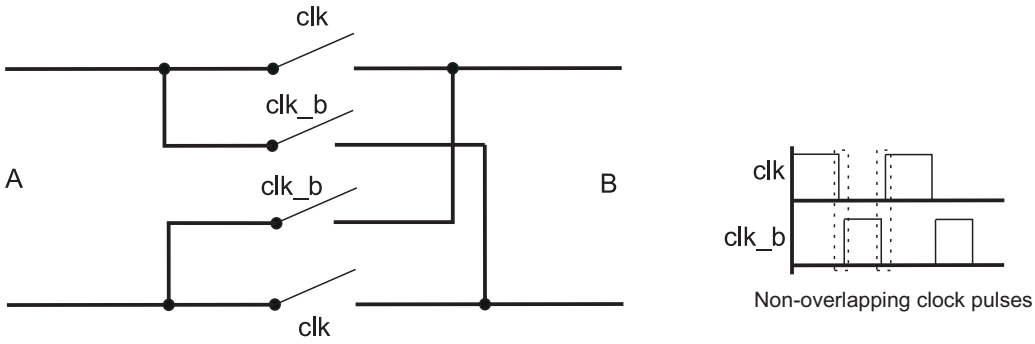

Figure 4.8: Chopper Switches Configuration

The OTA used in our design is a differential input single ended output amplifier. We therefore include a chopper switch configuration at the input terminals for modulating the voltage while at the output, the chopper is moved inside the OTA modulating the current output in each of the branches. The overall configuration of the OTA is shown in figure 4.9.

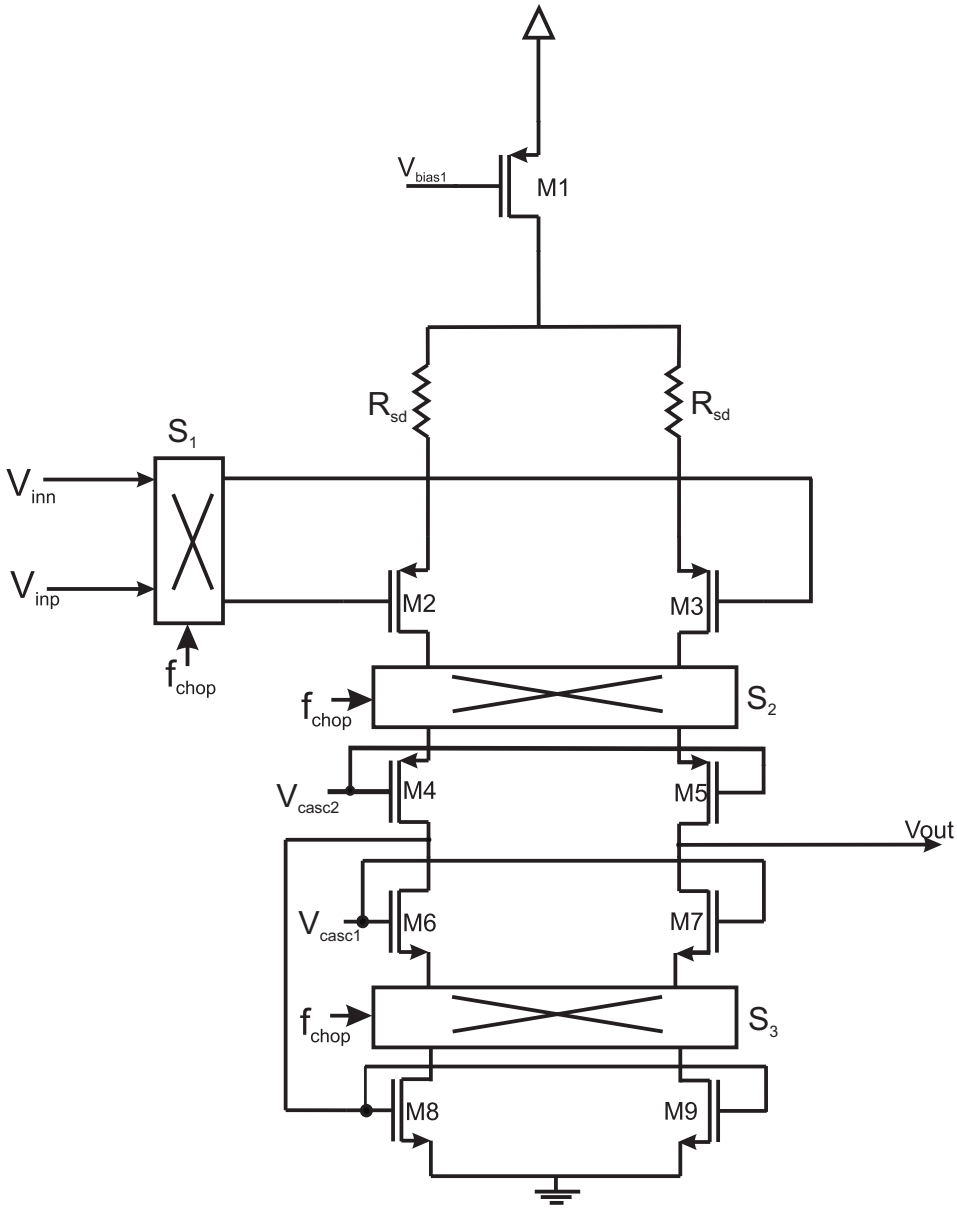

Figure 4.9: Chopper Inclusion into the OTA

Figure 4.10 shows the generation of non-overlapping clock pulses to the chopper amplifier.

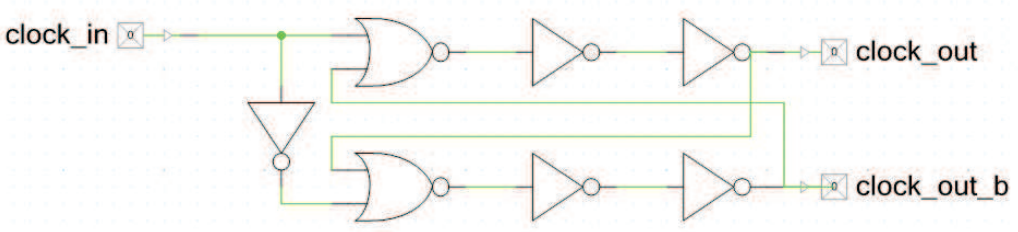

Figure 4.10: Non-Overlapping Clock Generation

The chopper switches S1 and S3 are implemented using NMOS transistors while S2 is implemented using PMOS transistors. The sizing of the switches is given in table 4.4.

Switch	W(in μm)/L(in μm)
PMOS	10/0.18
NMOS	6/0.18

Table 4.4: Sizing of Switches for Chopper

Using a periodic steady state analysis the input noise PSD was plotted after inclusion of chopper as shown in figure 4.11. The overall integrated noise is now reduced to $80pA$ as can be seen in figure 4.12.

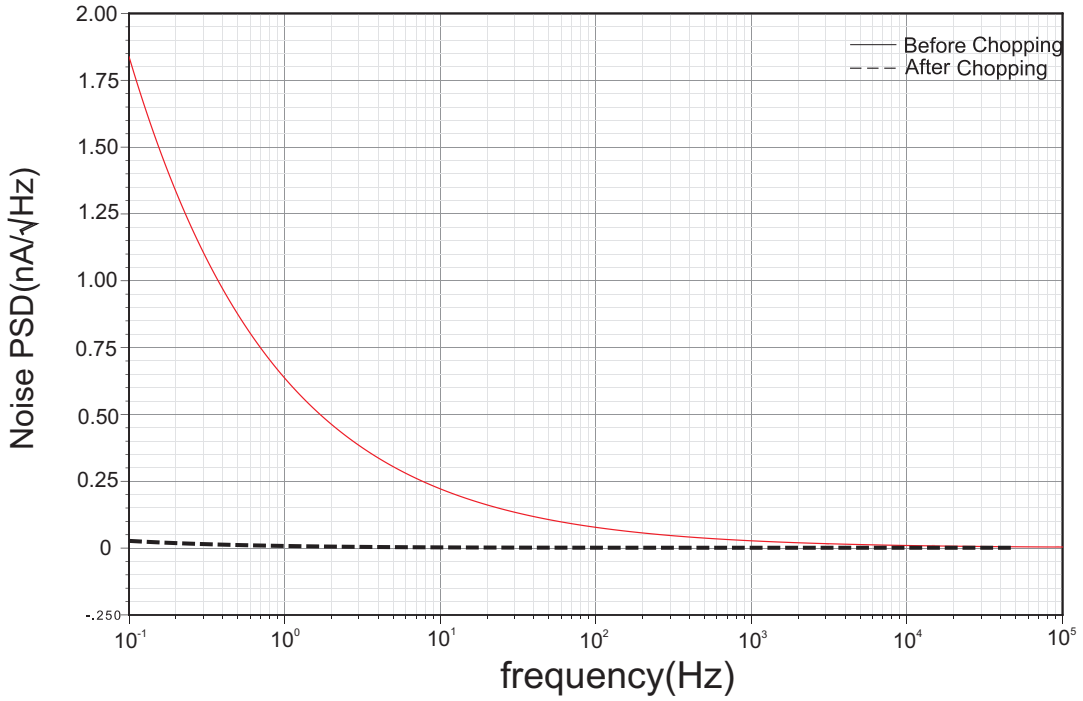

Figure 4.11: Comparison of noise PSD before and after chopping

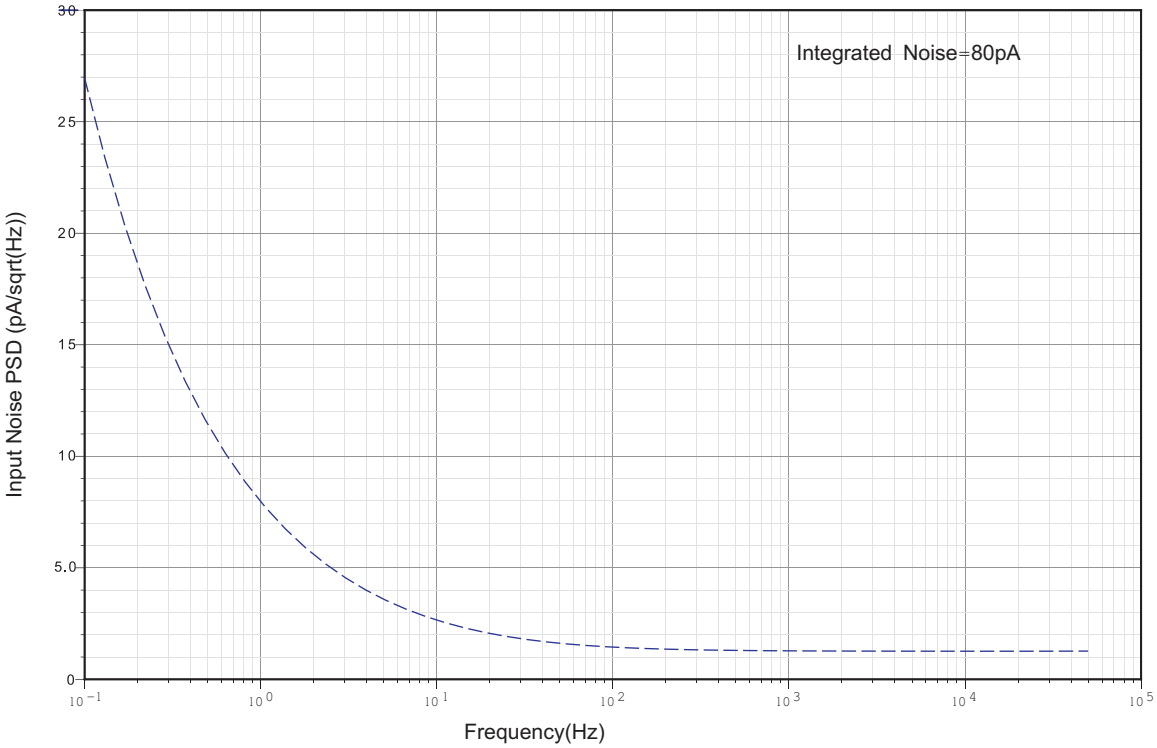

Figure 4.12: Input Noise PSD of the Chopped Integrator

The total current noise is given by Eq. (4.11) consisting of amplifier contribution as well as the sensor as shown in figure 4.13.

$$i_{ntotal} = \sqrt{i_{nsensor}^2 + i_{nreadout}^2}[A/\sqrt{Hz}] \tag{4.11}$$

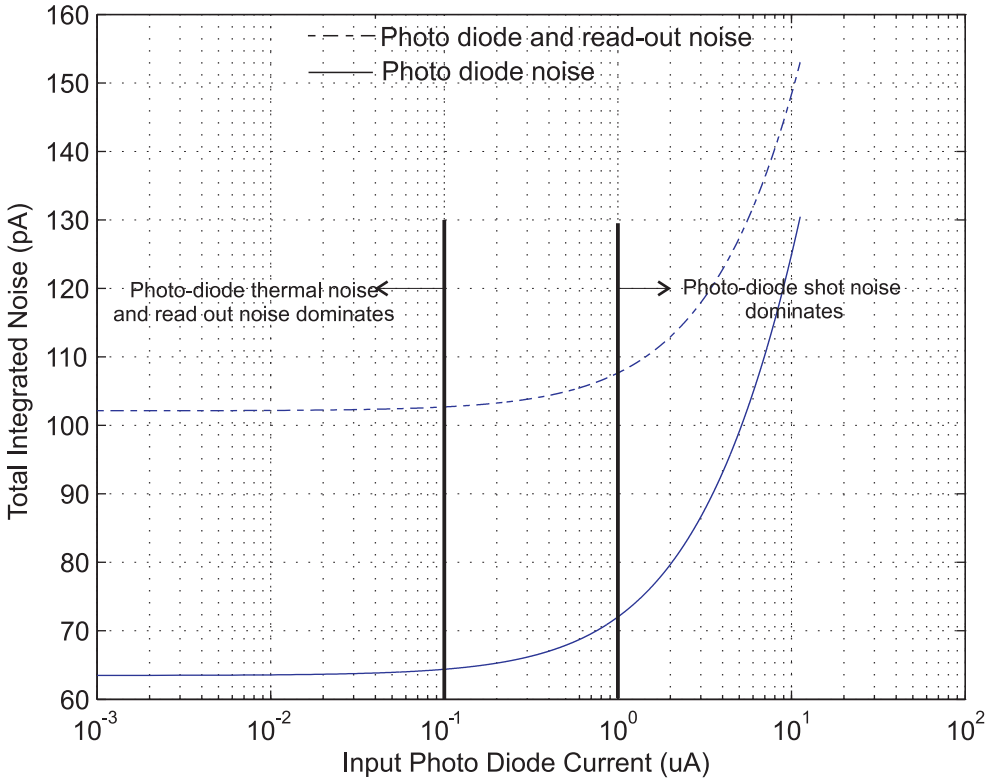

Figure 4.13: Total Input Referred Integral Noise

We find different contributions dominating depending on the magnitude of the input current. Between $1\mu A$ to $11\mu A$, the total noise is dominated by the photodiode shot noise.

We have arrived in Chapter 3 at a conversion time of $138\mu s$. With this conversion time for integration of the noise and signal, the resulting achievable SNR is shown in figure 4.14.

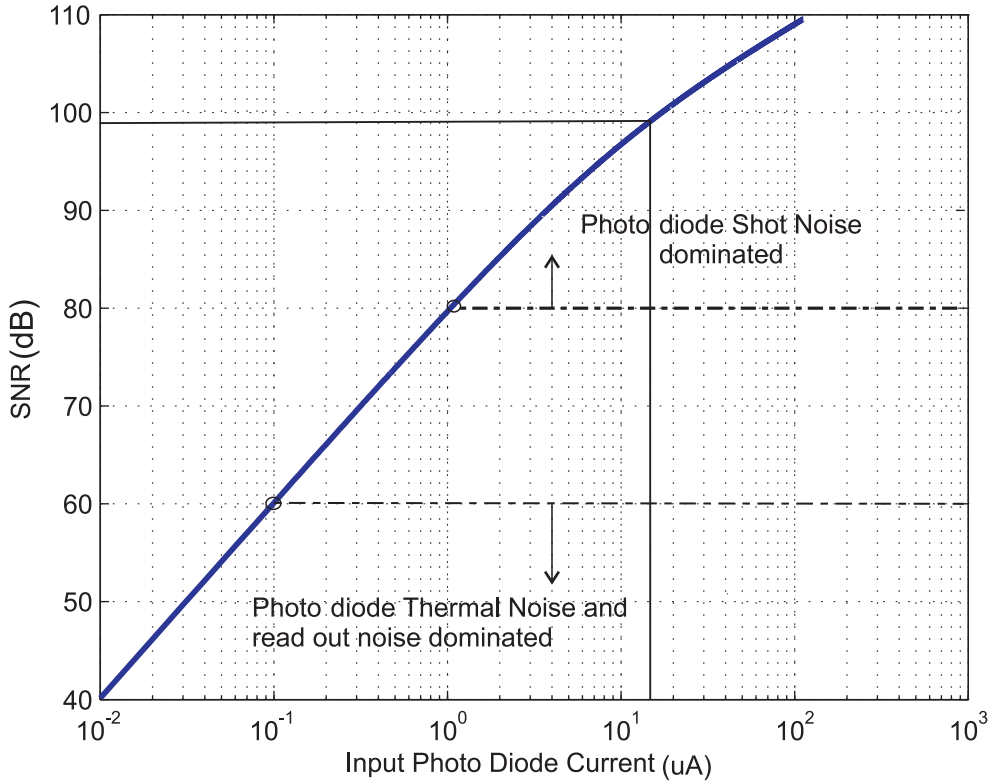

Figure 4.14: SNR for various input current signal

We see that the SNR is 98dB at the maximum input signal and decreases for the lower range of inputs. The 98dB target specification is for the full-scale range of input, which translates to approximately 78dB for one decade lower current input signal. The required SNR is also satisfied at the lower end of signal values where we see a 80dB SNR for input signal of $1.1\mu A$.

4.1.6 Sensor-adaptable biasing

In the overall ADC implementation the total power consumption is dominated by first integrator and in turn by the OTA. We have discussed that a major factor for our choice of transconductance is based on the shunt resistance of the photo-diode, which is dependent on the fabrication process of the devices. Therefore to provide an efficient interface for various resulting fabricated photo-diodes (as well as some commercial photodiodes), we include a switchable tail current biasing for the OTA.

As a proof of this concept, we have included two tail-current by means of switches

as shown in figure4.15. The transistor sizes for the telescopic stage are chosen so as to keep them in their respective bias region for the tail currents between these two boundaries.

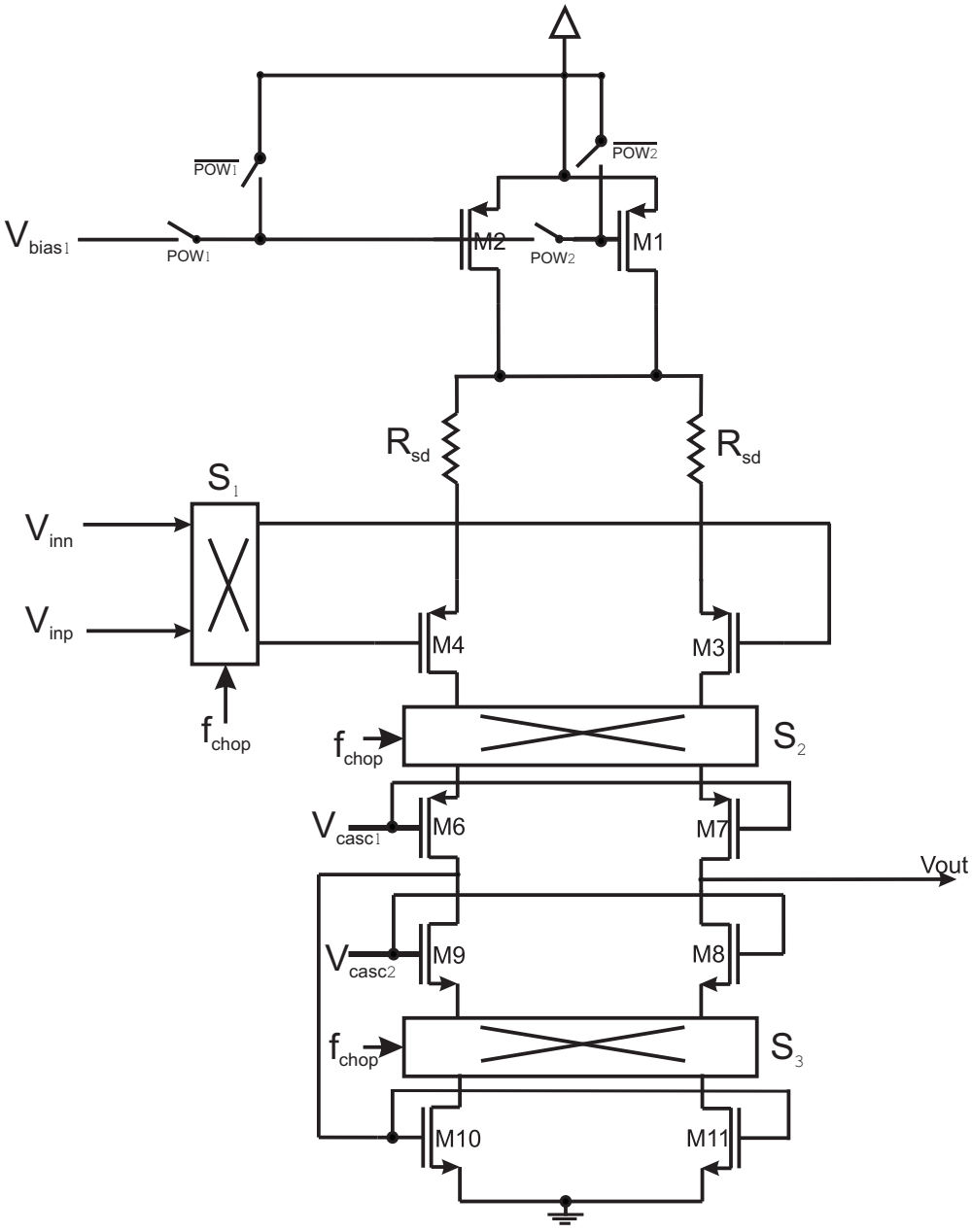

Figure 4.15: Modified OTA for realizing sensor adaptable front-end

The simulated performance of the OTA in the two modes is shown in table 4.5.

Specification	Mode1	Mode2	Units
Transconductance	350	200	μS
DC Gain	66	72.4	dB
Bandwidth	24	14.5	MHz
Power	201	50.4	μW

Table 4.5: Performance of the OTA in the two modes

Figures 4.16 and 4.17 shows Bode plots of the open-loop gain with the gain and phase margins annotated.

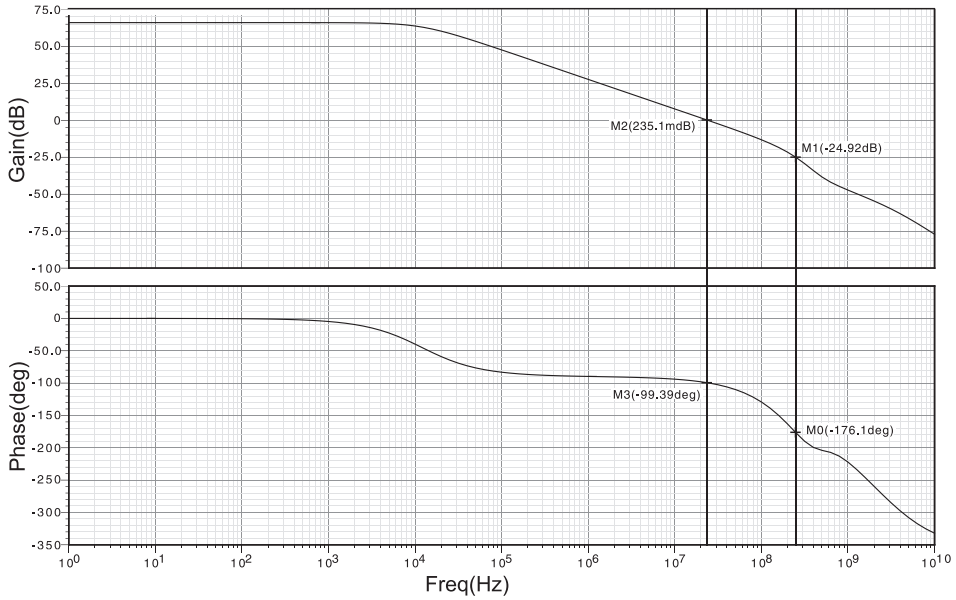

Figure 4.16: Stability Plot for the OTA in the Mode1

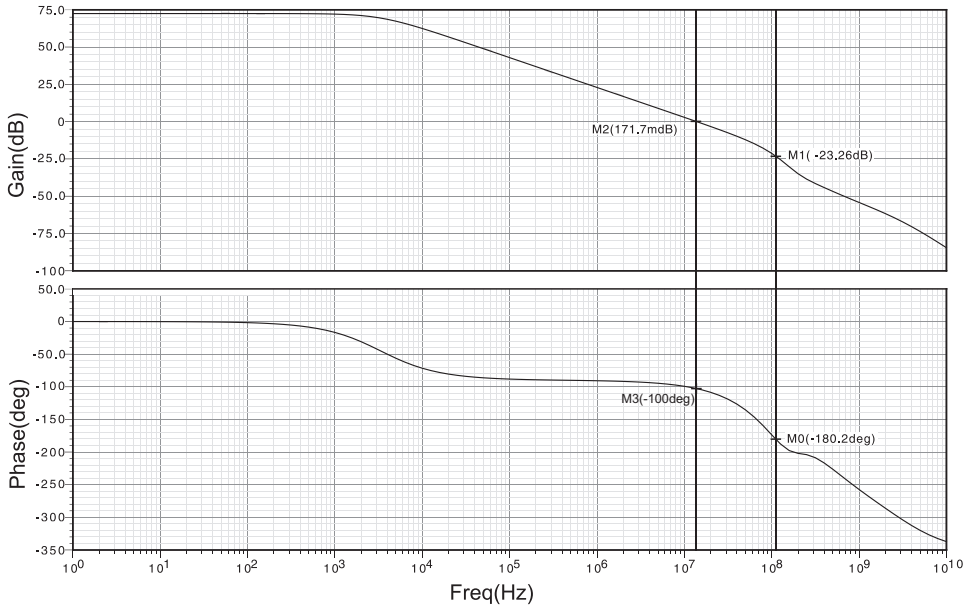

Figure 4.17: Stability Plot for the OTA in the Mode2

4.2 Design of the second integrator

The output of the first integrator is a voltage that needs to be integrated to provide the necessary second order function. There are different ways to implement this, such as by means of an active RC integrator, switched-capacitor integrator or a g_mC integrator. In our design, since the first integrator is implemented around a single-stage OTA, we cannot afford to have a resistive load, as this would affect the dc-gain of the first OTA. Therefore we choose a g_mC topology for our second integrator.

Let us first find the required specifications to achieve the transfer function based on the architecture derived in Chapter 3.

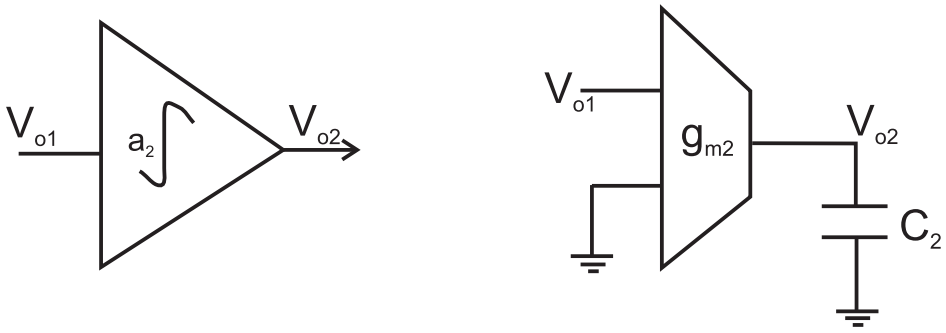

Figure 4.18: Mapping of Transfer Function for second integrator

Figure 4.18 shows the electrical realization and the equivalent component values can be found by equation:

$$V_{o2} = a_2 * \int V_{o1}\mathrm{d}t = \frac{g_{m2}}{C_2} * \int V_{o1}\mathrm{d}t \tag{4.12}$$

It should be noted that in first integrator design, a 10% output swing of the actual node voltage was chosen to relax the requirements for the OTA. Therefore to keep the same transfer function, we will include a factor 10 in the conversion equation.

Based on Eq. (4.12),we find that the components can be found as $\frac{g_{m2}}{C_2} = 10 * \frac{OSR * a_2}{T_{conv}}$. We had chosen a_2 as 1 in section 3 since it is followed by comparator. Choosing a nominal capacitance of 1pF results in a transconductance of $100\mu S$.

Since the amplifier is within the loop, any non-idealities such as linearity and offset will be shaped similar to the quantization noise based on the noise transfer function of the $\Sigma\Delta$ modulator. We find that the unity-gain frequency ($\frac{g_{m2}}{C_2}$) of the integrator is much greater than the loop bandwidth of the modulator($f_s = 10.14MHz$).
With the above specifications, a simple differential pair OTA topology satisfies the requirements of the g_m with tail of $7\mu A$. Figure 4.19 shows the implementation while table 4.6 shows the sizing of the transistors. This implementation provides us a transconductance of 105μS.

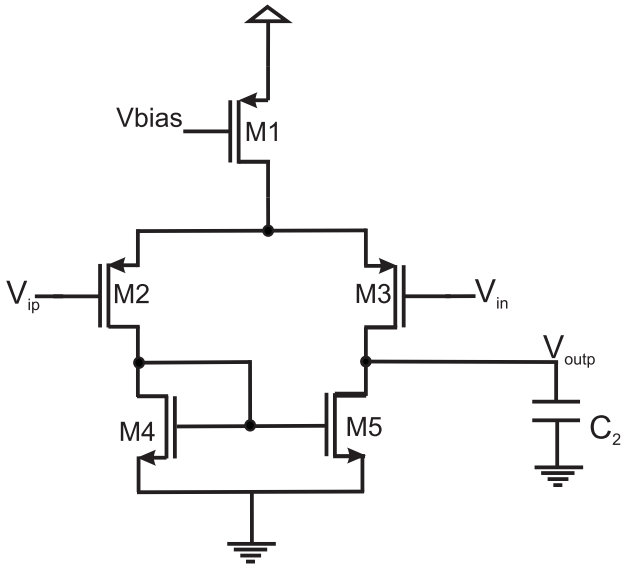

Figure 4.19: Implementation of the g_mC integrator

Transistor	W(in μm)/L(in μm)
M1	2/4
M2,M3	1/0.18
M4,M5	1/4

Table 4.6: Sizing of transistors for the transconductance amplifier

4.3 Design of the comparator

The second integrator is followed by a comparator. The modulator is continuous time until this point where the signal is sampled at a certain frequency and the digital output bitstream controls the feedback DAC.

The design concerns for a comparator in any ADC design are the speed, which

should be sufficient for the sample rate of the ADC, the input offset, which refers to the minimum input voltage difference which can be resolved within a certain time, the input-referred noise, and hysteresis. However in a $\Sigma\Delta$ modulator, offset and noise of the comparator traverse in the same path as that of quantization noise. Thus they are filtered by the Noise Transfer Function(NTF). It can also be shown that hysteresis of upto 10% does not change the in-band noise of the $\Sigma\Delta$ modulator[19].

There are many possible implementations for the comparator. One common method involves a pre-amplifier followed by a latch [26]. The pre-amplifier is a low gain stage which provides a reasonable output voltage. The main advantage of this stage is to prevent kickback, i.e. to reduce the charge injection into the preceding stage when the operation mode changes from tracking phase to latching phase. Without the pre-amplifier such kickback results in glitches at the input.

The combination of a pre-amplifier and a latch can be realized by a single tail-current source with stacked transistors to realize the two stages. The problem with such an implementation, however is the reduced swing available due to the large number of stacked transistors. Moreover, the offset and speed in such a design depends on the common mode voltage [27]. A method to make offset and speed independent requires different tail current sources, where the offset requires low current while speed requires large current. This is achieved by a double-tail approach as was shown in [28]. We choose this architecture for our comparator. The implementation is shown in figure 4.20.

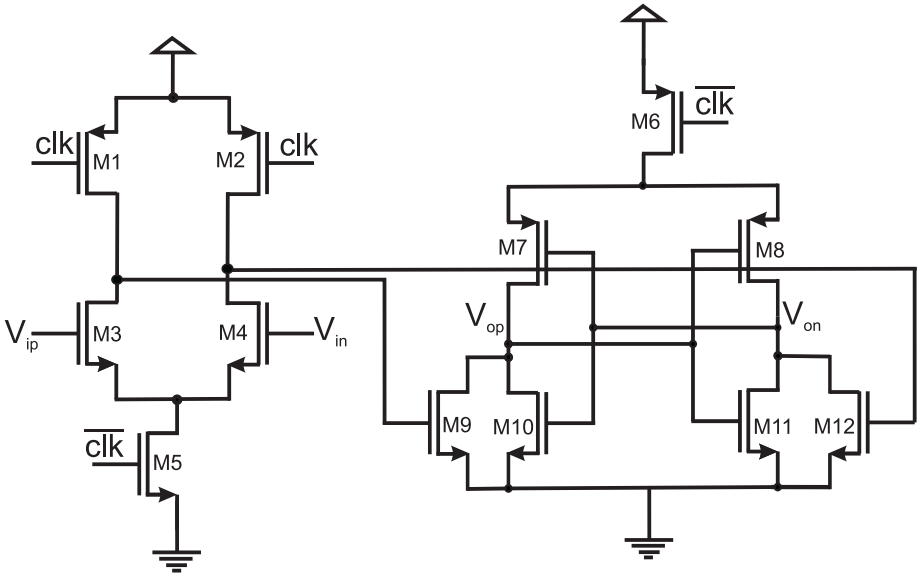

Figure 4.20: Implementation of the Comparator

The sizing of the transistors is such that the current in the pre-amplifier is low to decrease the input offset while the current in the latching structure is high so that regeneration is quick. The sizing of the various transistors is indicated in table 4.7.

Transistor	W(in μm)Ł(in μm)
M1,M2	0.5/0.18
M3,M4	3.75/0.18
M5,M9,M10,M11,M12	1/0.18
M7,M8	2/0.18
M6	10/0.18

Table 4.7: Sizing of transistors in the comparator

The architecture of the comparator [28] is such that the decision is available during the first half of the period while during second half the output node is reset to remove hysteresis. In order for the delay in output decision to DAC not be comparator input dependent, we introduce a half-cycle delay by latching the decision at the output at the negative edge while comparator is clocked at the positive edge of sampling clock [29].

4.4 Design of the current DAC

The feedback reference DAC in our case is a current sink which balances the input signal current during every cycle of operation. Figure 4.21 shows such a structure. In our modulator design, the feedback bit-stream is unipolar. Therefore the current sink is connected to the input or left open depending on whether the bit-stream is either logic high or low respectively. The transmission gate(TG) is used to control the connection of the node either to the input or to a fixed bias. The connection to a fixed bias during logic low is required so that the parasitic capacitances remain at same charged state irrespective of the output bit-stream value [11] of the modulator.This reduces the glitches which are caused due to charging and discharging of parasitics. The reference current needs to be accurately defined through out the operation period. This translates to keeping the drain-to-source voltage of the current sinking transistor constant irrespective of glitches. One way to achieve this is by cascoding. We see that a gain of approximately >60 should be required to bring the level to below 1mV based on transient simulations. The switches shown are implemented as transmission gates.

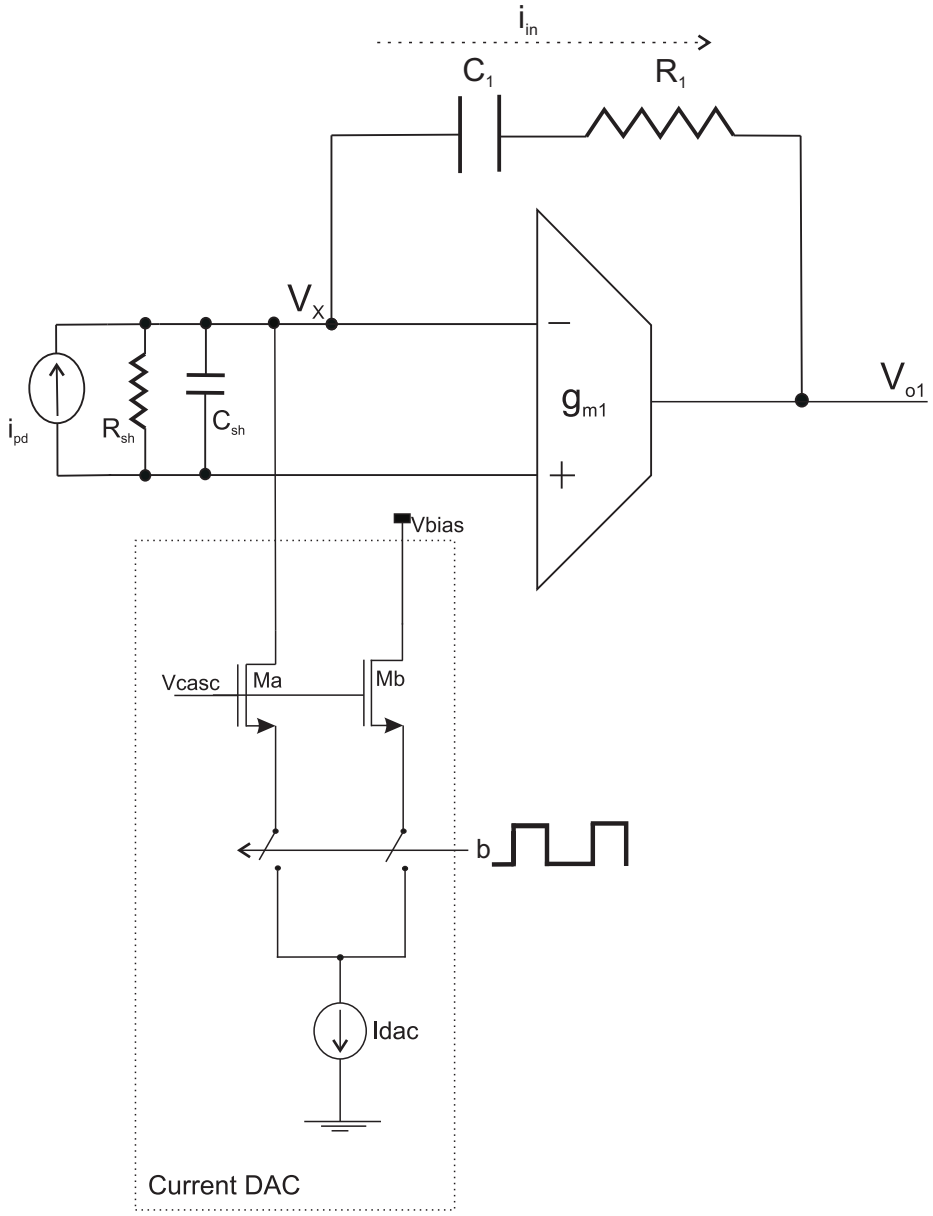

Figure 4.21: Simple Structure of the reference current DAC

Though cascoding helps in improvement, the limited gain provided by a single transistor can be overcome by using gain-boosting technique which is efficient even for low voltage designs [11]. The disadvantage of using gain-boosting is that it results in an additional pole-zero doublet thus limiting the settling specifications. In our design we have enough voltage room available for the current DAC(V_{bias}=0.85V) which can be used to cascode twice the common source amplifier.

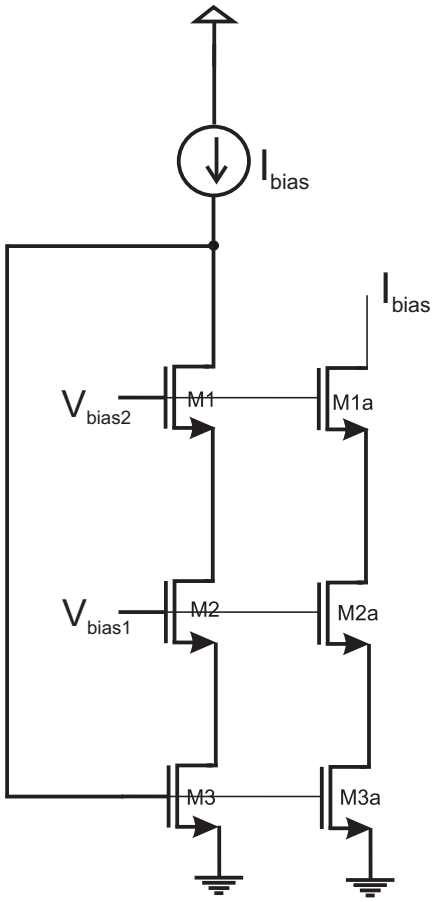

Figure 4.22: Double cascoded wide-swing current mirror reference DAC

This resulting large output impedance is given by

$$R_{out} = (g_{m1} * r_{ds1}) * (g_{m2} * r_{ds2}) * r_{ds3} \tag{4.13}$$

We use the current mirror in figure 4.22 for the current sink shown in figure 4.21. We choose four as the number of branches which contribute individually a fourth of total reference current. Each of these branches is normally connected to contribute to the current sink. A provisional switch is provided (controlled by SPI communication) for each of the four branches for test purposes, in the dynamic reference mode as discussed in section 3.15.

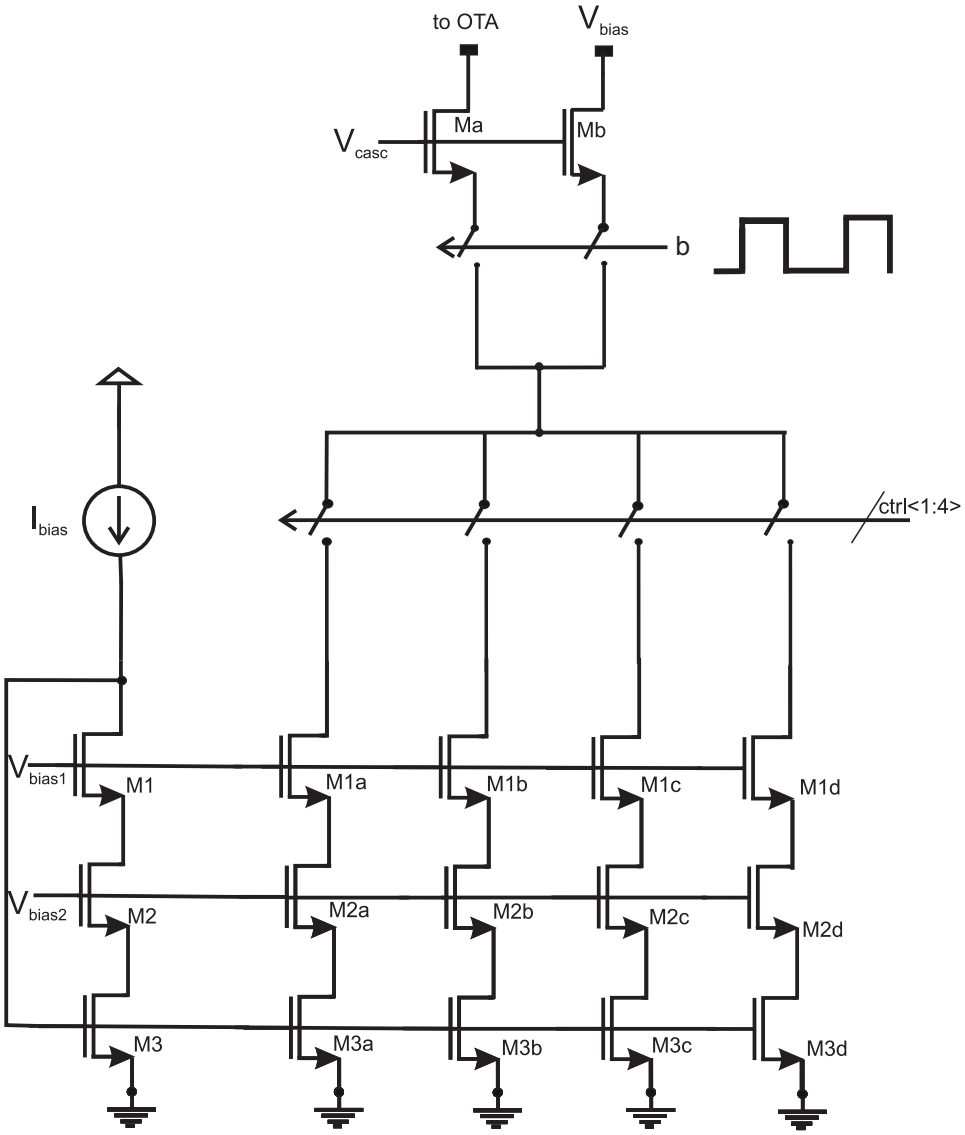

Figure 4.23: Schematic of feedback current mirror reference

The cascodes in figure 4.23 ensure that the drain-source voltage for the NMOS is kept undisturbed during the operation of the first integrator and the switching transients of the DAC current. This is shown by the smooth settling during the switching pulse control in figure 4.24.

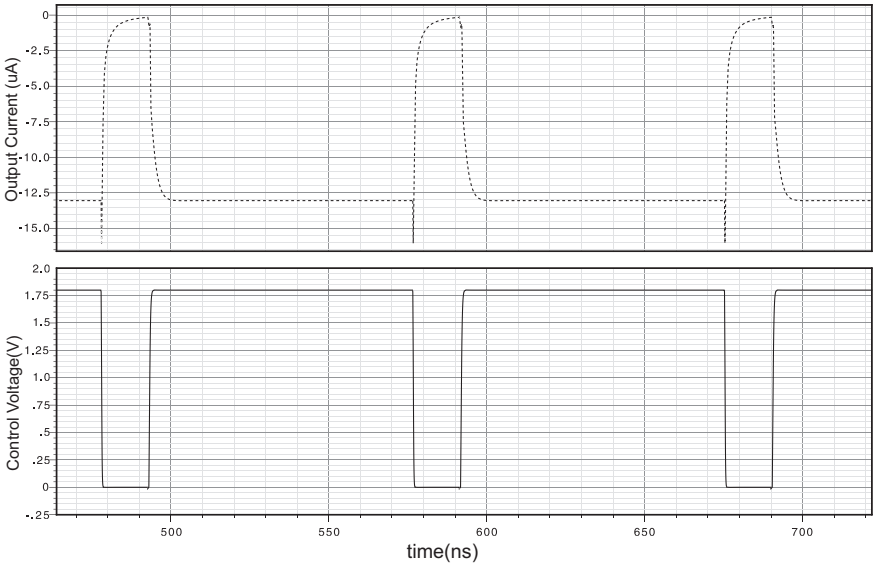

Figure 4.24: Switching control of the feedback current DAC

4.4.1 Return-to-Zero feedback scheme

The output of the comparator is a Non Return-to-Zero(NRZ) format waveform. This controls the feedback current sink. Since any current source or sink has a finite output impedance as well as requires a finite settling time to reach the required accuracy value; the feedback charge balancing of the loop depends on the bit-stream shape(figure 4.24) rather than only on the density. This results in a phenomenon known as Inter Symbol Interference(ISI) which adds non-linearity to the conversion result. One method to avoid ISI is by feeding back a Return-to-Zero(RZ) signal to the current DAC. This is achieved by feeding the control signal only for a fraction of the period. The feedback DAC reference value is chosen according to the duty cycle of the RZ pulse such that their product represents the same amount of charge as in the NRZ case. The RZ format is usually chosen to be 50% duty cycle. In our case this results in doubling of the reference DAC current. This increase in the input current to be integrated results in a higher requirement on linearity range of the OTA. Therefore we arrive at a conservative maximum duty cycle of 85%. This is much larger than the linear settling time given by $\frac{1}{UGBW * \beta} = \frac{1}{24MHz * (R_{pd}/R_{fb})} = 22ns$ for the first integrator.

4.5 Simulation of the modulator

All the blocks were integrated to form the modulator together with the photodiode model and a transient simulation was run for the input signal sweep. The integral non-linearity plot is shown in figure 4.25 with a worst case ±15 LSB without any calibration.

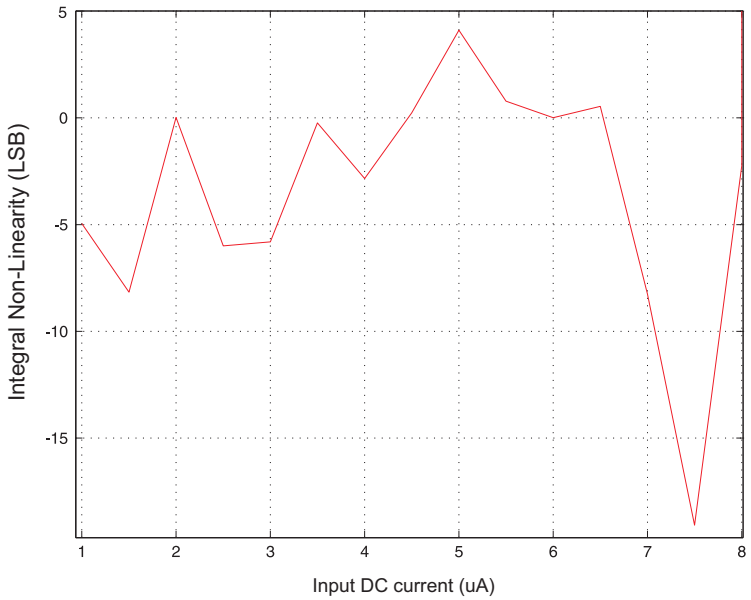

Figure 4.25: Integral Non-linearity plot

The performance is improved by choosing dynamically the reference current DAC value based on input range.This can be seen in figures 4.26, 4.27, 4.28, 4.29 which represent the respective INL in terms of 16bit LSB.

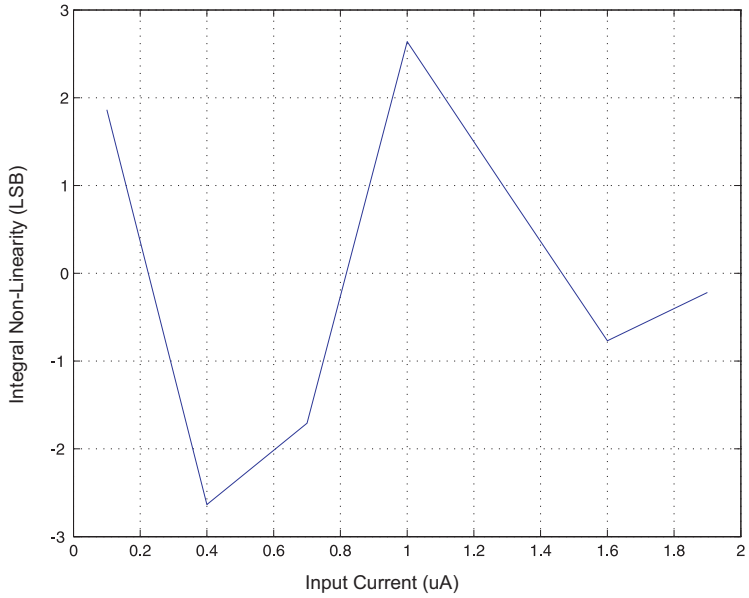

Figure 4.26: Integral Non-linearity plot with 0.25 full-scale reference

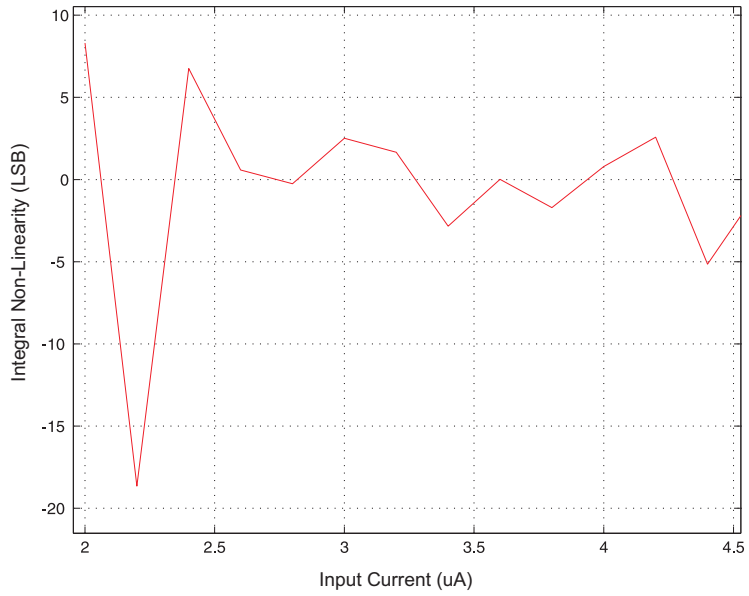

Figure 4.27: Integral Non-linearity plot with 0.5 full-scale reference

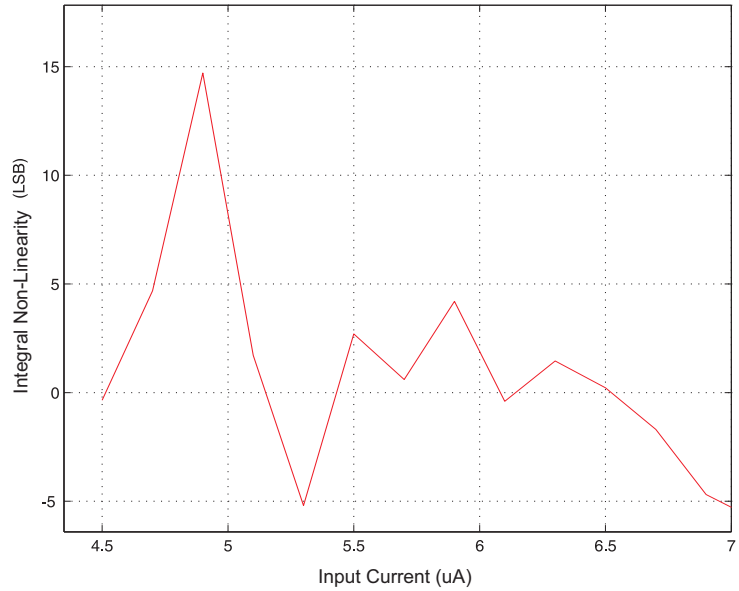

Figure 4.28: Integral Non-linearity plot with 0.75 full-scale reference

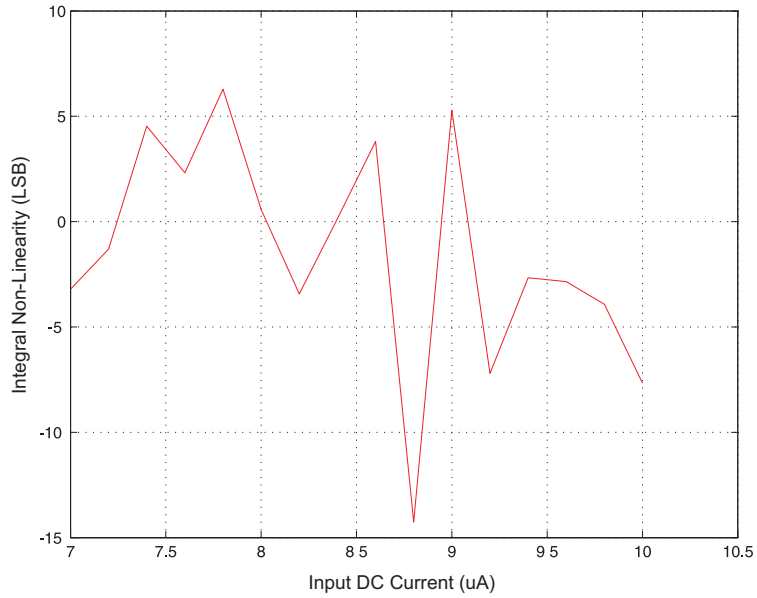

Figure 4.29: Integral Non-linearity plot with full-scale reference

4.6 Summary of the design

The design of the circuit blocks of the modulator has been presented. The specifications are based on the architectural model which was derived in Chapter 3. The biasing of the OTA of the first integrator is tunable in order to choose the value depending on the characteristics of the interfaced photo-diode. The required

noise specifications are met by incorporating chopping switches in the amplifier. The feedback current DAC employs a Return-to-Zero scheme along with provisions for dynamic control of the full-scale value depending on the input signal as a test mode in the presented architecture. The performance obtained from simulation is summarized in table 4.8.

Supply Voltage	1.8V
Sampling Frequency	10.14MHz
Equivalent Signal Bandwidth	3.623kHz
Read-out noise contribution(integrated)	80pA
Normal mode input range	$1\mu A$-$10\mu A$
Normal mode INL	±15LSB
Dynamic reference mode input range	100nA-$10\mu A$
Dynamic reference mode INL(with dynamic reference)	±10LSB

Table 4.8: Performance of the ΣΔ Modulator

4.7 Placement of multiplexer

The overall architecture of the sensor system has fifteen photodiodes connected to each ADC channel by means of multiplexer as described in Chapter 2. This could degrade the linearity, accuracy when the input signal passes through the multiplexer. This is because the multiplexer in the path adds its finite resistance which will be important especially in our design where the photo-diode shunt resistance is low (in the order of input impedance of the first integrator of modulator).

To solve this problem, two multiplexers are used. One to connect one of the photodiodes to the first integrator of the ΣΔ modulator, the other to connect the feedback DAC to this photodiode. Thus, both the input current and the feedback current see the same resistance path into the modulator. This is shown in figure 4.30.

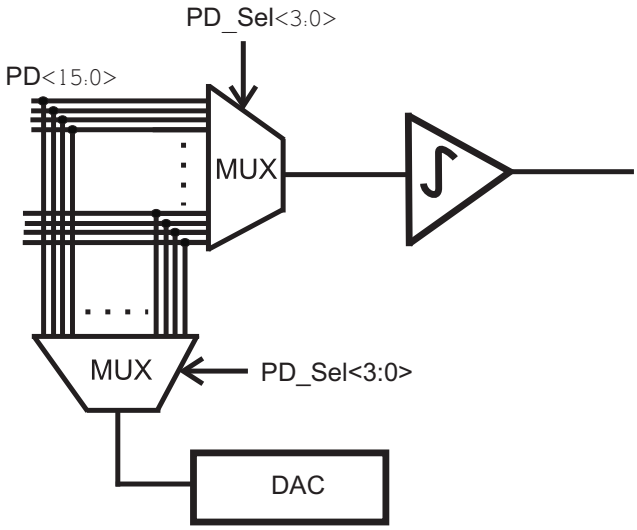

Figure 4.30: Interface of multiple photo-diodes to ΣΔ modulator

The additional multiplexing of the DAC current in the feedback helps to have the complete current flow into the loop as well as provide a symmetrical resistance path.This results in division of total current(input plus feedback) between photo-diode shunt resistance and series combination of input resistance of the first integrator and the ON resistance of the multiplexer ($R_{in} + R_{on} \approx R_{in}; where R_{in} = \frac{1}{g_m} > R_{on}$).

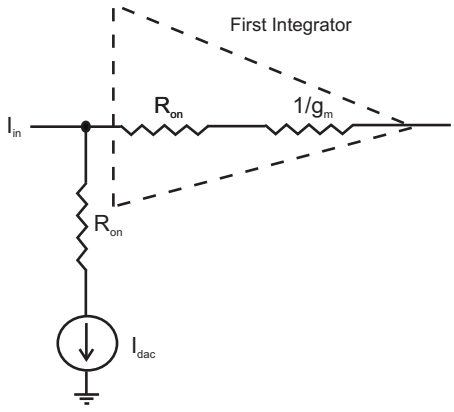

Figure 4.31: Symmetric path seen by the multiplexed input current

4.8 Layout of the blocks

The complete layout of the ΣΔ modulator is shown in figure4.32 and measures 250μm x 0.275μm. Some of the known layout techniques from literature [30] such

as common-centroid for the differential pair of the amplifiers and interdigitated placement of fingers for the current DAC have been incorporated in the layout.

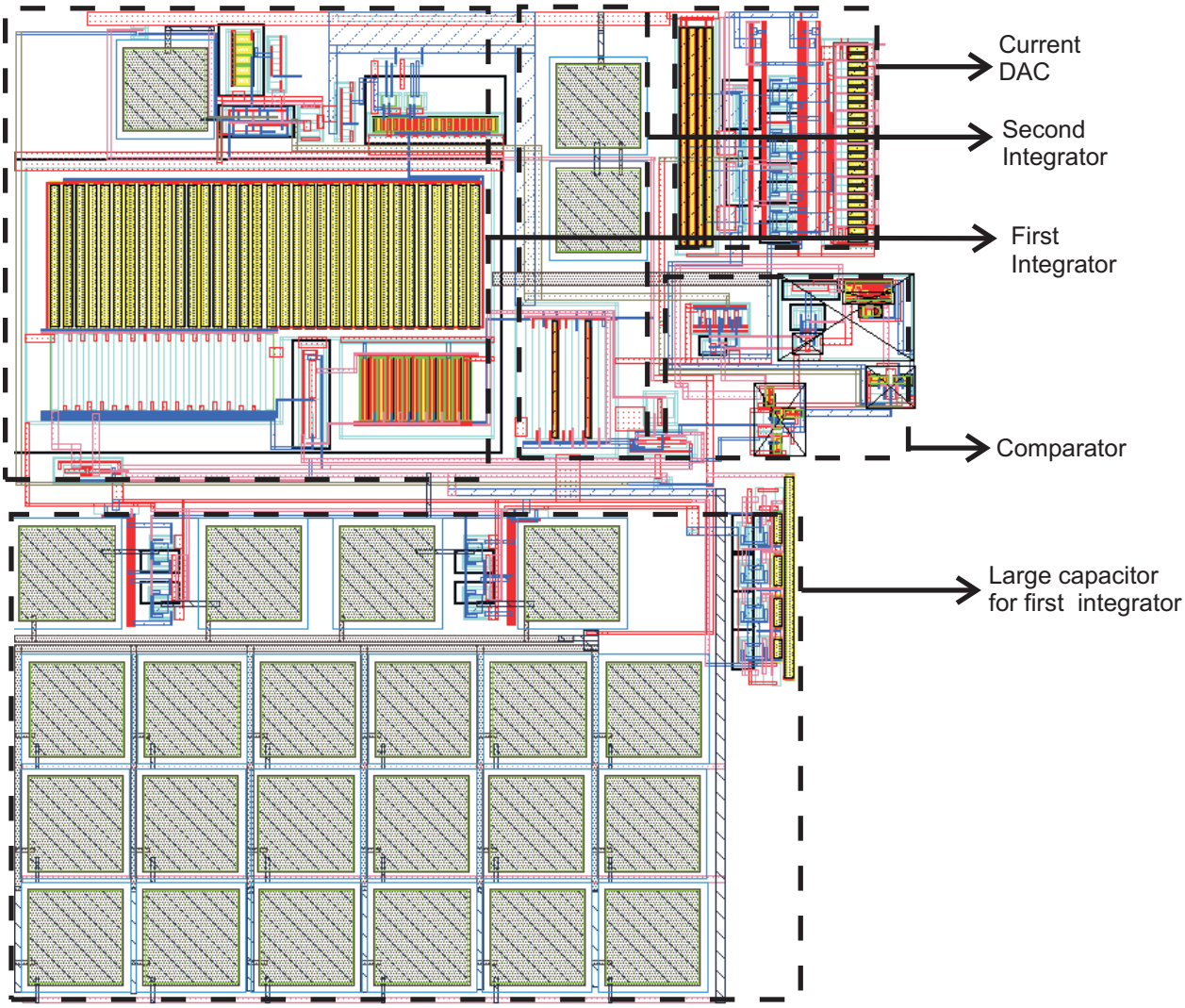

Figure 4.32: Layout of the ΣΔ modulator

There are three ΣΔ modulators on-chip which correspond to the three channels discussed in section 2 figure 2.1. These three modulators together with the multiplexers form the read-out part or the receiver part of the sensor system. This is shown in the figure 4.33. The receiver part layout was completed and measures 820μm x 710μm.

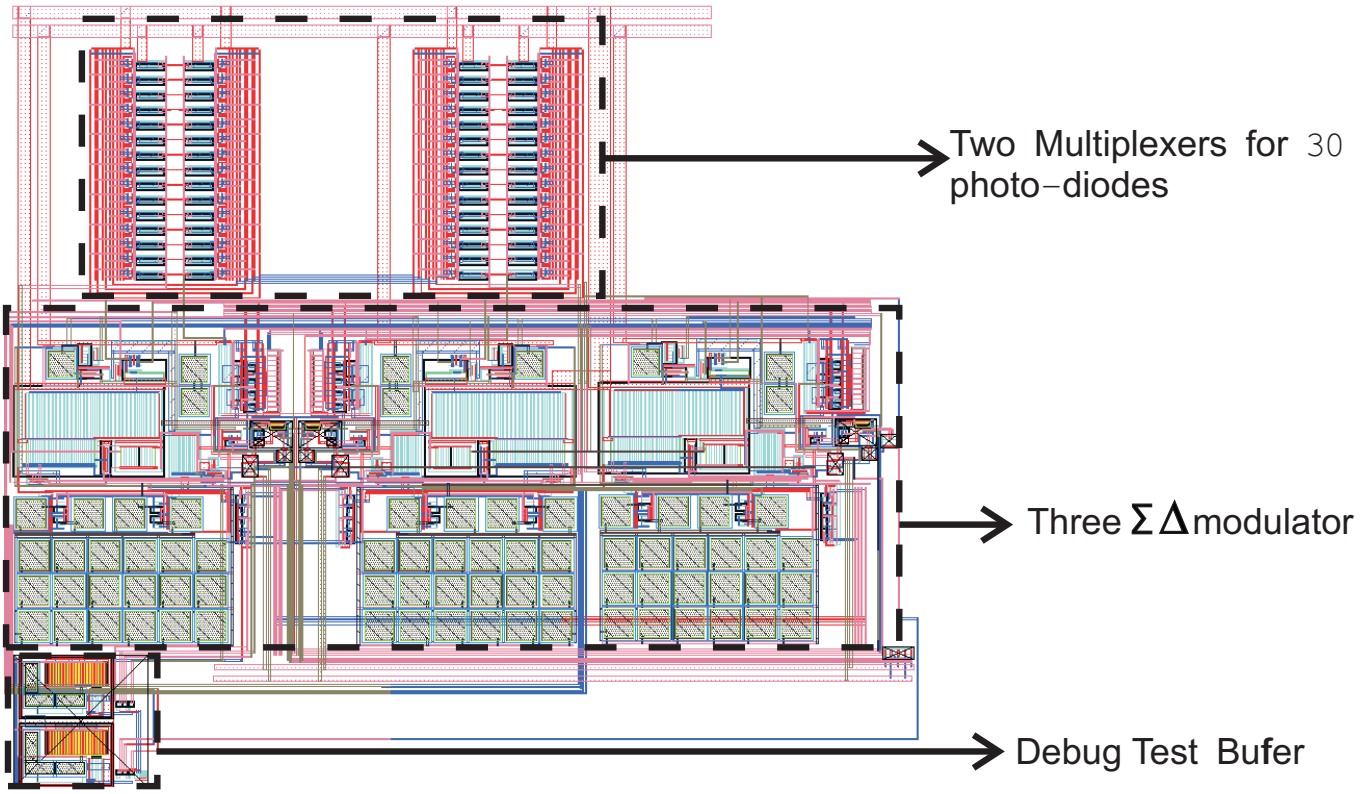

Figure 4.33: Layout of the complete read-out circuit

4.9 Overall chip implementation

The complete sensor system consists of the transmitter and the receiver parts along with the SPI digital block. The transmitter part consists of current DAC channels which was part of an earlier work and re-used here. The complete integrated chip with all the blocks is shown in figure 4.34.

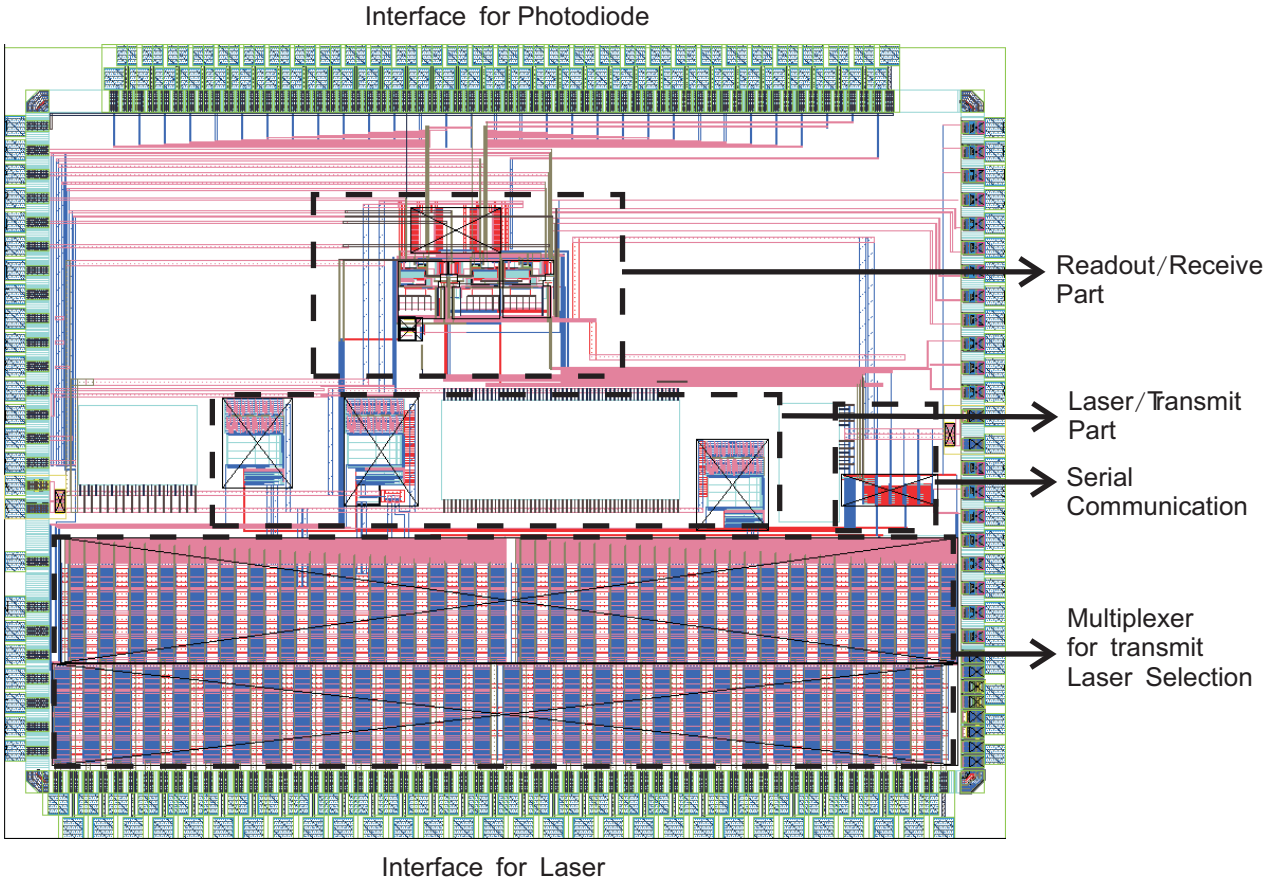

Figure 4.34: Layout of the complete chip

The total chip area is 4.9mm by 3.6mm. Such a large area is required due to the large number of pads and their size required for wire-bonding optical devices with the CMOS chip. The chip was taped out in 0.18μm TSMC process and packaged in a JLCC 84 pin package. The chip micrograph is shown in the figure4.35. The circuitry is not clearly visible due to the dummy metal coverage.

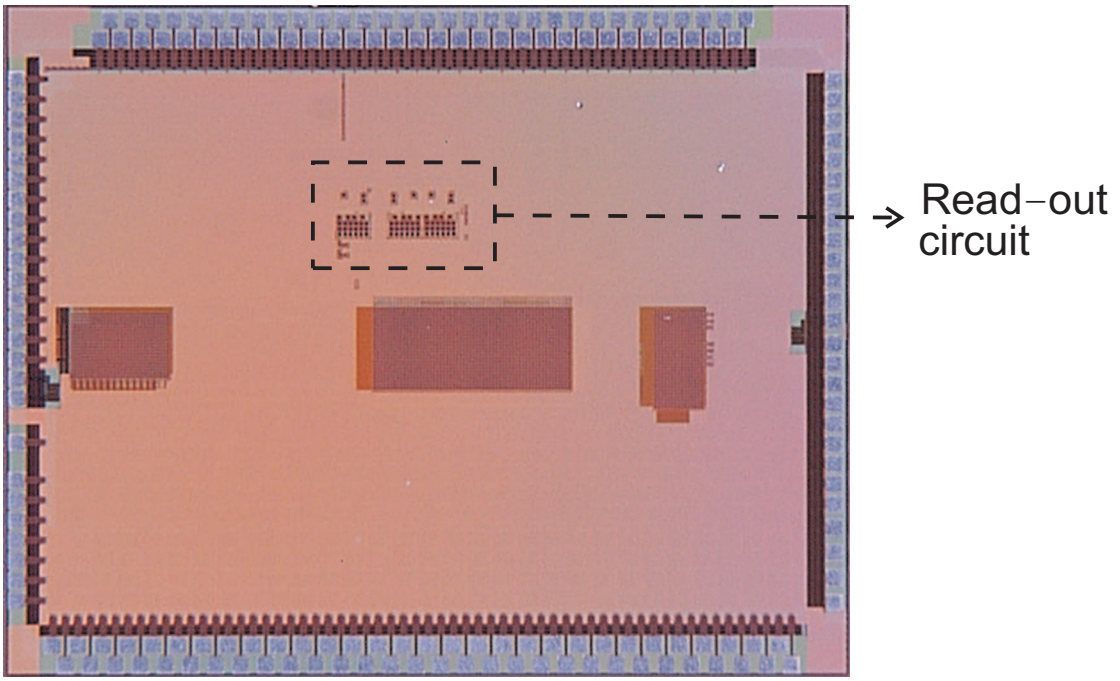

Figure 4.35: Chip micrograph

This chip forms the CMOS electronics for the processing of the signal acquired from the optical part of the system. In the future, the optical devices realized in SOI technology are proposed to be combined with the CMOS chip by either wire-bonding or via flip-chip connections to form a single packaged heterogeneous sensor system.

5

Testing and measurement

This chapter describes the test set-up used to characterize the ADC. The proposed techniques in design such as adaptable biasing scheme as well as dynamic reference selection have been evaluated. The complete characterization has been automated using Labview and the configuration of the glucosens chip is done via a generic microcontroller.

5.1 Measurement approach

A test PCB has been designed with provisions for being able to feed either an electrical test signal or the optical signal input. The resulting output (bit-stream from the $\Sigma\Delta$ modulator) is acquired using a USB interface for analysis in a host PC using Matlab or Labview. The main components of the test PCB schematic are included in Appendix C.

A microcontroller CY8C3866AXI Programmable System-on-Chip (PSoC) controls the overall characterization and configuration of the chip. The configuration of the ADC as well as that of the multiplexer for the transmitter channel and receiver channel are set by the registers provided in the chip via the SPI communication. The description of the registers is included in Appendix A. The configuration is done in our set-up by the firmware in PSoC which controls the operation of the chip. The configured bits are fed out serially from the glucosens chip as a method to verify the right digital configuration as shown in Appendix A.

We follow a three-step approach here due to the limited time available for the measurements during the final stage of the thesis project. The first step involves a 8-bit current DAC (Full Scale=31.875μ A) inside the PSoC feeding the glucosens chip. The results of this will confirm the functionality of our chip although the performance is limited by the linearity of the source (≈6-7 bits for 10μA range). The second step replaces the 8-bit current DAC with a Keithley 2602 Source Measure Unit (SMU) which provides a finer step current with noise PSD of 50pA/$\sqrt{Hz}$ across 0.1Hz to 100Hz for 10μA range of current. The results obtained will be shown to be close to the higher theoretical limit we expect, although still limited by the test stimulus noise which does not correspond to the specifications of the photodiode devices (2pA/$\sqrt{Hz}$). In the third step, a demonstration of the circuit with a custom silicon photodiode is shown to demonstrate the effectiveness of the application of the circuit to the sensor. Due to time restrictions, the final proposal of setting up an 18-bit voltage DAC and on-board voltage to current conversion could not be completed at the time of writing this thesis and will be followed up in future to completely characterize the ADC.

5.2 Results obtained using 8-bit current DAC

A block diagram of the test set-up is shown in figure 5.1 while the photograph is shown in figure 5.2.

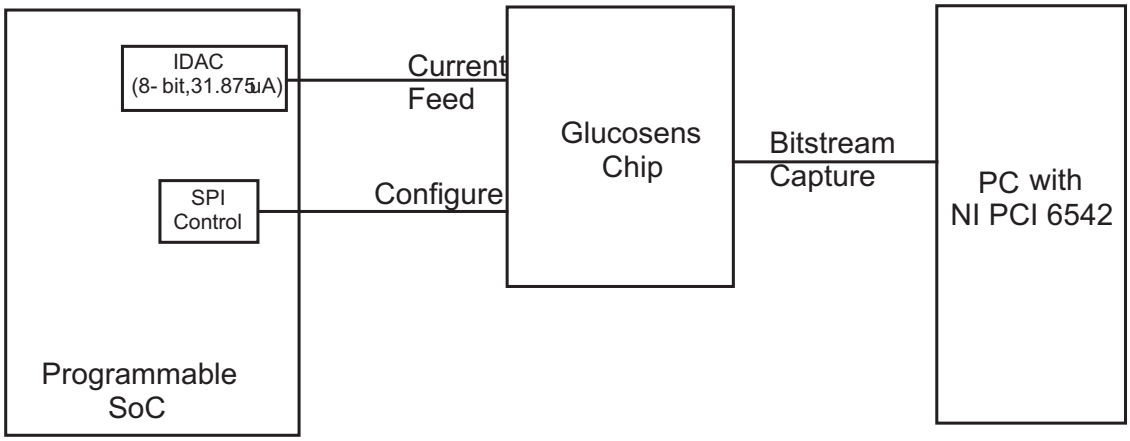

Figure 5.1: Block diagram of the first test set-up

The complete measurement procedure was automated with the feed-in current DAC value controlled in the firmware. The full-scale current for 8-bit current DAC in the PSoC is 31.875μA. The capturing of output bit-stream using Labview and post-processing using Matlab was done on the PC side. The PC was equipped with a NI PCI-6542 digital waveform analyzer.

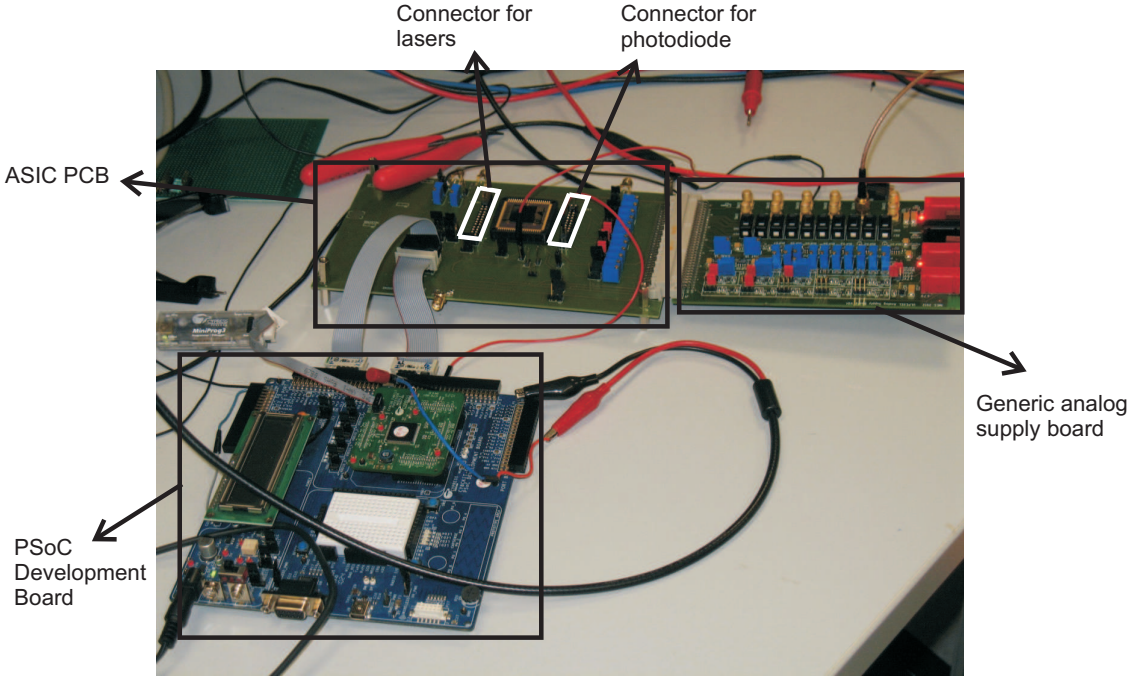

Figure 5.2: Set-up for testing the chip

The individual boards are shown in figures 5.3, 5.4 and 5.5. As can be seen that the development board shown in figure 5.5 is interfaced via programming header provided on the chip pcb side. This was done to be able to control the chip via any generic controller of via Labview on PC. The next version of the test PCB for chip is provided with both this generic programming header as well integration of PSoC with the glucosens chip which is shown in Appendix C. These provisions help make the testing and control modular while also helping ease debugging efforts.

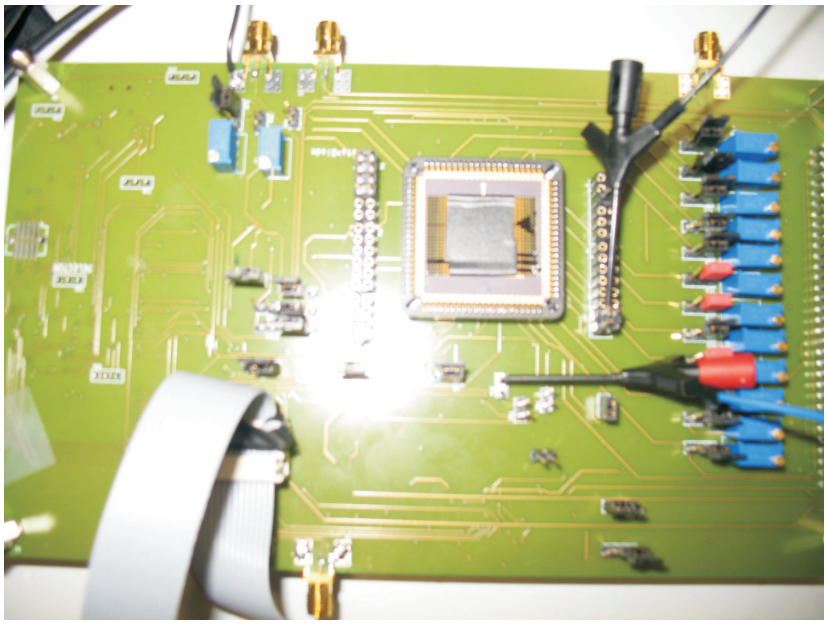

Figure 5.3: Test PCB for the chip

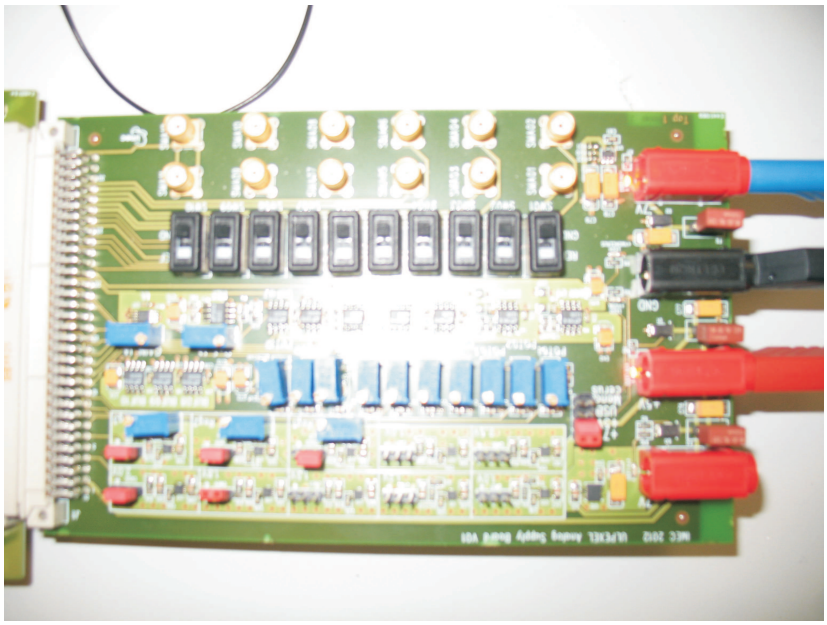

Figure 5.4: Analog supply board for the chip

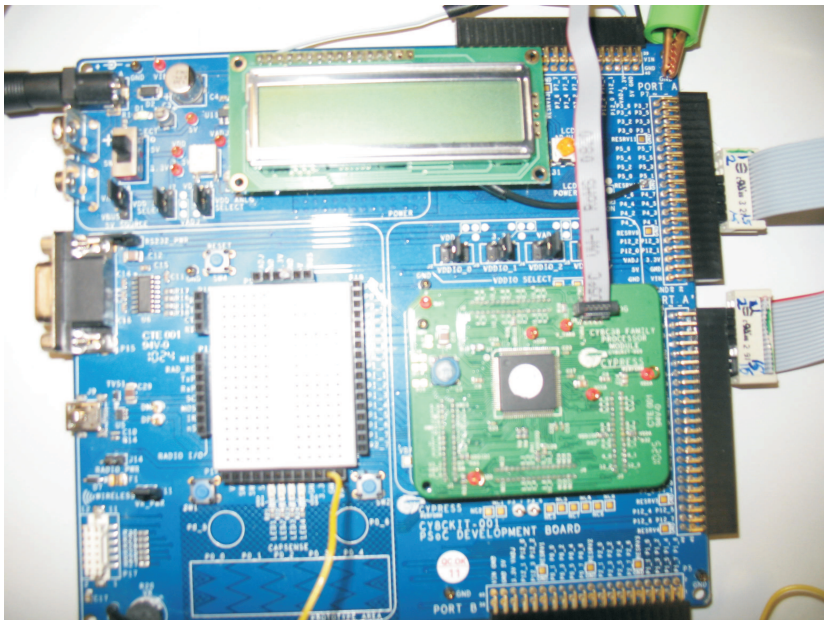

Figure 5.5: Microcontroller development kit used for interfacing

The current is fed to the direct laser channel, as shown in figure 2.1, for characterization. There are two knobs for the ADC as discussed in Chapter 4, that of adaptable biasing(mode-1 and mode-2) and dynamic reference. The results in the following are using mode-2 for biasing and the dynamic reference scheme is not used for the initial testing. Therefore the reference DAC is set to full-scale. The resetting of integrator before the start of conversion is via a reset pulse from PSoC to the pin of glucosens chip which operates the ADC in the incremental mode.

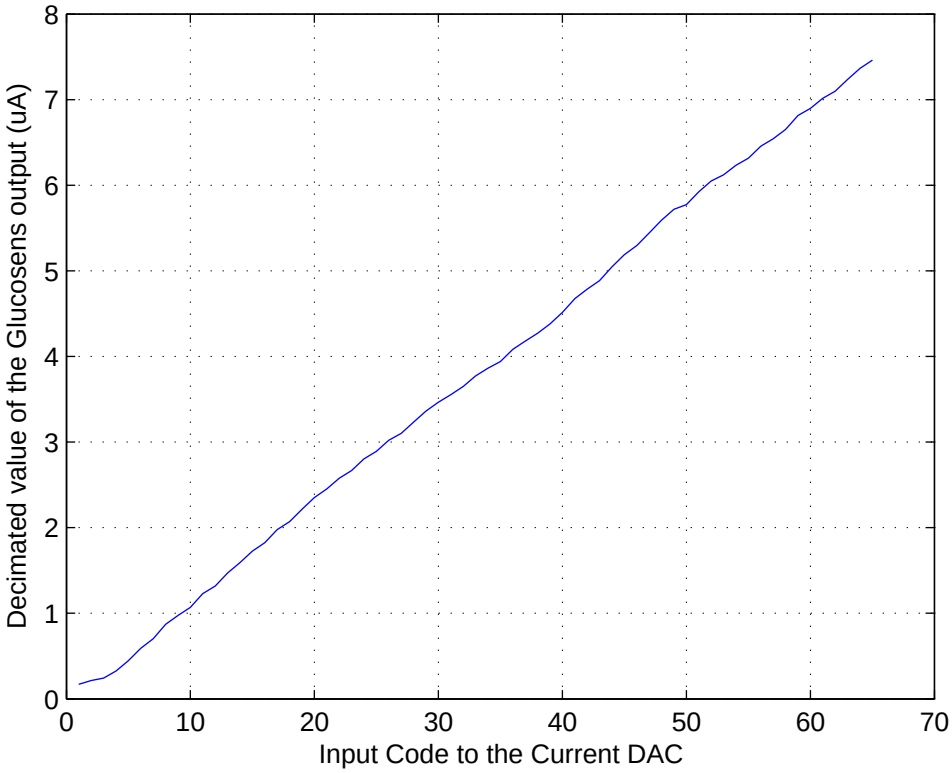

Figure 5.6: Measurement of the feed-in current

Based on the measurement data, we estimate the linearity. Here we must note that the best possible result is limited to a maximum of 7bits as guaranteed by the current DAC data-sheet for the 10μA range. In addition, the current noise PSD output of the DAC is higher than the estimate specified for the photo-diode (2.1 pA/$\sqrt{Hz}$). The Integral Non-Linearity obtained based on the measurements of first set-up is shown in figure 5.7.

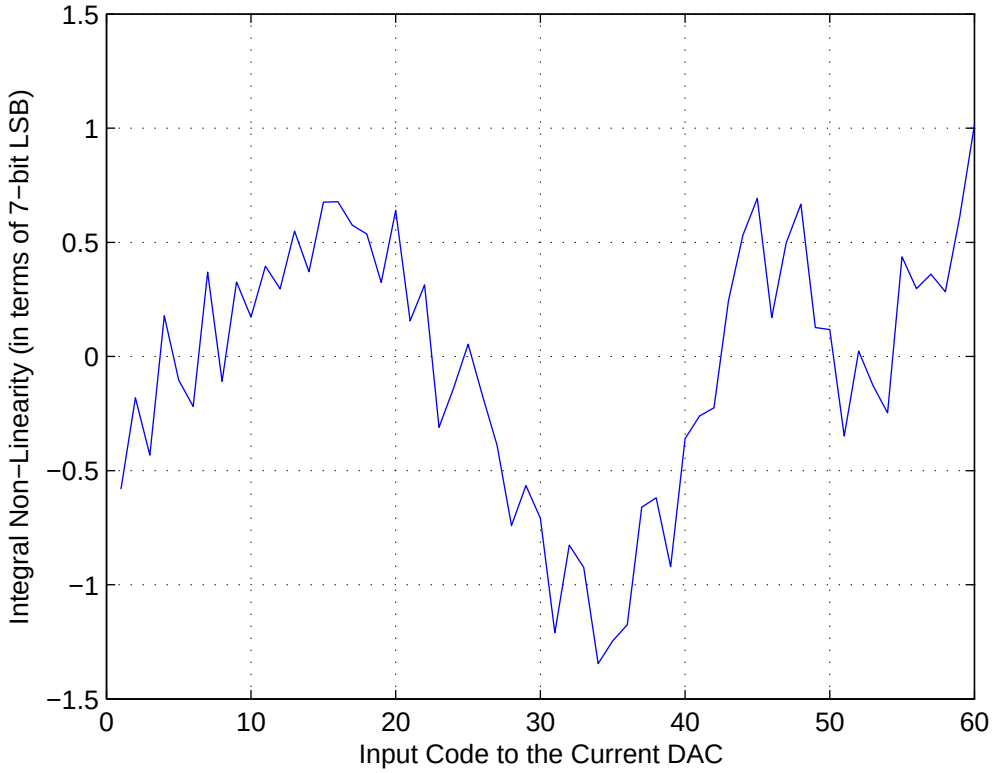

Figure 5.7: Integral Non-Linearity

The plot shows that we are close to the theoretical maximum (i.e. the INL of the stimulus DAC) possible in terms of linearity (results shown in terms of 7bits LSB).

5.3 Results obtained using Source Measure Unit (SMU)

The block diagram of the set-up is shown in figure 5.8. A Keithley 2602 source measure unit (SMU) provided a high resolution current for the characterization while a picoammeter was used to be able to calculate the applied current with a much better accuracy than the device under test for the calculation of linearity.

In Chapter 2, we had analyzed that the specifications of the maximum photodiode PSD is ≈ 2.1 pA/$\sqrt{Hz}$ which corresponded to maximum range of input current. In order to achieve low conversion time for energy-efficiency at the system level, we used this noise specification as the major contributor in the system and the achievable resolution of the design was based on this value. In comparison, in our present test

set-up, though we are able to provide finer steps of current, the SMU specifications [31] show that the output current noise PSD is 50pA/$\sqrt{Hz}$ for 0.1Hz to 100Hz when sourcing currents in the 10μA range. Therefore we find an increase in noise by approximately 25 times with our SMU source. As a result, the resolution obtainable from the ADC is reduced. The degradation in performance can be quantified by the noise factor involved i.e. noise increased by $20 * log_{10}25 = 28dB$ implying a reduction of ≈5bits of performance. Therefore theoretically the maximum achievable resolution is limited to 10-11 bits from the ADC.

The Integral Non-Linearity obtained based on the measurements of chip shows ±1 LSB linearity for 10bit resolution in figure 5.9.

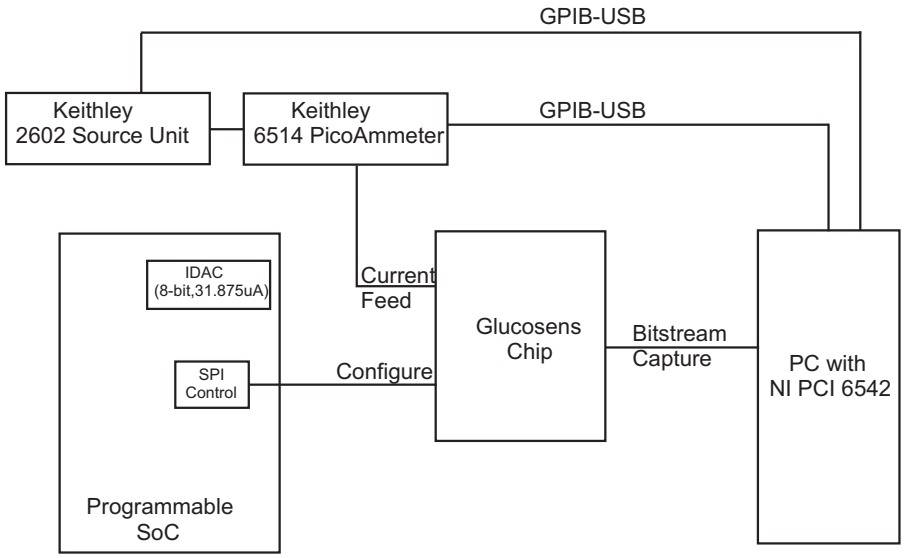

Figure 5.8: Block diagram of the second test set-up

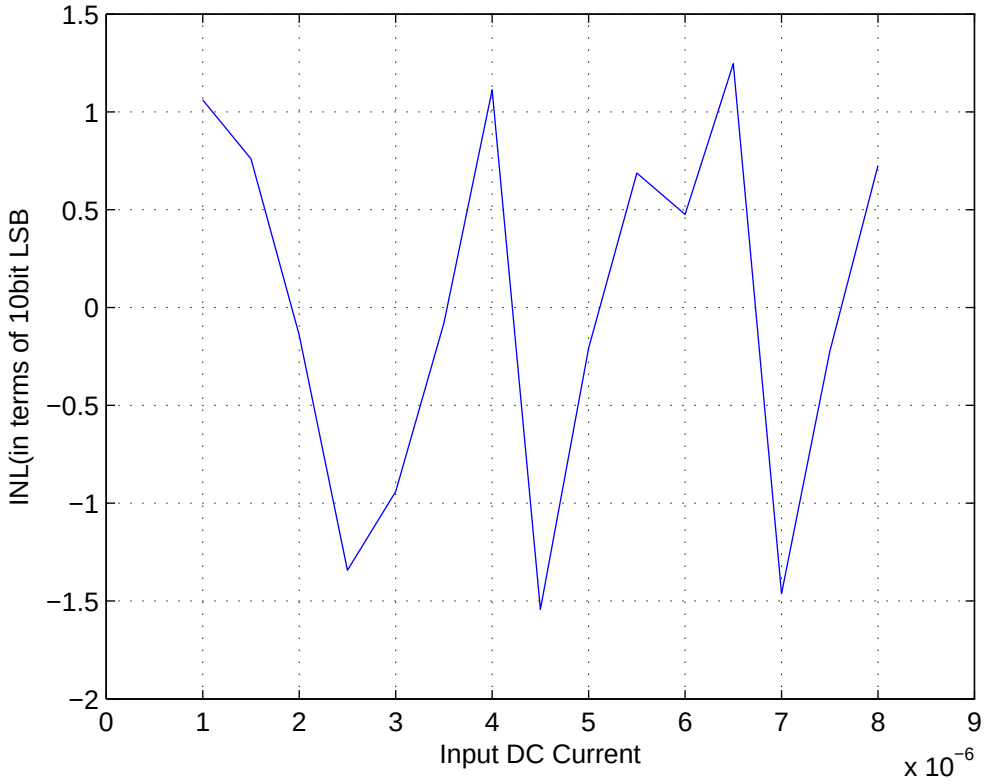

Figure 5.9: Integral Non-Linearity

5.3.1 Noise shaping

Figure 5.10 shows the measured power spectrum of the second-order modulator for a dc current feed. It can be noted that there is tonal behavior for the dc signal input.The second-order noise shaping (40dB/decade) is shown by the spectrum.

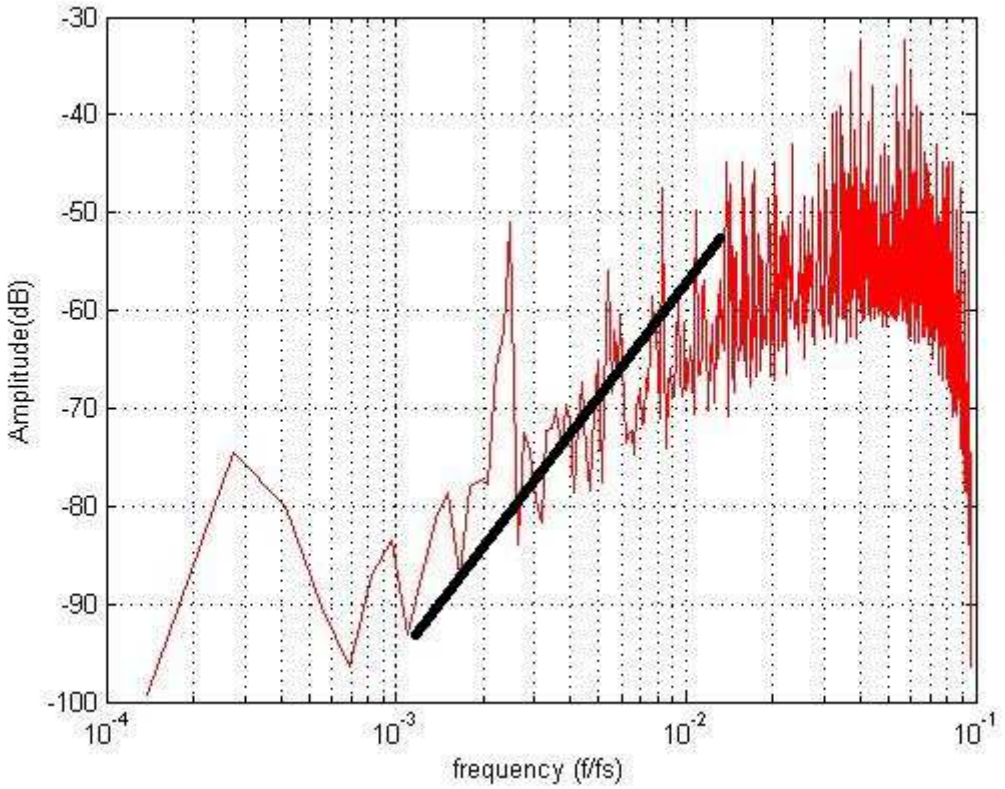

Figure 5.10: Spectrum of measured bit stream(FFT of 700 bits)
for dc current input of full scale/3

5.3.2 Dynamic reference mode

The concept of improvement of dynamic range was tested for various control settings. It was shown that the performance is maintainable across the different dynamic reference selections.

The results with reference DAC set to 0.25 times full scale value is shown in figure 5.11 and 5.12.

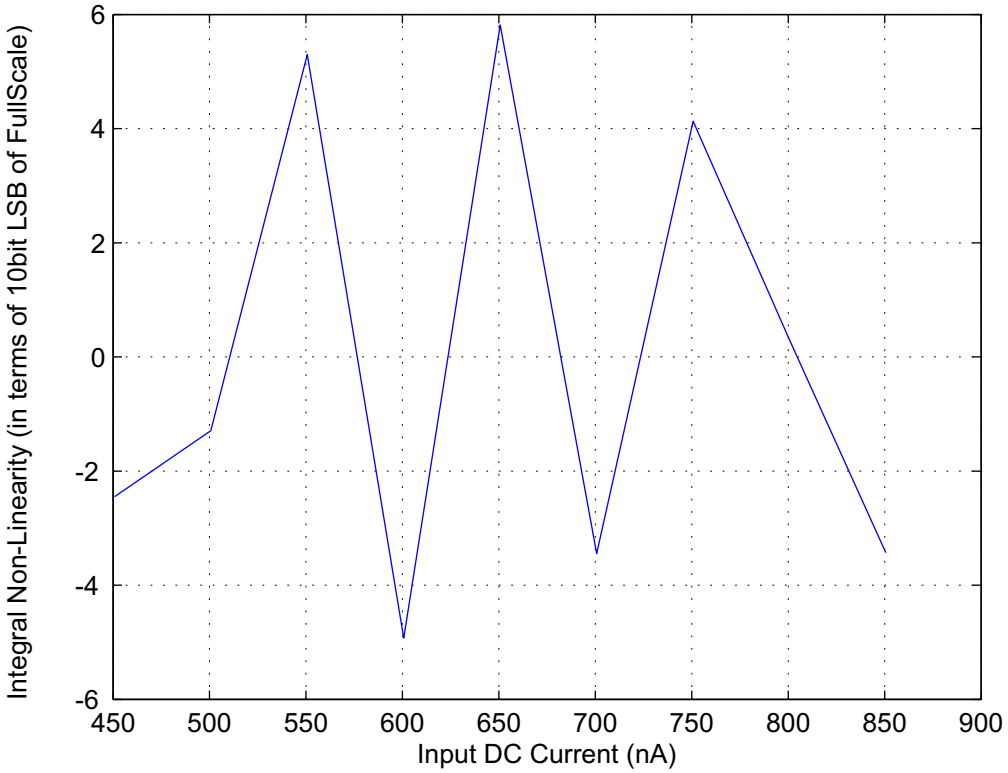

Figure 5.11: Integral Non-Linearity using reference of 0.25*full scale for low currents

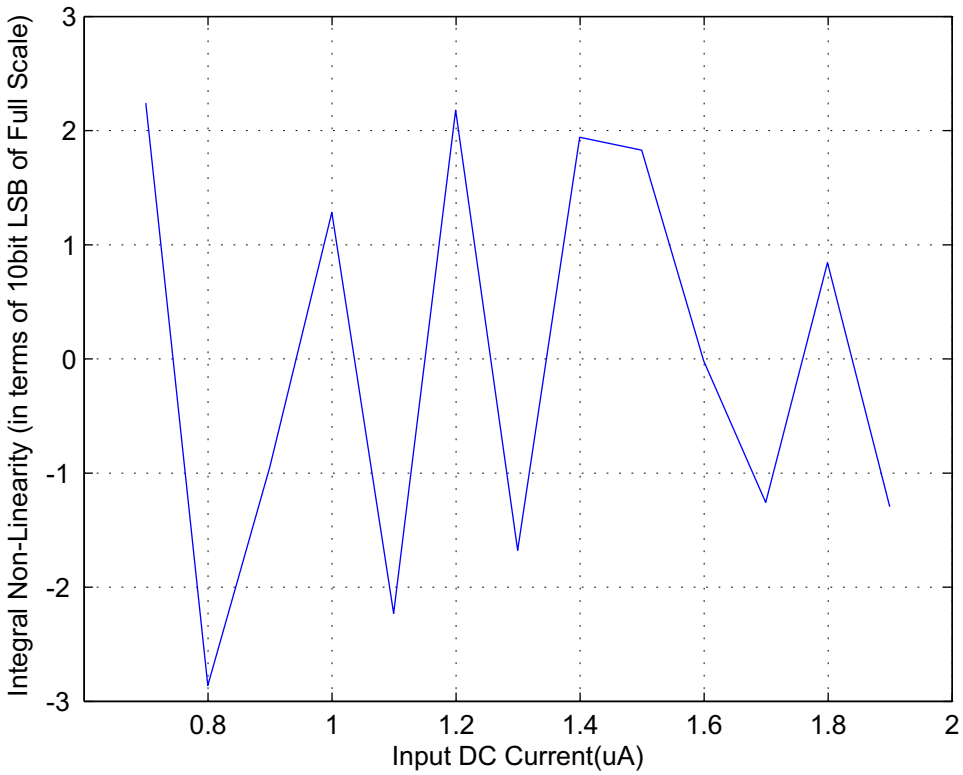

Figure 5.12: Integral Non-Linearity using reference of 0.25*full scale

At the other settings, i.e. 0.5 and 0.75 times full scale, the performance is limited to about 10bits (due to source thermal noise) and does not improve the SNR. This is because the assumption of our proposed dynamic reference scheme is that the system is limited by quantization noise. This does not apply to our current test set-up where we have a fixed higher thermal noise floor.

To conclude this section, we note that from measurement results in figure 5.11, our idea of tuning dynamic reference based on input signal made it possible for the ADC to be interface with a larger dynamic range input current. The other advantage we proposed on improvement of SNR in our simulations in figure 3.18 could not be proved by measurements. This was because the underlying idea of changing reference improves the quantization noise and thus improves the SNR, while in the present measurement set-up we are limited by the thermal noise and thus do not see this improvement in the results.

5.3.3 Power consumption

The power consumption of the read-out part of the chip was measured. As discussed in section 4.1.6, we note the power consumption in two operation modes. The two operation modes were mode-1 which was used when the photodiode shunt resistance was low while mode-2 was selected when the shunt resistance of the photodiode was large. In mode-1, the total current consumption of the read-out part is 346.6μA while in mode-2 the consumption was measured to be 142.3 μA from a 1.8V supply. This power consumption is divided among three ADC channels which results in an effective power consumption of 207.96μW for mode-1 and 85.38μW for mode-2. In contrast to the power numbers from simulations in Chapter 4, we find this to be slightly lower. This can be explained because the biasing scheme for the read-out was via external potentiometers which gave us freedom to fine tune around the actual bias current.

The biasing scheme (mode-2) can be employed when a different photodiode is interfaced (whose shunt resistance is large) with the circuit. The setting of the configuration bit is done based on prior knowledge of the photodiode characteristics. This provides an overall factor of 2.44 times lower power consumption than the default mode (mode-1).

5.3.4 Adaptable biasing of the read-out channel

The adaptable biasing of the design was verified by testing the operation of the chip in mode-1 and mode-2 as discussed in Chapter 4. The operation used for characterization until now was mode-2 as the characterization set-up was done using Keithley SMU or by a current DAC (which did not have a low shunt resistance as that of photodiode).

To test in the mode-1, we included a shunt resistance(22kΩ) with the SMU and configured the chip to operate in mode-1. The linearity plot for the input current from SMU is shown in figure 5.13.

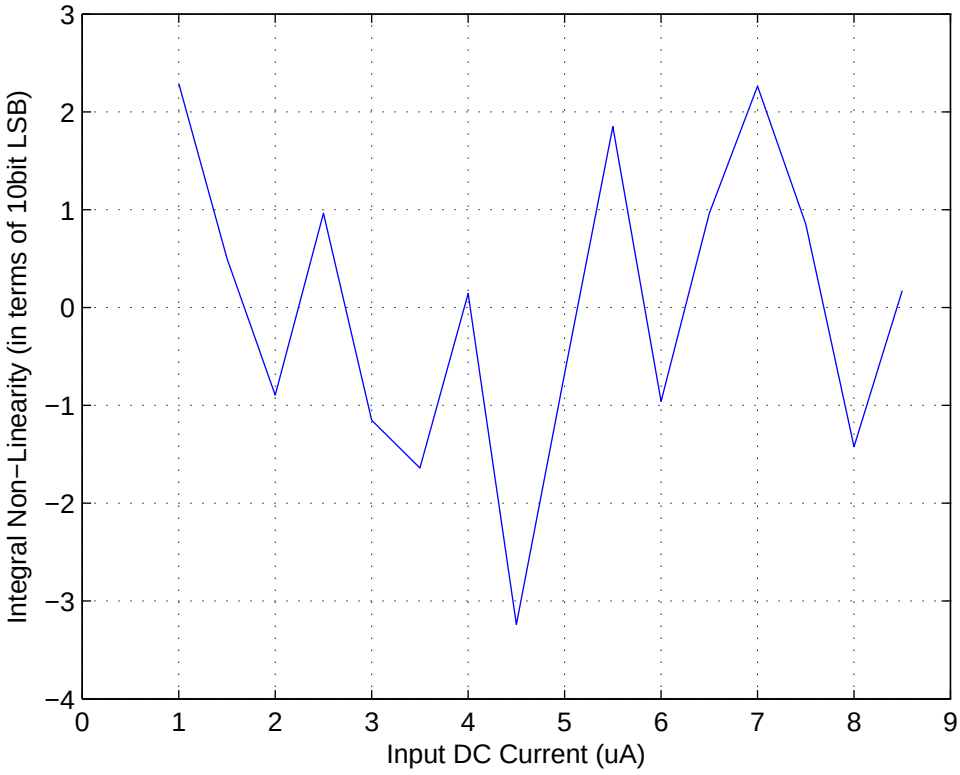

Figure 5.13: Integral Non-Linearity for power mode-1

In the above measurement, in addition to 50pA/$\sqrt{Hz}$ noise, we have an additional 0.88pA/$\sqrt{Hz}$ due to thermal noise of the shunt resistance.

In contrast,response for mode-2 operation when SMU is used without external shunt resistance is shown in figure 5.14.

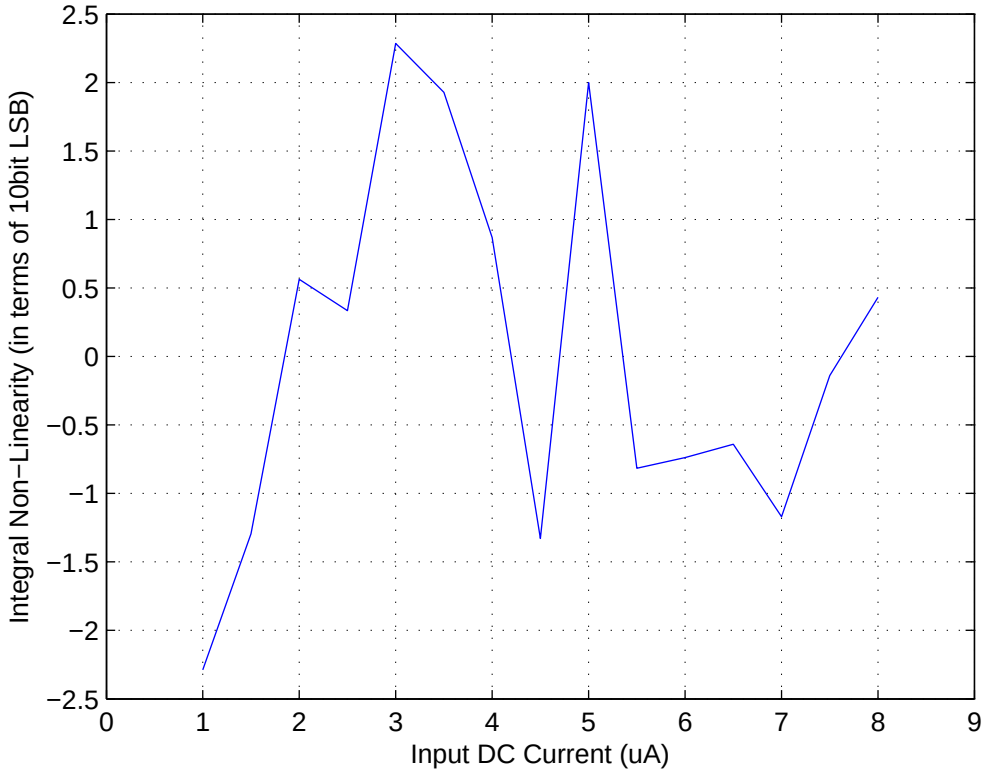

Figure 5.14: Integral Non-Linearity for power mode-2

5.4 Benchmark

The table below shows the comparison of the design with a similar photodiode read-out from literature [2].

Features	CICC'06[2]	This Work	Units
Technology	CMOS 0.35	CMOS 0.18	μm
Current Consumption per channel	<4m(range dependent)	<115.5μ (range dependent and photodiode shunt impedance dependent)	A
Conversion time	236	138	μs
Resolution of ADC(Design/Simulation)	13	18	bits
Measured SNR	66(thermal noise of sensor limited)	62(thermal noise of test stimulus limited)	dB
Input Current Range	40n-2.56m	10n-10μ	A
Number of photodiodes per channel	8	16	

Table 5.1: Comparison of results with [2]

Though the read-out designed in this work and [2] address the issue of interface circuits for photodiode, the end application decides the specifications targeted. The targeted resolution in our design is 16 bits while [2] presented a maximum of 13 bits. Discrete time implementation was used with additional front-end stage for gain selection was employed in [2], while in our work we have used continuous time

$\Sigma\Delta$ modulator implementation while using dynamic reference tuning technique for addressing the dynamic range problem. The measured performance of [2] was with a photodiode (BPW 34 [32]) whose noise PSD is given by 2.6*10^{-14} A/$\sqrt{Hz}$ (i.e. Spectral Sensitivity[A/W]*Noise Equivalent Power[W/$\sqrt{Hz}$]), while our measured results presented were with a SMA of noise PSD of 50pA/$sqrtHz$. In terms of the conversion time and performance in the common range of input current, our design performs better. The performance comparison takes into account that the thermal noise of the source is higher in our set-up compared to [2] while the achieved resolution is comparable. On the other hand, [2] can convert a wide dynamic range of input which is two orders higher than the range we designed for. This advantage is at a cost of an order increase in the power consumption.

5.5 Optical-electrical interface demonstration

A demonstration of a photodiode interfaced with the chip is shown in this section as a proof of concept. Since the photodiodes on SOI by Ghent University were not available at the time of writing of this work, a Si photodiode available at IMEC was used to show the application of the circuit.

A controlled light source was used to illuminate the photodiode. The photodiode was covered by a polarizer to limit the incident light so that the output current was less than the full scale of 10μA of the read-out. The sensor and light source used for the experiment is shown in figure 5.15 and 5.17.

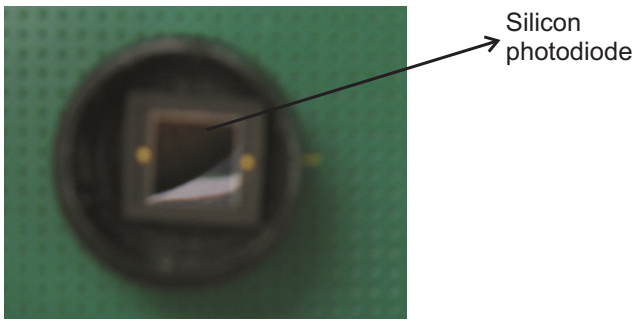

Figure 5.15: Silicon Photodiode used for the measurement

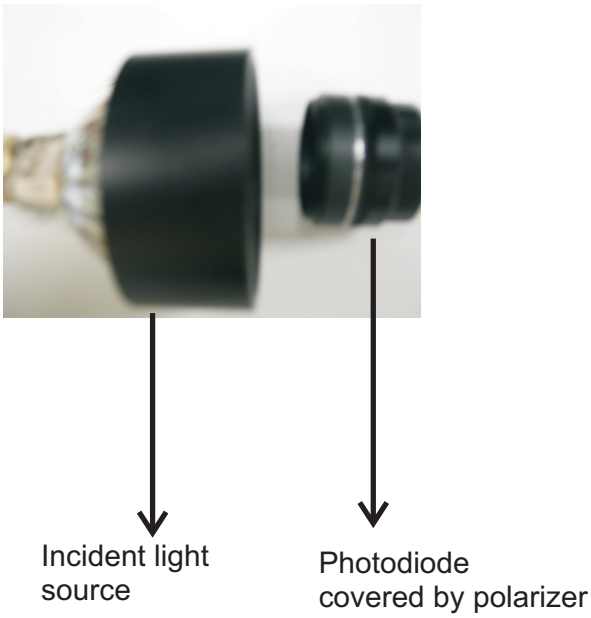

Figure 5.16: Photodiode set-up to be interfaced with the glucosense chip

The visible light from the source is incident on the photodiode at four different intensities and corresponding current output from the photodiode is noted via Keithley pico-ammeter. Figure **??** shows the resulting current measured by the glucosens chip against that recorded on the pico-ammeter. Note that these measurement shows the application of the circuit for the interface function and no calibration of incident light was done in this test set-up.

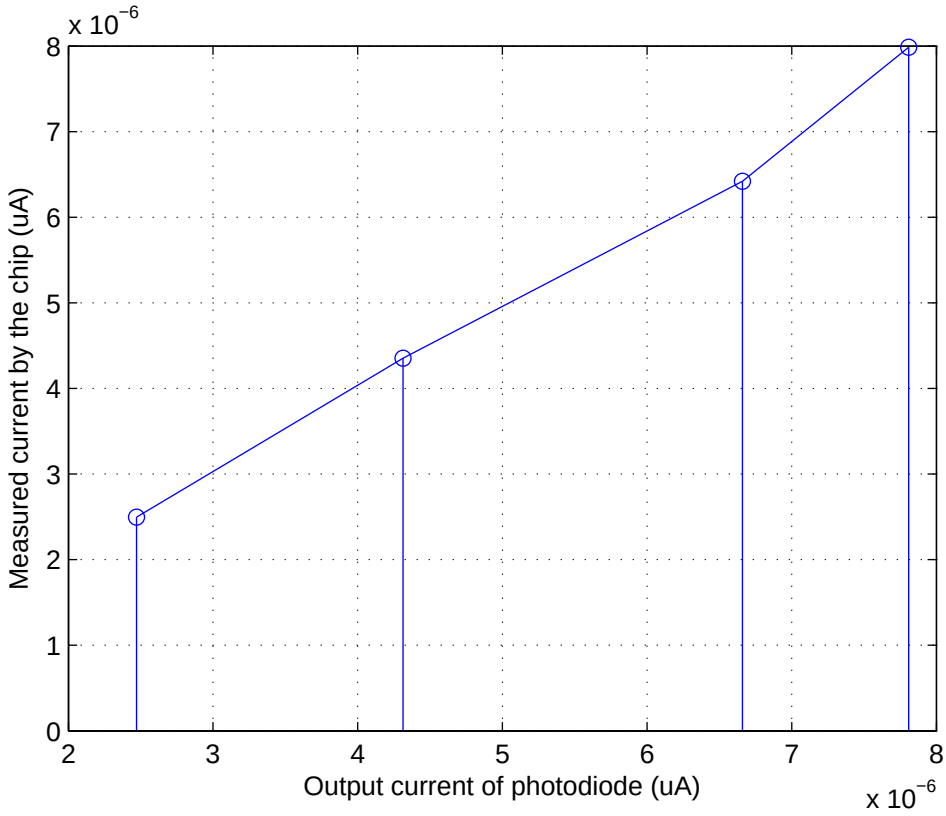

Figure 5.17: Measurement of current from a silicon photodiode

5.6 Further proposed characterization

The analysis of the second test set-up showed us that the noise PSD of Keithley SMU is higher than required. Therefore a method to reduce this and to increase the resolution is needed.

A voltage DAC (TI DAC9881) was chosen whose output voltage is converted to a current by a regulated current-mirror circuit. A 5:1 ratio is used to feed the current to the device under test. This is done to make the noise contribution of the input branch of the current mirror negligible. An amplifier (LT1006) provides the necessary dc gain to keep the drain-to-source voltage level same so that M2 provides the required current in the range of $1\mu A$ to $11\mu A$ to the ADC under test. The DAC is controlled via the SPI to the DAC9881.

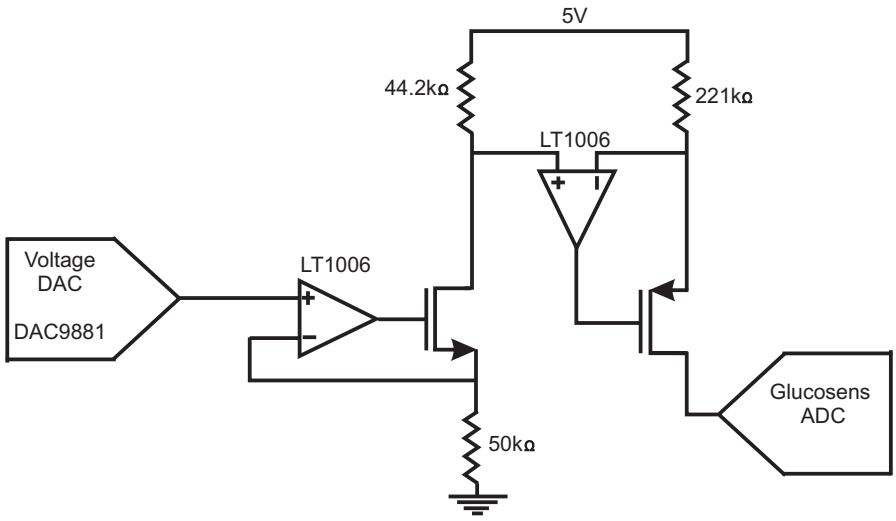

Figure 5.18: Current stimulus to the ADC for characterization

This is the proposed solution for future characterization which is currently being undertaken.

5.7 Conclusion

The measurement of the chip showed us that the chip is functional followed by the analysis that the performance was limited by the test set-up, as the resolution improved when a source closer to noise specifications of the photodiode was used in the form of a Source Measure Unit. The application of the circuit was demonstrated by having visible light incident on a silicon photodiode and the output current read-out by the chip in the final step.

The future steps to complete the characterization of the chip using the voltage DAC followed by a voltage to current converter have been proposed in the final section of this chapter. During the characterization process, few additional points were noted. On observing the clock fed to the chip using active probe, it showed that the method of external clock generation can be improved with better PCB layout method [33] (inclusion of end termination, routing in pair) or using on-board clock dividers fed from pulse generator. This provides for better synchronization as well as shape of the pulse arriving at the glucosens chip is close to ideal. There was

also a limit on the duty cycle achievable for the Return-to-Zero clock(10.14 MHz) due to the available on-chip PLL maximum frequency of the PSoC being limited(60 MHz).This made the duty cycle with finite steps. This restricted our full range achievable in above measurements because the full scale of the DAC was decided by the set duty cycle times the fixed full-scale of the feedback DAC. This can be further improved if a higher clock frequency is available in the controller.

6

Conclusions

This final chapter summarizes the work completed and the results achieved. It also outlines the limitations and improvements suggested in the test set-up for future characterization.

6.1 Summary of the work

An understanding of the photodiode has provided us an insight into the signal and noise characteristics of the input. This was crucial as it also led us towards optimizing the overall design for energy efficiency which were discussed in Chapter 2. The complete sensor system was implemented based on the architecture we proposed in Chapter 2. It was shown in Chapter 3 that $\Sigma\Delta$ modulators are the ideal candidates for this application and a second order topology suitable for the current input was proposed. A new method of using dynamic reference method to tune the reference based on input signal was proposed in Chapter 3. This method provided improvement over existing solutions to address the issue of interfacing with wide-dynamic range inputs. Implementation of sub-blocks for the integrators, comparator and current DAC were discussed and techniques such as chopping was used to achieve the required noise specifications from the read-out circuit in Chapter 4. The current division between photodiode and read-out, due to the parasitic resistance of photodiode, showed us that the transconductance of the first integrator relied on this parameter and hence a sensor adaptable front-end biasing scheme was

included as a proof of concept and the results showed a power saving of 6 times.

Finally the chip has been measured and various test set-ups have been used to demonstrate the functionality of the design. It was shown that the achievable resolution of the implementation from measurements was limited to 10 bits. This result can be explained due to the higher output current noise (50 pA/$\sqrt{Hz}$ over 0.1 Hz to 10 Hz) in the Keithley SMU as compared to the required noise PSD of 2.1 pA/$\sqrt{Hz}$ which were the given specifications of the sensor. As a final step to further characterization, a proposal of using on-board higher resolution(18 bits) low-noise voltage DAC followed by a voltage to current converter was explained in Chapter 5 which was not completed in this work due to the limited time available for complete characterization. A demonstration of the optical-electrical interface showed the application of the circuit using a silicon photodiode.

6.2 Future improvements

At the overall architecture, concept of using an additional front-end current mirror needs to be investigated better to compare its achievable performance in terms of linearity and/or improvement of the performance of existing ADC design together with it. In our present results, we could achieve upto ± 10 LSB for 16 bits INL in case of simulation while the measurements with a larger thermal noise floor showed an achievable resolution of 10bits with ± 1 LSB INL. We clearly demonstrated, by employing two step process during measurements to show analytically the correlation between the measured performance of ADC and the noise PSD of the stimulus used. But there needs to be further understanding at the simulation level for the cause of non-linearity with the photodiode model. This could be due to the limited modeling of non-idealities in simulink for the interface (modulator together with the photodiode) architecture which showed a better performance. One reason why a more thorough analysis was not done was due to the inference that since both signal and feedback reference undergo same current division, the parasitic should not significantly affect our performance. This needs to be evaluated if the application

demands a more stringent linearity specifications. When dealing with high resolution read-out, calibration proves to be a useful technique to improve the performance. In our present case, this remains not explored in this work and could be useful to further improve the performance of the design.

A

Operation of the system

A.1 Control registers

The overall architecture consists of transmitter and the receiver circuits which needs to be controlled for each operation in the chip. Figure A.1 shows a representative timing diagram of the configuration for operation of the ADC.

The operation begins with the START signal which initiates the configuration of various registers. The DACVAL controls the current output from the laser drivers while DACSEL chooses the respective laser channel output through which the laser driver output is fed. LASERON controls the operation of the laser by switching ON and OFF the laser driver. On the receiver side PDSEL selects the multiplexed channel to be connected to one of the three read-out channels as was explained in Chapter 3. The determination of the signal involves difference of the signal plus dark current and the dark current. This can be noted in figure A.1, where during T2, T3, T4 cycles; the LASERON is kept low indicating determination of dark current while during the cycles from T5 until T8, the laser is switched ON and the read-out circuitry determines signal plus dark current. Before the beginning of every conversion, the ADC is reset by a short pulse on RST.

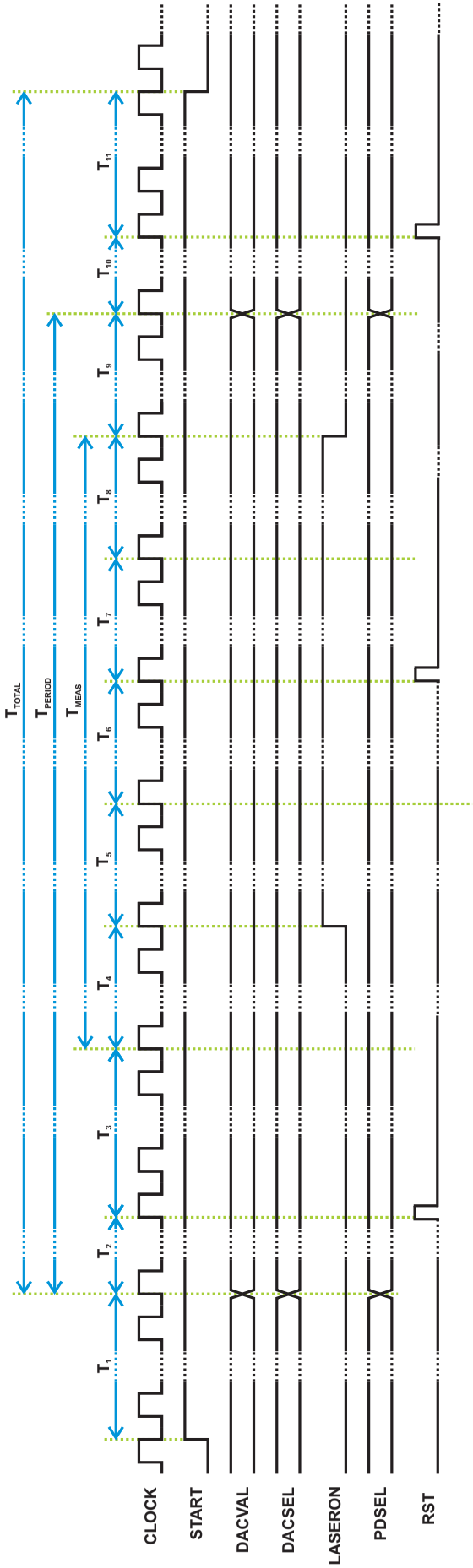

Figure A.1: Timing Operation of the Glucose Sensor

In order for the timing operation to be controlled, respective register bits for the controls explained in figure A.1 are provided within the glucosens chip. These are configured via SPI communication. The table A.1 shows the description of the registers.

DACLASER$< 0:9 >$ and DACTUNER$< 0:9 >$ represent the DACVAL for the respective transmitter channels. PDSEL$< 1:4 >$ and LASERSEL$< 1:5 >$ choose the respective photodiode to be read and laser to be driven. In order to be control the capacitor and resistor values forming the first integrator, to be close to the architecture coefficients in spite of statistical variations in implementation, CTUNE$< 1:4 >$ and RTUNE$< 1:4 >$ are provided. Each of the three read-out channels namely laser, input and reference can be reset by setting the RST_OTA1_LASER_REG, RST_OTA1_IN_REG and RST_OTA1_REF_REG. There is also provision to control the resetting via a pulse on a pin of the chip. PD_LOWPOWERMODE chooses the biasing scheme depending on the photodiode to be interfaced while PD_OTA1 is provided incase of complete power down of the read-out circuits.

Register	Description
DACLASER$< 0:9 >$	Control current output to the laser
DACTUNER$< 0:9 >$	Control the current output to the tuner
PDSEL$< 1:4 >$	Selection of the Photo-diode channel
PD_DAC$< 1:4 >$	Dynamic Reference control of the feedback DAC
LASERSEL$< 1:5 >$	Selection of the Laser channel
CTUNE$< 1:4 >$	Control to switch capacitors for first integrator
RTUNE$< 1:4 >$	Control to switch resistors for first integrator
SEL_TEST$< 0:1 >$	Selection of the debug test output
RST_OTA1_LASER_REG	Resetting the first OTA of the laser channel
RST_OTA1_IN_REG	Resetting the first OTA of the input channel
RST_OTA1_REF_REG	Resetting the first OTA of the reference channel
PD_LOWPOWERMODE	Choice of tail current bias
LASER_ON_REG	Register to control ON of laser
PD_OTA1	Power down for all the first OTA
LASER_10	Choice of 10mA or 100mA laser current

Table A.1: Registers to control the operation of the chip

The verification of the configuration is done by serially shifting the bits outside the chip. Figure A.2 shows the result for one such configuration during the measurement of the chip.

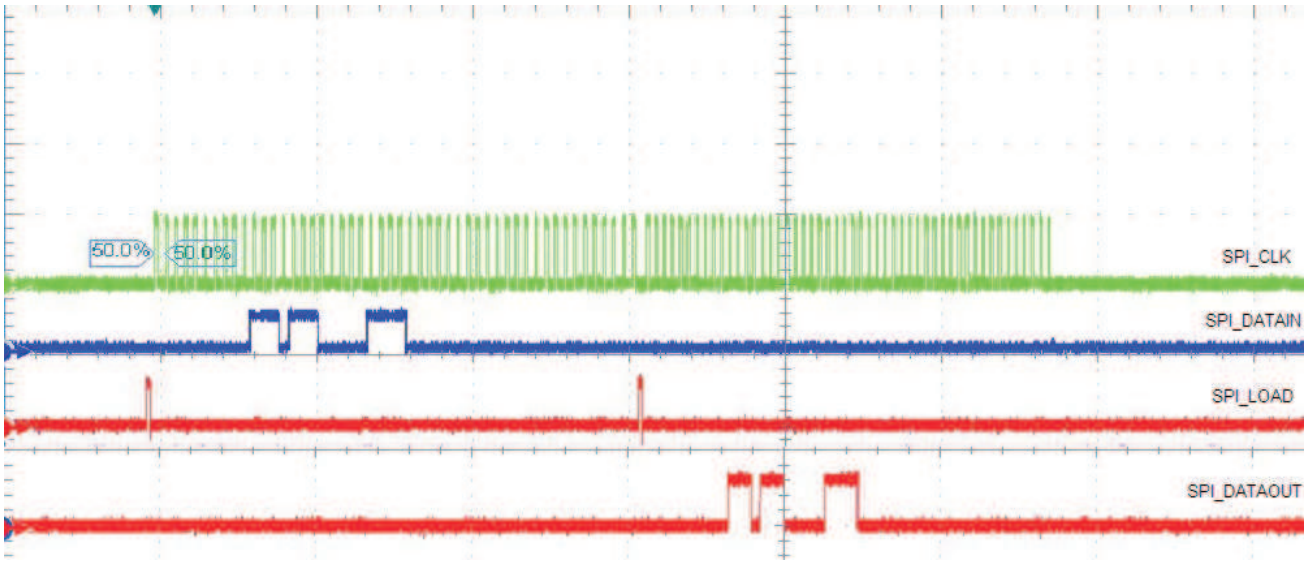

Figure A.2: Configuration of the chip during measurement

A.2 Operation control by microcontroller

The following represents the high-level flow for the control of operation of the chip by the external micro-controller. Together they form the sensor-system which conveys resulting data to the PC.

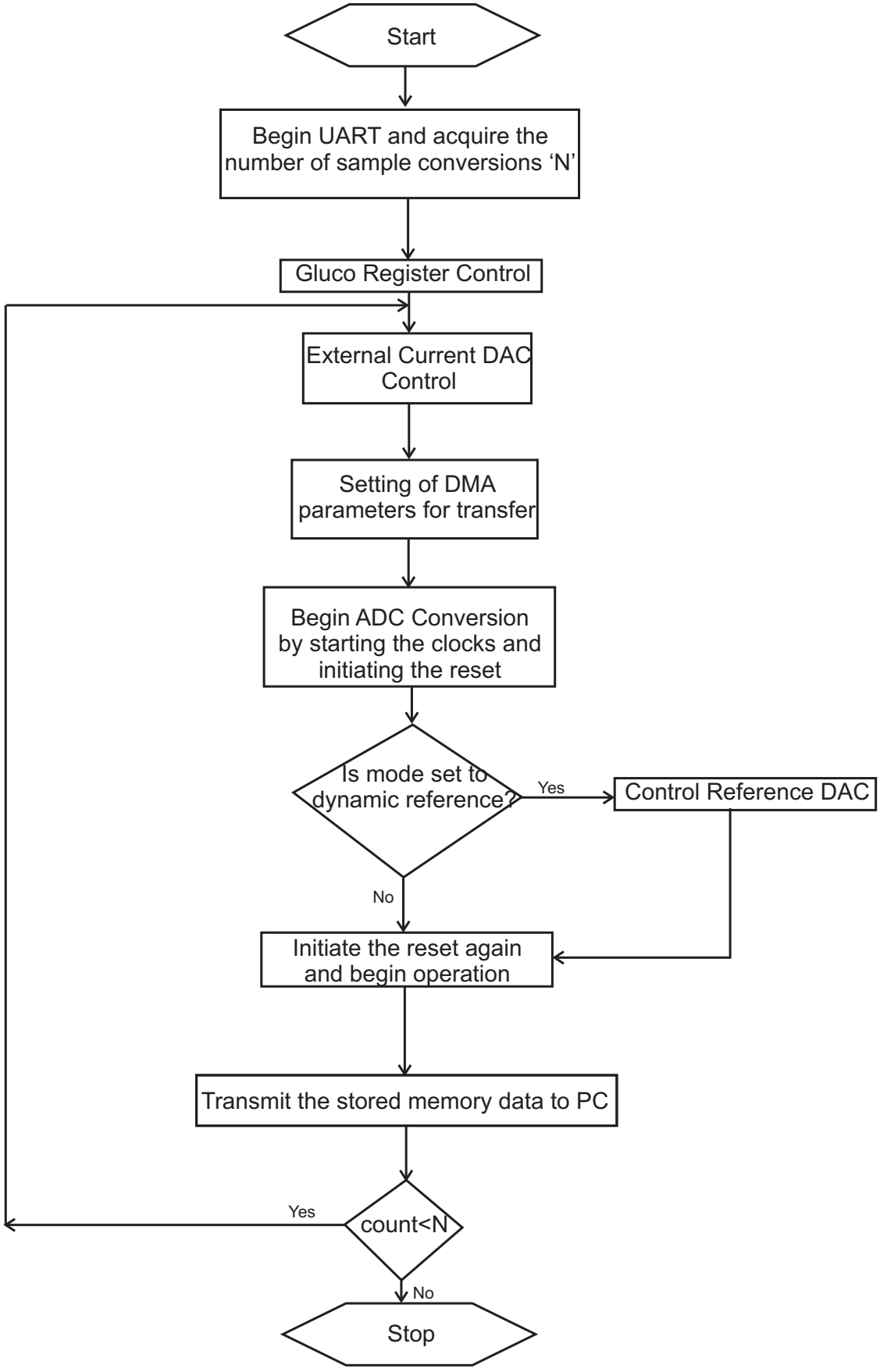

Figure A.3: Software for control of the overall sensor

B

Spectrum of the photodiode response

The results of transmission spectra measured for various wavelength can be seen in the figure B.1 and figure B.2 based on results from experiments for glucose and water molecules displacement. We note that glucose (signal channel in our design) and water (reference fluid channel) have a noticeable spectral signature which is characteristic in the first-overtone and combination band which were explained in section 1.

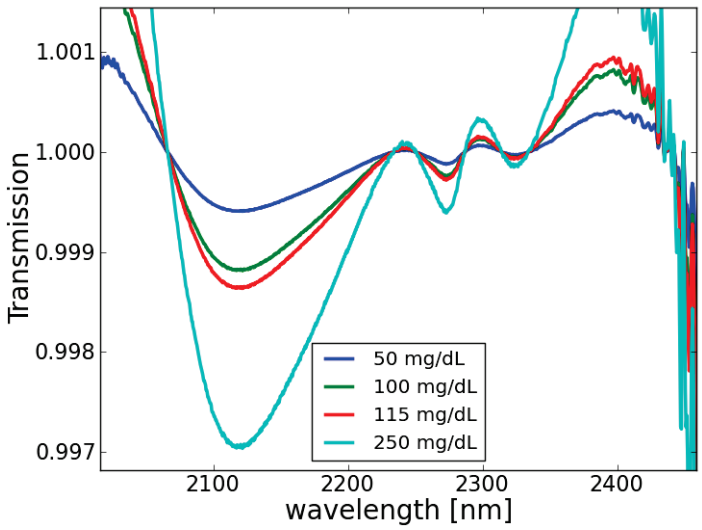

Figure B.1: Measured Transmission Spectra in combination band (Courtesy: Photonics group,Ghent University)

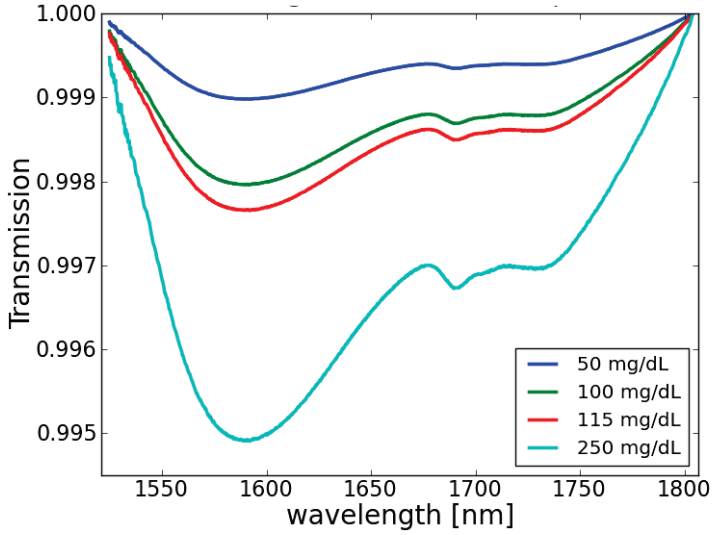

Figure B.2: Measured Transmission Spectra in first overtone band (Courtesy: Photonics group,Ghent University)

At some points in plot transmission is above 1, which is due to the strong absorption by water than glucose at certain wavelength whose effect is shown by this number [4]. The transmission will increase because the added glucose molecules will push away the water molecules with higher absorption.

C

Schematics of the test board

The schematic of the chip and the controller on the test PCB are shown in figuresC.1 and C.2.

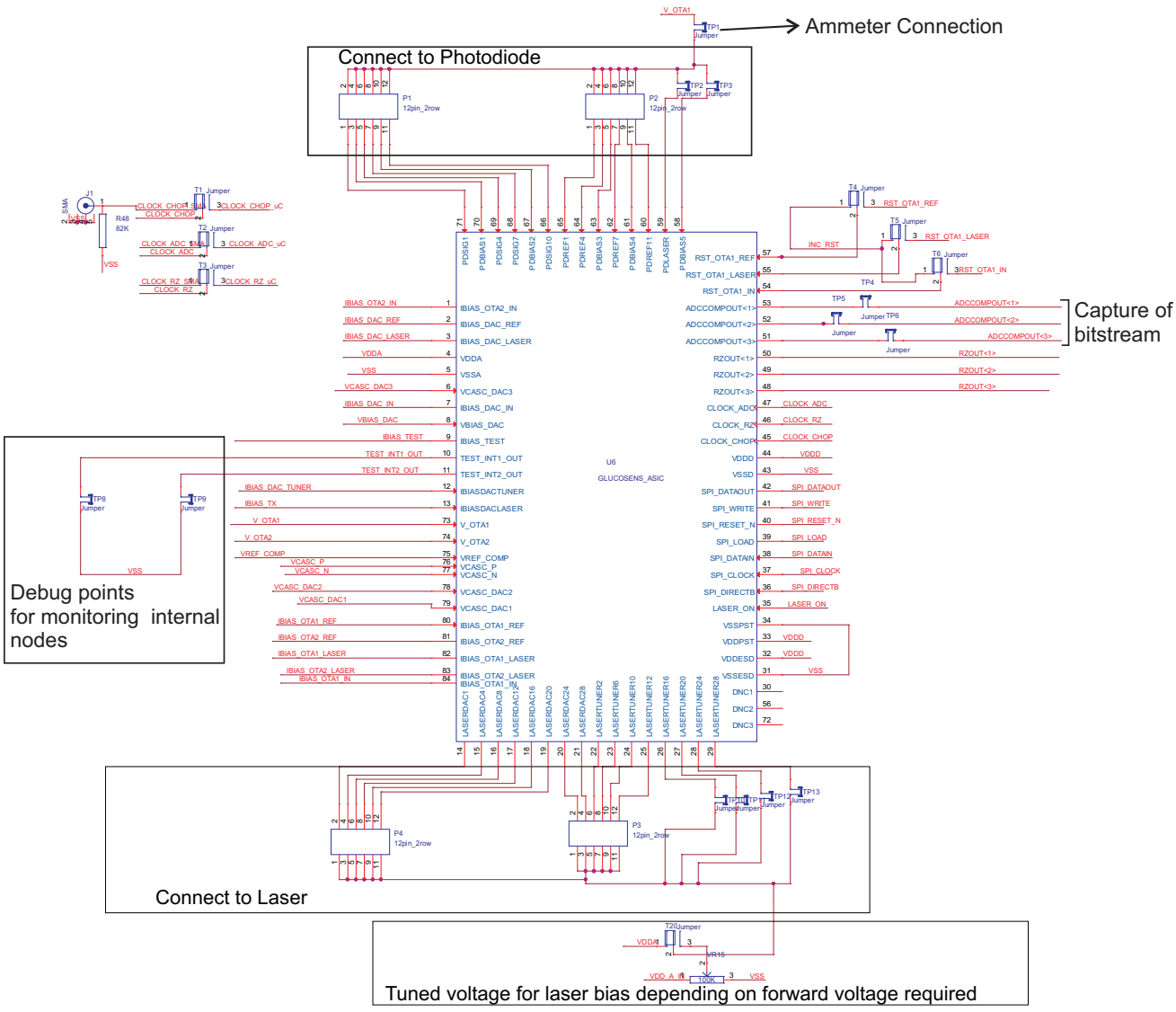

Figure C.1: Schematic of the chip connections on the PCB

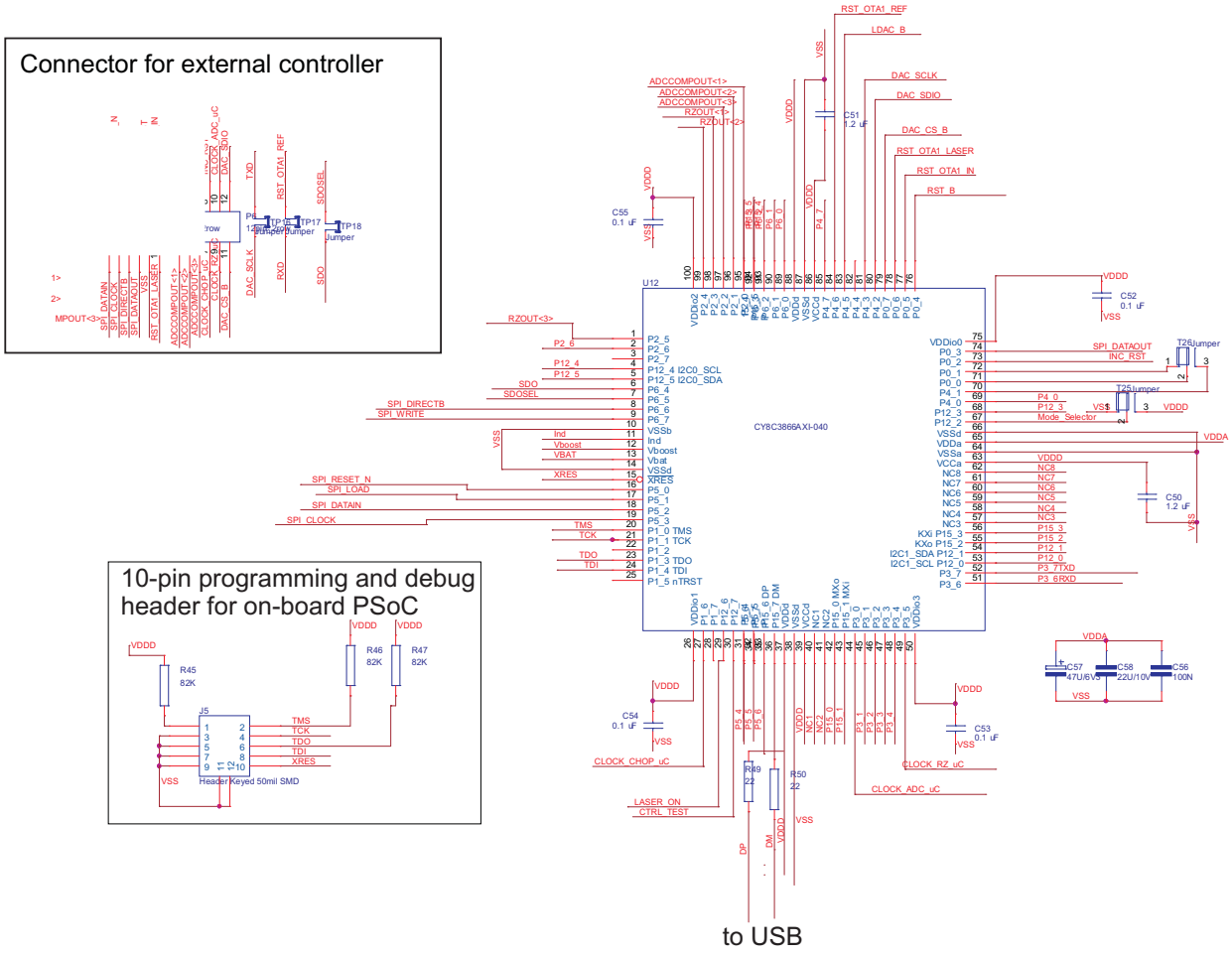

Figure C.2: Schematic of the controller on the PCB

Bibliography

[1] "Glucosens: Enabling technologies for continuous glucose monitoring using implantable single chip optical sensors," Proposal IWT, Tech. Rep., 2009.

[2] I. Koudar, "Balanced low noise high dynamic photodiode interface for automotive," in *Custom Integrated Circuits Conference, 2006. CICC '06. IEEE*, sept. 2006, pp. 579 –582.

[3] "Glucosens project website," www.glucosens.be.

[4] A. Amerov, J. Chen, W. Gary, and M. Arnold, "Scattering and absorption effects in the determination of glucose in whole blood by near-infrared spectroscopy," *Analytical chemistry*, vol. 77, no. 14, pp. 4587–4594, 2005.

[5] S. G. W. Arnold M. A., Olesberg J. T., *Near-Infrared Spectroscopy for Noninvasive Glucose Sensing, in In Vivo Glucose Sensing, Volume 174.* John Wiley and Sons, 2009.

[6] E. Ryckeboer, W. Bogaerts, and R. Baets, "Silicon photonics based evanescent sensor for absorption spectroscopy of glucose," in *XI Conference on Optical Chemical Sensors and biosensors (EUROPTRODE XI), Spain*, 2012.

[7] J. Goetz, M.J., G. Cote, R. Erckens, W. March, and M. Motamedi, "Application of a multivariate technique to raman spectra for quantification of body chemicals," *Biomedical Engineering, IEEE Transactions on*, vol. 42, no. 7, pp. 728 –731, july 1995.

[8] P. Rako, "Photodiode amplifiers: changing light to electricity," National Semiconductors, Tech. Rep., 2008.

[9] "ADC performance survey 1997-2012," B. Murmann, http://www.stanford.edu/~murmann/adcsurvey.html.

[10] H. Kulah and T. Akin, "A current mirroring integration based readout circuit for high performance infrared fpa applications," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, vol. 50, no. 4, pp. 181 – 186, apr 2003.

[11] D. A. Johns and K. Martin, *Analog Integrated Circuit Design.* John Wiley and Sons Inc., 1997.

[12] M. Alonso, R. del Ro, and J. Rosa, *Nanometer CMOS Sigma-Delta Modulators for Software Defined Radio.* Springer Publishing, 2011.

[13] M. Steyaert, *Continuous time Sigma-Delta Converters.* IMEC Academy, 2012.

[14] J. Markus, "Higher-order incremental delta-sigma analog-to-digital converters," Ph.D. dissertation, Budapest University of Technology and Economics), 2005.

[15] J. Hughes, A. Worapishet, and C. Toumazou, "Switched-capacitors versus switched-currents: a theoretical comparison [in cmos]," in *Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEEE International Symposium on*, vol. 2, 2000, pp. 409 –412 vol.2.

[16] R. Schreir and G. Temes, *Understanding Delta-Sigma Data Converters.* John Wiley and Sons Inc., 2005.

[17] M. A. P. Pertijs and J. H. Huijsing, *Precision Temperature Sensors in CMOS Technology.* Springer Publishers, 2006.

[18] H. J. Lee, "The effects of excess loop delay in continuous-time sigma-delta modulators," Master's thesis, MIT, 2005.

[19] B. Boser and B. Wooley, "The design of sigma-delta modulation analog-to-digital converters," *Solid-State Circuits, IEEE Journal of*, vol. 23, no. 6, pp. 1298 –1308, dec 1988.

[20] K. Souri, M. Kashmiri, and K. Makinwa, "A cmos temperature sensor with an energy-efficient zoom adc and an inaccuracy of±0.25 c (3s) from- 40 c to 125 c," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International*. IEEE, 2010, pp. 310–311.

[21] H. Lee, H. Lee, J. Woo, S. Kim, Y. Park, and S. Kim, "A CMOS readout integrated circuit with wide dynamic range for a CNT bio-sensor array system," in *Proceedings of the 17th IEEE/ACM international symposium on Low-power electronics and design*. IEEE Press, 2011, pp. 357–360.

[22] J. Morizio, M. Hoke, S. Tucker, and E. Danford, "Programmable dynamic range $\sigma\delta$ converter," US Patent 6255974, 2001.

[23] C. Ji and J. Tyrrell, "Infrared photocurrent front-end adc for rain-sensing system with ambient light compensation," US Patent 8097853, 2012.

[24] B. Murmann, *Course Reader EE214B, Advanced Analog Integrated Circuit Design*. Stanford University, 2012.

[25] C. Enz and G. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization," *Proceedings of the IEEE*, vol. 84, no. 11, pp. 1584 –1614, nov 1996.

[26] A. Yukawa, "A CMOS 8-bit High-Speed A/D Converter IC," *Solid-State Circuits, IEEE Journal of*, vol. 20, no. 3, pp. 775 –779, june 1985.

[27] B. Wicht, T. Nirschl, and D. Schmitt-Landsiedel, "Yield and speed optimization of a latch-type voltage sense amplifier," *Solid-State Circuits, IEEE Journal of*, vol. 39, no. 7, pp. 1148 – 1158, july 2004.

[28] D. Schinkel, E. Mensink, E. Kiumperink, E. van Tuijl, and B. Nauta, "A double-tail latch-type voltage sense amplifier with 18ps setup+hold time," in *Solid-State Circuits Conference, 2007. ISSCC 2007. Digest of Technical Papers. IEEE International*, feb. 2007, pp. 314 –605.

[29] J. A. Cherry, "Theory, practice, and fundamental performance limits of high-speed data conversion using continuous-time delta-sigma modulators," Ph.D. dissertation, Carleton University, 1998.

[30] R. A. Hastings, *The art of analog layout.* Pearson Prentice Hall, 2006.

[31] "Model 2602 dual-channel system sourcemeter instrument datashee."

[32] "Bpw34fa data sheet," Osram GmbH, http://www.farnell.com/datasheets/1672033.pdf.

[33] H. Johnson and M. Graham, *High-Speed Digital Design : A handbook of black magic.* Prentice Hall, 1993.

D

Acknowledgements

It was about 3 years ago that I had planned on pursuing graduate studies and looking back it has been an enriching experience. All this was due to many people who made this journey possible and enjoyable. I would like to thank my advisor, Dr.Michiel Pertijs. I remember our first email interaction which began before I applied to the MSc program at Delft and since then our association continued during the course, internship and finally the Master Thesis project. He has been supportive and encouraging through out my studies, both inspiring me to set targets while also helping me decide at important points. His valuable inputs,patience and regular feedback through out my studies have been crucial for my understanding of analog circuit design as well as aspects of conducting quality research. It has been inspiring to have worked under his guidance during this period.

I thank my daily supervisor Dr.David San Segundo, who provided me an opportunity to work on the Glucosens project for my Master thesis at IMEC. It has been a great opportunity for me to work under his guidance at IMEC. He was always patient and supportive whenever I had anything to discuss and was welcoming all the time (at some phases, even during his vacations). He provided a wide scope, not limited by the project, for me to experiment and try different ideas during the course of my project which helped me appreciate the process of design. His inputs during the beginning of project on understanding of photodiode read-outs have been useful for me to appreciate the optimization involved both at circuit and

system level in such implementations. During the measurement phase, he always filled me with enthusiasm and confidence every day. I have learnt many things from him especially how to look at a problem from different perspective and to approach things in systematic and structured manner which were useful. It has been a memorable experience at IMEC and an important step for my career ahead.I would like to acknowledge the support and discussions with Ronny, Wim, Nannicha, Eva from Ghent University on photonics which made this work complete towards addressing the interface better. I also thank Georges, who was part of the project earlier and helped in the beginning with understanding of the system.

I thank Dr. ir. Reinoud Wolffenbuttel and Prof. dr. Edoardo Charbon who agreed to be on the defense committee. It is an honor to be able to have such experts of different domains in the panel for this project. I also would like to thank Prof. dr. Kofi Makinwa for the support during courses as well as at the Electronic Instrumentation Laboratory.

IMEC has been a great learning place for me due to both the facilities it offered as well as some of the amazing people I met. I would like to thank Dr. Firat Yazicioglu for providing every support within the group for this project as well as being encouraging and advising me whenever I approached him with questions. I would like to thank my colleagues at IMEC who were helpful and provided a very interesting work environment which made me look forward to work every single day. I would like to express my gratitude to Dr. Alonso Morgado who has been a good friend and the various coffee,lab dinner, weekend tape-out mode time spent were enjoyable due to his company. I could always bounce ideas of him and expect very critical while supportive remarks which helped me improve during course of time. Our joking story of 20 years ahead of state of the art remains unsolved and may be will inspire me to perform better ahead. I would like to thank Jan Putzeys for all his support with the lab set-up and measurements. His inputs during the debug phase and tips for the measurement and acquisition were very valuable during the bring-up phase. I like to thank Nick, Srinjoy, Long, Ybe and all other members

of the bio-medical circuits group for technical discussions and inputs. Thanks to Kiki for help and sharing the photo-diodes for the tests. I also like to thank all my friends from the student-lab who always were happy to see me knock on their doors for discussions on and off the topic of electronics. Thanks also to Dr. Guy Meynants, Gavril Arsinte who have been helpful during my earlier stay in Belgium as well as Viktor, Mukul Sarkar who helped during my transitioning to Leuven.

The first year at Delft provided me courses which were valuable towards my understanding of various concepts. They have motivated me to work in this direction and I would like to thank all the professors for those courses. I thank Dr. Nick van der Meijs for giving me opportunity to be assistant for the course on Digital IC Design. I wish to thank all my friends from whom I learnt during that period as well as through team project. I wish to thank Jianghai He who is a good friend and supported me in many ways throughout the last 2.5 years. The countless discussions, dinner and time spent at the EWI building will be memorable moments for me. I thank my friends Prashanth, Renil, Bhaskar, Chetna and Brhamesh who made the stay at Roland Holstlaan enjoyable with the weekly dinners and discussions. I also thank Esther and Frank Buizer who have been good friends and like a family in Netherlands for me. The times during christmas at their home will be cherished by me and also the support they provided in many ways while I am away from Netherlands during thesis was very helpful. I acknowledge the scholarship support by Delft University during the two years in Netherlands. This work was funded by IWT under the Glucosens project. I wish to thank IWT, IMEC and KU Leuven for the same. I also thank Jan de Vries from the international office for helping with administration and support for my study abroad.

This journey would not have reached so far or never have begun without the amount of support provided by my parents whose many sacrifices helped me reach so far. They have stood by me and provided everything I could have asked for. The confidence and encouragement from my father has always been the strength for me to dream further. I especially thank my mother who always made everyday

beautiful due to the morning call. I would like to thank my sister for being there for me. Also thanks to my grandmother and the rest of my family who always cared for me.

Umanath Kamath