High-temperature CVD silicon on ceramic substrates for solar cell applications

Ad van Zutphen
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Cover:
Selective area diffraction pattern of a polycrystalline film-silicon layer on a thermally oxidized silicon wafer. This diffraction pattern is recorded during a transmission electron microscopy analysis performed at the National Centre for HREM at Delft University of Technology.
High-temperature CVD silicon on ceramic substrates for solar cell applications

Proefschrift

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus prof. ir. K.F. Wakker,
voorzitter van het College voor Promoties,
in het openbaar te verdedigen op 17 september 2001 om 13.30 uur

door
Adrianus Johannes Martinus Maria van ZUTPHEN

Landbouwkundig ingenieur

Geboren te Veghel
Dit proefschrift is goedgekeurd door de promotoren:
Prof. dr. C.I.M. Beenakker
Prof. dr. W.C. Sinke

Samenstelling promotiecommissie:

De Rector Magnificus, voorzitter
Prof. dr. C.I.M. Beenakker, promotor
Prof. dr. W.C. Sinke, promotor
Prof. dr. J. Schoonman
Prof. dr. F.H.P.M. Habraken
Prof. dr. R van de Sanden
Prof. ir. L. van der Sluis
Dr. M. Zeman

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The work described in this thesis was supported by the "Netherlands Agency for Energy and the Environment" (NOVEM) and the Delft University of Technology.

ISBN: 90-90144-77-3

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PRINTED IN THE NETHERLANDS
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Chapter 1

Introduction

1.1 Solar radiation as an alternative source of energy
1.2 Industrial silicon solar cells
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1.4 Film-silicon deposition methods
1.5 Scope and outline of this thesis
1.6 References

This thesis deals with research on thermal chemical vapour deposition of films of polycrystalline silicon on different types of substrates. The study forms part of a larger research effort aimed at the realization of cost-effective solar cells based on thin layers of crystalline silicon. This chapter gives a general introduction to solar energy as an alternative energy resource and it presents current solar cell technologies and the state-of-the-art in film-silicon solar cell technology.
1.1 Solar radiation as an alternative source of energy

The world consumption of energy is increasing year after year. The overview from ref. [1] in Figure 1.1 shows that at present most energy is produced using fossil resources (oil, gas and coal), nuclear resources and hydropower.

![Diagram showing energy production from 1860 to 2060](image)

**Figure 1.1:** Development of the global energy production from 1860 to 2060. The estimations are based on the scenario of a sustained growth of the energy consumption (after [1], 1 exajoule = 3 * 10^{11} kWh).

The fossil resources, which form the major part of all resources, are exhaustible, and their use pollutes the environment. Awareness of these problems has given a strong impulse to the search for alternative sources of energy. Possibilities for future energy production can be found in sustainable sources of energy, which include wind energy, solar energy, geothermal energy and energy from biomass. In this introduction, we focus only on solar energy.

The energy the sun irradiates to the earth is about 1 * 10^{18} kWh per year. This is roughly 10000 times more than the present annual world consumption of energy. The irradiated energy can be used either actively or passively. Passive methods require no special systems to take advantage of the irradiated sunlight and are often used to heat
buildings. In this case architecture plays an important role in constructing buildings and their surroundings for optimal use of incident sunlight. Active methods involve the use of special systems to convert sunlight into a usable form of energy. These special systems are divided into two groups: solar thermal systems and solar cells. Examples of the solar thermal systems are collectors, which operate at low temperature for water and space heating and systems operating at high temperature for electricity generating purposes. Solar cells are able to convert the incident light directly into electricity. The basic process involved is called the photovoltaic effect. No moving parts are involved; no waste products and no noise are formed during normal use. Therefore, photovoltaic energy can be considered a clean source of energy if the following conditions are fulfilled: (1) the materials used for the solar cell must be environmentally harmless, and (2) the production process of the solar cells must use significantly less energy than the energy the solar cells themselves generate during their operational lifetime. Since, on the time scale of human evolution, the supply of sunlight is eternal, the sun can be considered as an unlimited source of energy.

For almost every application, a number of solar cells are encapsulated in solar modules. This encapsulation will protect the fragile solar cells from atmospheric and mechanical damage. The modules can be used separately or can be placed in arrays. Dependent on the application, custom-designed large systems can be made with these modular arrays. About 40% of the total costs of a complete solar electricity system are the costs of solar cells [2]. The remaining parts of the costs are due to module production, inverters, installation and maintenance. So a reduction in the production costs of solar cells will reduce the total system costs and thus the cost of solar electricity.

Due to the increased recognition of the potential of solar irradiation as an alternative source of energy, the investments in terrestrial installation of photovoltaic systems increase. Two major groups of applications can be distinguished, each with their own balance of system. The first one is the field of stand-alone or off-grid systems, for which photovoltaic systems have proven to be an adequate solution to provide reliable, custom-made and clean energy. Costs per kWh are not the most important factor in this case, but the possibility to provide a reliable energy service. For the second application, the grid-connected
power supply, the costs per unit of solar electricity are still too high. To allow competition with conventional sources of energy, the costs of the photovoltaic system and its components must be lowered; only this enables large-scale use.

1.2 Industrial silicon solar cells

The first crystalline silicon solar cell was developed in 1954 by Chapin et al. at the Bell Laboratories in the USA; it had an efficiency of 6% [3]. This efficiency was increased to 10% within a few years. In the following years, solar cells were mainly developed and produced for space applications. The oil crisis in the beginning of the 1970s and the awareness that fossil fuel sources were limited generated renewed interest in solar cell technology. Since then tremendous progress has been made in increasing the efficiency and in reducing costs. Since the 1980s solar power for the grid-connected systems became of more interest and the shipments of solar modules have increased tremendously (Figure 1.2).

![Graph showing the increase in global shipment of photovoltaic modules from 1982 to 2000.]

**Figure 1.2:** Global shipment of photovoltaic modules [4,5].

The present production of solar cells is for more than 98% based on silicon and silicon is expected to be the major material for solar cells for the near future as well [5]. The present market for silicon solar cells can be divided in solar cells based on crystalline bulk material, constituting about 87% of the PV-market share and those based on a thin-film
approach, today mainly amorphous silicon and constituting about 12% of the PV-market (Figure 1.3).

Figure 1.3: Solar cell production shares of different technologies in 1999 [5].

Figure 1.4 presents an overview of this silicon solar cell market, based on structure of the material, which is either crystalline or amorphous.

Figure 1.4: Overview of the present silicon solar cell market based on silicon material used [6].

The market of crystalline silicon solar cells is further subdivided into single or mono-crystalline silicon share, a multi-crystalline silicon share and a small share of ribbons.

The traditional monocristalline silicon materials are produced by Czochralski or float zone crystallization [2]. The advantage of using this material for solar cells is the relatively high efficiency obtained using simple cell processing. At a laboratory scale cell efficiencies of 24.7% and module efficiencies of 22.7% have been achieved [7]. A disadvantage is the higher wafer price due to the high thermal energy budget of the production process. In addition, valuable silicon is wasted
Introduction

when the rods are sawn in wafers and when the circular wafers are cut to become square. After the ingots have been sawn, the silicon wasted by sawing cannot be used directly since it has to be purified again.

Multicrystalline silicon is produced by casting processes [2,8]. Casting produces evidently cheaper crystalline wafer materials, due to higher throughput and up-scaling possibilities. Also in this case, valuable silicon is wasted during the process of sawing the ingots. Compared to the monocrystalline silicon solar cells, lower cell efficiencies are obtained. At a laboratory scale cell efficiencies of 19.8 % and module efficiencies of 15.3 % are achieved [7].

The loss of silicon during the sawing process is one of the drawbacks of both monocrystalline and multicrystalline silicon wafers. This was decreased by the development of multi-wire sawing processes, in which less material is lost and in which thinner wafers could be sawn, which gives the possibility of a more efficient use of the ingot. Also methods to produce crystalline wafers without a sawing process have been developed. Several technologies have been developed to produce sheet or ribbon material, but only a few left the laboratory scale successfully [9]. Two of those processes will be reviewed briefly. The Edge defined Film Growth (EFG) process consists of drawing an octagonal tube from a silicon melt using suitable templates. Laser cutting is used to separate the tubes into individual wafers. Cell efficiencies of 14.5 % have been reported [10]. Another sheet process is the Ribbon Growth on Substrate (RGS) process. This process is characterized by a moving support or substrate, which is pulled across a silicon melt, so that silicon solidifies on the substrate. After solidification, the support or substrate is removed, leaving a sheet of silicon. Cell efficiencies of 11% have been reported [11]. Both processes produce polycrystalline material, as in cast silicon.

All three described types of bulk crystalline silicon solar cells suffer from the lack of the availability of feedstock material, which is at present mainly scrap of the IC industry. The shortage of feedstock may even raise the cost of the solar cells. Possible solutions to this problem are increasing the production capacity of solar grade silicon and/or reducing the silicon consumption per Wp of the solar cell.
1.3 Film-silicon solar cells

Besides the optimised sawing process, an additional reduction of the amount of silicon needed for the silicon solar cell fabrication process can be achieved by decreasing the thickness of the solar cell. It has already been demonstrated that cells with a thickness between 30 and 50 μm can deliver efficiencies between 11 and 21.5 % [7] dependent on the fabrication method. To reach these (relatively) high efficiency values, fine-tuning of the cell using light-trapping schemes and reduction of recombination processes are necessary. Light trapping is often achieved by texturing or roughening the front and back surface of the active layer. A rough surface is able to scatter the incident light, which can result in total capture of the incident light in the film-silicon layer.

The term film-silicon (f-Si) covers the broad range of all silicon layers deposited on a substrate. The thickness of these deposited layers range from 1 – 100 μm. Due to the reduced thickness, the f-Si solar cells are normally not self-supporting. To overcome this problem, the films are supported by a substrate. Additional to the reduced amount of valuable silicon, most f-Si techniques have the potential to become a large-area technology, which is advantageous in reducing costs. A schematic drawing of the base structure of a f-Si solar cell is presented in Figure 1.5.

![Figure 1.5: Schematic drawing of the base structure of a film-silicon solar cell.](image)

In general the active layer of a f-Si solar cell will have a thickness between 10 and 50 μm, which is roughly 10 % of the thickness used in bulk crystalline silicon technologies. The basic device structure of the solar cell on the substrate is similar to the crystalline solar cells: a pn-
Introduction

Junction. In general, the fabrication of the solar cell on the substrate starts with the deposition of a p-type silicon layer. To form the pn-junction n-type dopant will be introduced. Dependent on the final device structure, the substrate may have to serve as a contact. In this case, the material of the substrate has to be conductive. Besides this two-sided contact device, a device can be produced that has all contacts on one side of the cell. This device is easier to incorporate in a module than a two-side contacted solar cell. However the fabrication of such a device is much more complicated, since localized processing is required.

1.4 Film-silicon deposition methods

The methods to deposit films of silicon on a substrate can roughly be divided in low-temperature ($T_{\text{substrate}} < 650 \, ^\circ C$) and high-temperature ($T_{\text{substrate}} > 800 \, ^\circ C$) methods. All techniques in the low-temperature deposition regime require an additional source of energy, e.g. a hot wire, plasma or an ion gun. These additional sources are necessary to reach economically attractive deposition rates of several micrometers per minute. In the high-temperature techniques, heat itself or a difference in temperature is the driving force. A selection of both high-temperature as well as low-temperature deposition methods will be reviewed briefly in this section. This selection is based on methods that are currently evaluated in both national and European projects.

Liquid-Phase Epitaxy (LPE) is based on precipitation of silicon from a melt on a substrate. Silicon precipitates when the temperature of the silicon/metal melt is lowered. Dependent on the materials of the melt, temperatures between 800 and 1000 °C are used. This technique gives excellent results when the film is grown in a homo-epitaxial situation (deposition of a material on a substrate made of the same material). However, when hetero-epitaxy (deposition of a material on a different material) is desired, formation of a dense and compact film is quite difficult. It is not easy to form nuclei on a foreign substrate. The term 'foreign' covers the range of non-(crystalline) silicon materials. In many cases the adhesion of the precipitated silicon to the substrate is poor. In addition, there is an anisotropy in the growth speed during the formation of the film, which is therefore not homogeneous in thickness [12]. Normal LPE systems are not suitable for continuous production
process. This has been improved in the Temperature Difference Method (TDM), which is based on LPE [13]. In this case the temperature difference is not reduced by lowering the temperature of the melt, but by applying a spatial temperature difference across the melt. The substrate is placed at the position with the lowest temperature of the system.

A technique commonly used for deposition of silicon in the IC technology is thermal chemical vapour deposition [14]. Silicon is deposited by pyrolytic decomposition of a gaseous precursor at temperatures between 800 and 1200 °C. When a crystalline silicon substrate is used, epitaxial deposition on the existing crystal of the substrate will occur. Deposition rates of up to 5 μm/min have been reported. Although rather complex equipment is used, the technology is well established and is used worldwide for epitaxial deposition of electronic-grade silicon for the IC industry. It is flexible in controlling electrical properties of the silicon film by just varying the composition of the gaseous reaction mixture. In general, deposition on foreign substrates results in fine-grained polycrystalline material, homogeneously covering the whole substrate.

A method to deposit both amorphous and polycrystalline silicon at low temperatures is Hot-Wire Chemical Vapour Deposition (HWCVD). The source that initiates the deposition reaction is a heated tungsten or tantalum filament. Deposition rates of 0.3 μm/min. have been reported by Matsumura [15]. He showed that the dissociation of the precursor at the tungsten filament is a catalytic process and called the method cat-CVD. The substrate is kept at relatively low temperatures ranging from 200 to 600 °C. This relatively low temperature enlarges the choice of suitable substrates. Despite the low substrate temperatures, also low-pressure conditions are required. In general, the use of high-vacuum equipment is less desirable for industrial processes, because of the cost associated with this equipment.

A new approach for f-Si deposition is the plasma spray method [16]. Silicon powder is fed into a plasma torch and sprayed onto a substrate. The substrate can be kept at every desired temperature. However, a high substrate temperature (1000 to 1200 °C) is necessary to ensure the best quality of the film. Deposition rates of 10 μm/sec have been reported. In general, relatively high concentrations of metallic impurities can be detected in the deposited films. These impurities are either due to the
contact with the plasma torch or due to impure starting powder. The impurities will directly influence the electronic quality of the deposited film. This technique also requires vacuum equipment.

All described methods deposit fine-grained polycrystalline silicon on foreign substrates. This material mostly shows relatively short minority carrier lifetimes compared to multi- or monocrystalline silicon material. Since the solar cell used is a diffusion device, enhancement of the electronic properties is desired to obtain reasonable efficiencies. In general, enlargement of the crystal grain size increases the average carrier lifetime. Zone melting recrystallization (ZMR) at 1420 °C is often used to convert the fine-grained material into large-grain material [17]. ZMR is feasible to increase the efficiency of a f-Si solar cell, but requires several additional steps e.g., deposition of a silicon oxide capping layer, the ZMR process itself and at least two etching processes. Therefore, the addition of ZMR to a solar cell production process is still doubtful, since its additional steps will increase the total cost of the final solar cell.

1.5 Scope and outline of this thesis

This thesis will report on the investigations of thermal chemical vapour deposition of silicon on several types of specially developed ceramic substrates. The research is part of both national and European projects aimed at the realization of cost-effective solar cells based on polycrystalline f-Si layers on substrates.

The substrates have been developed for high-temperature deposition methods such as LPE and thermal CVD. In this research, all developed substrates are tested on their suitability in a thermal CVD process. The general aim of this research is to obtain a deposition process using thermal CVD of compact silicon films on the selected ceramic substrates. Initially, emphasis is put on the structure of the deposited film and not on the electronic properties of the deposited material. In addition, a crystallite size as large as possible is desired, to meet some of the criteria for electronic properties needed for photovoltaic conversion. Chapter 2 gives a brief overview of the CVD equipment and procedures used. Chapter 3 briefly discusses the substrates we used. In addition, the results of depositions on these substrates are presented and the selection is refined. Whisker formation was noticed on some of
the substrates used. Some methods to reduce this formation were tested successfully and are described.

When a compact film could be deposited, the morphological properties of the film-silicon layer were analysed more extensively. Chapter 4 reports on a more extensive research on the structure of the film using TEM and XRD analysis methods. Chapter 5 reports on a simulation study on f-Si solar cells. Computer simulations have been used to gain more understanding of device design issues and physics of f-Si solar cells. The first results of f-Si solar cells on ceramic substrates are reported in Chapter 6. To conclude this thesis Chapter 7 summarises the main conclusions of our research.

1.6 References


Introduction


Introduction
Chapter 2

Thermal chemical vapour deposition of film-silicon

2.1 Thermal chemical vapour deposition
2.2 Description of the reactor
2.3 Standard characterization methods
2.4 References

The aim of this chapter is to give an introduction to the thermal chemical vapour deposition process, which was used in this work. The CVD-reactor and deposition processes used are described in more detail and the standard measurement methods for sample characterization are presented.
2.1 Thermal chemical vapour deposition

Chemical vapour deposition (CVD) is the formation of stable solids by decomposition of gaseous chemicals using heat, plasma, ultraviolet or other energy sources or a combination of sources [1]. In our case the reaction is initiated by heat and therefore we use the term thermal CVD. The chemical reactions usually take place at or near the heated deposition surface in the so-called boundary layer. Thermal CVD is used worldwide for epitaxial growth of electronic grade silicon in the IC industry. Four silicon source gases are commonly used for chemical vapour deposition: silane (SiH₄), dichlorosilane (SiH₂Cl₂), trichlorosilane (SiHCl₃) and tetrachlorosilane (SiCl₄) [2]. We used dichlorosilane (DCS), since it is the standard silicon source gas used in the DIMES process infrastructure.

The overall deposition process can be viewed as the sum of a series of microscopic steps. Figure 2.1 presents schematically the basic steps involved.

![Diagram](image)

Figure 2.1: Schematic representation of thermal chemical deposition process with dichlorosilane.

First, the dichlorosilane is introduced into the reaction chamber by means of forced convection and flows to the vicinity of the wafer. It approaches the wafer as it diffuses through the boundary layer near the wafer and may decompose partially or completely in the gas phase. When the reaction intermediates react on the wafer surface, they adsorb and diffuse on the surface before completely decomposing to silicon and hydrochloric acid. The resulting silicon atoms diffuse to stable sites.
where they either start nucleation or are incorporated in an existing matrix.

The basic chemistry involved in growth of silicon from DCS consists of three steps [3]:

1. Thermal decomposition of the input gas:

   \[ \text{SiH}_2\text{Cl}_2 \leftrightarrow \text{SiCl}_2 + \text{H}_2 \]  
   \[ (2.1) \]

2. Adsorption to surface:

   \[ \text{SiCl}_2 + s \leftrightarrow \text{SiCl}_2 \cdot s \]  
   \[ (2.2) \]

where \( s \) is an active site on the surface. The reaction intermediates adsorb preferentially on sites of reduced surface energy.

3. Surface reaction where silicon is incorporated:

   \[ \text{SiCl}_2 \cdot s + \text{H}_2 \leftrightarrow \text{Si}(s) + 2\text{HCl} \]  
   \[ (2.3) \]

This reaction is assumed to be the rate-controlling step in the deposition process, while the others are assumed to reach equilibrium fast [4]. Figure 2.2 shows a graph with the deposition rate of monocrystalline silicon versus the temperature in the reactor used for this research.

![Graph showing deposition rate vs. temperature](image)

**Figure 2.2:** The deposition rate of monocrystalline silicon in the reactor used for this research at several temperatures.
Thermal chemical vapour deposition of film silicon

This graph is characteristic for deposition of monocristalline silicon using thermal CVD [1,3]. At lower temperatures the deposition rate is kinetically controlled according to reaction R2.3; this will be referred to the temperature-controlled reaction regime. The growth rate is strongly dependent on the temperature and follows an exponential law: 
\[ r \propto \exp\left(-\frac{E_a}{kT}\right) \], with \( E_a = 1.4 - 1.7 \text{ eV} \). At higher temperatures, the temperature dependence is much smaller. In this regime the gas-phase diffusion of reactants to the surface is the limiting factor of the growth rate and therefore this regime will be referred to as the diffusion-controlled reaction regime.

Reaction R2.3 is reversible and by adding HCl to the reaction mixture one can shift the equilibrium of the reaction. If enough HCl is added to the system at a given pressure and temperature, silicon etching occurs.

\[ 2.2 \text{ Description of the reactor} \]

\[ 2.2.1 \text{ The reactor chamber} \]

For deposition of polycrystalline silicon the cold-wall epitaxial reactor, Gemini-1 from the Huettinger Company was used. This commercial reactor is designed to be used for IC production. In this reactor the wafers are placed on a flat supporting plate, the susceptor, which is heated by radio-frequency (RF) induction. This susceptor is fabricated from high-purity graphite covered with a silicon carbide coating. The RF-energy couples to the supporting susceptor, but not to the quartz walls of the deposition chamber, which remain relatively cool. The gas mixture enters the chamber through the centre of the susceptor. It flows in the space above the susceptor and flows downward to the wafers and exhaust. A small partial pressure of the reactant gas, SiH₂Cl₂ (DCS), is added to the large flow of the carrier gas hydrogen. All depositions were carried out at atmospheric pressure. In one run, up to 10 wafers with a diameter of 100 mm could be processed. The wafers are placed in the recessed pockets. All ceramic samples were placed on the supporting wafers in the pocket. Figure 2.3 presents a picture of the chamber of the reactor.
The susceptor requires periodic etching to remove excess silicon deposits. Etching is performed using HCl at 1150 °C. After etching the susceptor is coated with a silicon layer using a standard procedure.

![Diagram of reactor](image)

**Figure 2.3:** Schematic drawings of the reactor used.

### 2.2.2 Gas flow control system

This system is isolated from the electronics in a self-contained modular unit located in the rear top compartment of the control cabinet. It includes standard flows for N\textsubscript{2}/H\textsubscript{2}, DCS, HCl and diluted diboran (B\textsubscript{2}H\textsubscript{6}) dopant precursor gas. Precision automatic flow controllers control all flows. Flow rates are displayed on the process control panel. On/off gas control is regulated by pneumatically activated Nupro\textsuperscript{®} valves. Digital potentiometers on the main control panel adjust the flow rates. These can be set from 0.0 to 99.9% of a maximum value using a thumbwheel [5].

### 2.2.3 Dopant control system

In order to dope the epitaxial layer a dopant source gas is added to the mainstream of gases. The ratio of dopant source gas flow and silicon source gas flow is an important factor in determining the concentration of the dopant in the deposited layer. The dopant supply must be diluted before it joins the mainstream to obtain the desired concentration relative to the silicon source gas. A scheme of the used dopant dilution system is presented in Figure 2.4:
Thermal chemical vapour deposition of film silicon

Figure 2.4: Schematic drawing of dopant dilution system of the Gemini-1 reactor.

The $\text{H}_2$ is added from a controlled pressure source to the dopant flow from the "source" mass flow controller. The combined gas flows pass through a gas mixer and are directed to "inject" and "diluent" flow controllers. The inject flow is directed to the reactor main stream or to the venting system and the dilute flow goes directly to the venting system.

2.2.4 Automatic temperature control system

The temperature of the susceptor is controlled with an automatic, closed-loop system, which is composed of an infrared heat-sensing element and a temperature controller. The sensor element, an electronic pyrometer, is centred directly above the bell jar, where it senses the temperature of the whole susceptor through a window in the bell jar. The controller can be set to control the generator power over an optical temperature range between 650 and 1200 °C. The susceptor temperature, which is maintained within ±2 °C of the set value, is displayed on the process control panel [5].

Note that the displayed temperature is the so-called optical temperature, which differs from the actual susceptor temperature. The true temperature of the susceptor was measured with an IR-camera Minolta Land Cyclops 52. The temperature measured by the reactor was corrected to the temperature measured with the IR-camera to ensure a constant temperature of the susceptor from run to run. This correction is important since reproducibility of the temperature is important in this fabrication process.
2.2.5 Process sequence and control

An Epitaxy EPITYME programmable unit controlled the process sequence. The settings of temperature and flows, etch time and deposition times were set manually with thumbwheels on the main control panel. Figure 2.5 presents the typical standard process sequence used for most of the depositions at 1100 °C.

![Diagram of process sequence](image)

**Figure 2.5:** Schematic overview of the standard process sequence at atmospheric pressure:
1. Prepurge with H₂
2. Ramp up to 700 °C (5 min.)
3. Ramp up to 1100 °C (10 min.)
4. Stabilisation of temperature and prepurge of gas system with reaction mixture
5. Deposition
6. Purge of reactor chamber
7. Cool down

The process sequence for deposition could be extended with extra steps e.g. an in-situ cleaning step with HCl or a prebake in H₂ just before the stabilisation step (4).

The reactor was loaded with wafers manually using vacuum tweezers and with samples using normal tweezers. During loading the chamber was continuously purged with N₂. The whole chamber was positioned in a down-flow cabinet.
2.3 Standard characterization methods

Besides several normal light microscopes, a scanning electron microscope (SEM, Philips PW 6705) was used for several purposes e.g. to check coverage, homogeneity and to measure the thickness of the deposited layers.

Several methods to measure the thickness of the deposited layer were used. For monocrystalline films on monocrystalline wafers an IR spectrophotometer BioRad Digilab QS-300 measurement system [6] was used. For films deposited on silicon oxides and ceramics a SEM equipped with a line-width measurement set-up was used. In some cases, conventional weighing using an accurate laboratory balance (Mettler) in combination with area measurements was used to determine the average thickness of the deposited layer.

Sheet resistances were measured with a Versa Probe VP10 resistivity tester from Prometix [7] in order to determine the active dopant concentration in the deposited films. This measurement is carried out on an n-type monitor wafer covered with the p-type epitaxial deposited layer using an automatic measurement sequence. This method can only be applied to films deposited on monocrystalline wafers; these wafers were used to monitor and tune the deposition processes. The incorporation of dopant atoms in polycrystalline silicon is significantly different, due to the presence of grain boundaries [8,9]. In general, all dopant concentrations reported in this thesis refer to the dopant concentration in the epitaxial film on the monocrystalline reference wafer, which has been grown simultaneously with the films on other substrates during the experiments.

2.4 References


Thermal chemical vapour deposition of film silicon
Chapter 3

Substrates for film-silicon thermal chemical vapour deposition

3.1 Substrates for film-silicon solar cells
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The choice of the substrate is one of the most important material issues in film-silicon solar cell research. In this section we will outline criteria for the selection of a substrate for the thermal CVD process. The initially selected substrates will be described in more detail. We tested whether they could serve as substrate for the CVD thermal processes. Finally, we describe the results of these tests and the refinement of the selection of substrates for film-silicon solar cells.
3.1 Substrates for film-silicon solar cells

In this section we outline some general criteria for the selection of a substrate for the thermal CVD process used in this film-silicon research. The most important criteria are listed in Table 3.1.

Table 3.1: General criteria for selection of a substrate:

1) Thermal expansion coefficient
2) Quality of the surface
   a) Porosity
   b) Surface roughness
3) Thermal stability
4) Process compatibility
5) Adhesion of silicon to substrate
6) Quality of the bulk
   a) Impurity concentration
   b) Phase composition
7) Costs per m²
8) Abundance of materials
9) Electrical properties
10) Optical properties

Since the aim of this research is to obtain a base structure consisting of a ceramic substrate covered with a compact and dense film of silicon, we only focussed on deposition of f-Si on substrates. Therefore, items 1 – 6 of the listed criteria in Table 3.1 are the most important and will be reviewed briefly in this section.

The thermal expansion coefficient of both the substrate material and the deposited silicon must match closely. If they differ, stress will be introduced in the silicon film after deposition, resulting in cracking of the silicon film or bending of the base structure. Bending will hinder the subsequent processes, in which the base structure will be changed into a working photovoltaic device. Porosity and surface roughness will influence the morphology of the deposited film directly. With a view on light trapping, some roughness can be desired. However, pores with a diameter larger than the thickness of the layer that has to be deposited, can result in films that do not cover the whole surface of the substrate.

With regard to the deposition conditions of the thermal CVD process, the substrate material must be stable at the high temperatures that are used. The material of substrate must be highly refractory
(capable of enduring high temperature). In addition, when recrystallisation processes like ZMR are used to enhance the electronic quality of the deposited material, the melting point of the ceramic material must be higher than the melting point of silicon, which is 1420 °C. The thermal shock resistance must also be high, since the temperature can be changed rapidly during the deposition and recrystallization processes. To speed up the process it is desired that the ramp-up times of temperatures are short.

The compatibility of the substrate material with the deposition environment in the reactor is also of major importance, because undesired reactions during the deposition are not allowed. In addition, good adhesion of the film to the substrate is required.

The composition of the bulk material must be considered too. Because a cheap substrate is desired, the base materials and production process must be cheap. This requirement results in the use of bulk materials, which in general contain impurities. Many of these impurities can diffuse into the film of silicon during the deposition process. These impurities may negatively affect the electronic properties of the silicon, which will result in reduction of the efficiency of the photovoltaic conversion process. A way to reduce contamination of the deposited silicon layer by impurities from the substrate is to introduce a barrier layer between the substrate and the deposited film. The criteria used for the selection of the substrate can also to choose a barrier layer material. An additional criterion for the selection of barrier layer material is its ability to minimize the diffusion of impurities from the substrate to the silicon during the deposition or during other high-temperature processes afterwards. The introduction of a barrier layer demands one or more extra steps (e.g. the deposition itself and pretreatments) in the production process of a film-silicon solar cell. Additional steps will increase the costs of the final solar cell. So it must be well considered whether the introduction of a barrier layer is necessary.

Several substrate materials have already been tested and evaluated in combination with a thermal CVD process. Some of them will be reviewed briefly in the next paragraphs.

Graphite has been studied extensively [1,2,3]. It is conductive and stable at high temperatures. However, severe problems with contamination from the substrate during the deposition have been
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reported [4]. Barrier layers appeared to be necessary. Efficiencies up to 11.0 % have been reported for a SiC coated graphite substrate [5].

Quartz is stable at high temperatures, but the thermal expansion coefficient differs too much. Films deposited on quartz crack [6] and even blister off. Therefore no notable efficiencies have been reported for film-silicon solar cells on quartz. Apart from the difference in thermal expansion coefficient, pure quartz is a very expensive material. However, glass or quartz is often used as substrate material for low-temperature deposition processes [7].

Problems with thermal expansion also occur when alumina (= Al₂O₃) is used as substrate material. The adhesion is very good, but the difference in the thermal expansion coefficient results in bending of the base structure. Efficiencies for small-area solar cells of 2.6 % have been reported in the past [8].

Metallurgical grade silicon substrates are still of interest [1,9]. The quality of the metallurgical grade silicon is lower than that of the solar grade silicon that is used for the active photovoltaic conversion layer. The metallurgical grade silicon is much cheaper since it is available in large quantities. For the production of these substrates processes like EFG, RGS and casting can be used. One example of a novel type of metallurgical grade silicon substrate is the Silicon Sheet from Powder (SSP) [10]. These substrates are made from metallurgical grade silicon powder, which is recrystallised using the ZMR method.

At present mullite [11] is gaining more and more interest. Mullite is an oxide-based ceramic made of alumina and silicon oxide. Besides these well-known materials, ceramic materials like SiSiC [12] and silicon nitride are being investigated.

For this research, alumina, mullite and metallurgical grade silicon substrates are used. In addition, two ceramic substrates based on commercially available SiAlON powder have been developed especially for this research.

3.2 Selection of substrates

In this paragraph we briefly review the composition, properties and preparation processes of the substrates used in this research. The substrates are based on metallurgical silicon and on ceramic materials. All substrates were developed and prepared at ECN in Petten (NL).
SEM micrographs of the surface of all substrates are presented in Appendix A.

### 3.2.1 Silicon with aluminium

Metallurgical grade silicon is used as base material for this substrate. The substrates were produced by a conventional tape casting technique using commercial silicon powder mixed with 4 wt% aluminium [13]. We will refer to these substrates as the Si/Al substrates. After tape casting the green tape, it was sintered at 1300 °C for 1 hour in argon. The aluminium increases the sinter ability of the silicon particles and enhances the conductivity of the final substrate. The substrates were about 50 % porous. The SEM micrographs in Appendix A show the surface of the substrate, in which large pores are visible.

### 3.2.2 Atmospheric plasma sprayed silicon

*Atmospheric plasma spraying (aps-Si)* is a fast deposition technique, which can be used for several materials. In this case commercial metallurgical grade silicon powder is sprayed using an Ar/H₂ plasma on a sodium chloride substrate [13]. After spraying, the sodium substrate is solved leaving a freestanding film of silicon. The preparation is simple, but the substrates have a very high porosity and very high surface roughness. Dependent on the feedstock material the substrates can be made conductive.

### 3.2.3 Mullite

Due to its outstanding properties, mullite is one of the most important materials in crystallography and ceramic science and technology today [14]. E.g. the material is highly refractory (melting point at 1828 °C), highly electrically insulating and its thermal expansion coefficient can be adjusted by changing the composition [14,15]. Therefore, mullite is gaining more interest as substrate material for film-silicon solar cells [11]. The mullite substrates for this research have been produced by a mixed oxide route using the tape casting technique starting with commercial Al₂O₃ and SiO₂ powders followed by a sinter process at 1600 °C for 1 hour in air [16]:

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\[ 3 \text{Al}_2\text{O}_3 + 2 \text{SiO}_2 \xrightarrow{1600^\circ\text{C}, 1 \text{h}, \text{aut}} \{3\text{Al}_2\text{O}_3 \cdot 2\text{SiO}_2\} \text{mullite} \]

Two types of mullite have been used. The first material was prepared using 28 wt% on silicon oxide in the mixed oxide route and the second using 30 wt% on silicon oxide. The substrates will be referred to as the 28% SiO\textsubscript{2} mullite and the 30% SiO\textsubscript{2} mullite respectively. The mullite substrates used in this research were not fully engineered to match the thermal expansion coefficient of silicon. The thermal expansion coefficient of the mullite with 30 wt% on silicon oxide matches the thermal coefficient of silicon most closely. All mullite substrates used show a smooth, yet porous surface.

3.2.4 SiaION

SiaION is one of the most inert ceramic materials available and has attracted interest for high-temperature engineering applications for decades [17]. This nitride-based ceramic material has a thermal expansion coefficient that closely matches the thermal expansion coefficient of silicon. SiaION substrates were made from commercial SiaION powder [16]. This powder is made from Si\textsubscript{3}N\textsubscript{4}, AlN and Al\textsubscript{2}O\textsubscript{3} powders as main reaction components and Y\textsubscript{2}O\textsubscript{3} powder for stabilisation reasons. The composition of SiaION can be described by a simplified formula: Si\textsubscript{x}Al\textsubscript{y}O\textsubscript{3}N\textsubscript{y}, in which x and y can vary.

Two substrates based on SiaION were developed. The first SiaION substrate, which is insulating, is produced from the SiaION powder by using tape casting and is sintered at 1550 °C for 1 hour in argon. This substrate will be referred to as the SiaION substrate. The second substrate, which is conductive, is also made of this material but 43 % silicon powder was added as an additional phase to the slurry. The samples have been sintered using the same conditions as used for the SiaION substrates. This modified substrate will be referred to as the Si/SiaION substrate.

The Si/SiaION substrates were still under development during the period of this research. The batch-to-batch homogeneity of the substrate preparation was not optimal. Therefore, emphasis was put on carrying out experiments with substrates, which were produced in one substrate production batch. Despite this selection, still inhomogeneities in color
of the surface of substrates from one batch could be observed, indicating inhomogeneities in substrate material at the surface. Even inhomogeneities in the colour of the surface of one substrate was observed.

3.2.5 Alumina

Alumina is widely used and known for its stability at high temperatures. In the field of microelectronics thermal CVD has been carried on sapphire, which is in fact monocristalline alumina. On the sapphire substrate epitaxial growth of silicon is possible with thermal CVD [18]. For this research polycristalline alumina substrates were produced from commercial Al₂O₃ powder by tape casting and sintering at 1600 °C for 1 hour in air. The thermal expansion coefficient of alumina and silicon differ significantly, therefore severe bending of the substrate can be expected. The substrates were mainly used for reference purposes. The substrate is referred to as Al₂O₃.

Table 3.2 gives an overview of the substrates used in this work, including their properties.

**Table 3.2: Properties of selected substrates used.**

<table>
<thead>
<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>Silicon²</td>
<td>2.33</td>
<td>-</td>
<td>-</td>
<td>grey</td>
<td>-</td>
<td>-</td>
<td>110</td>
<td>0.0001</td>
<td>4.5</td>
<td></td>
</tr>
<tr>
<td>Si/Al</td>
<td>1.2</td>
<td>49</td>
<td>450 – 470</td>
<td>grey</td>
<td>2</td>
<td>4.3</td>
<td>-</td>
<td>0.05</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Al₂O₃</td>
<td>3.7</td>
<td>5</td>
<td>320 – 350</td>
<td>white</td>
<td>1-6</td>
<td>0.5</td>
<td>350</td>
<td>1.0 × 10¹³</td>
<td>8</td>
<td>4-7</td>
</tr>
<tr>
<td>Mullite</td>
<td>3.17</td>
<td>22</td>
<td>200 – 220</td>
<td>white</td>
<td>1-6</td>
<td>1.0</td>
<td>140</td>
<td>1.0 × 10¹³</td>
<td>4-7</td>
<td></td>
</tr>
<tr>
<td>SiAlON</td>
<td>3.23</td>
<td>3</td>
<td>250 – 350</td>
<td>grey/white</td>
<td>1-3</td>
<td>3.0</td>
<td>290</td>
<td>1.0 × 10¹⁵</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>Si/SiAlON</td>
<td>-</td>
<td>3</td>
<td>320 – 360</td>
<td>grey/black</td>
<td>-</td>
<td>4.5</td>
<td>-</td>
<td>1-6</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>aps-Si</td>
<td>-</td>
<td>15</td>
<td>320 – 360</td>
<td>grey</td>
<td>25-75</td>
<td>5-6</td>
<td>&lt;110</td>
<td>1.5</td>
<td>5</td>
<td></td>
</tr>
</tbody>
</table>

¹) Average of the absolute values of the surface height variations measured from the mean surface level [19].
²) Data of monocristalline silicon for comparison.
3.3 Deposition of film-silicon layers

All substrates described above were tested on their suitability in a thermal CVD process by carrying out several depositions directly on these substrates. The main requirements are a compact and dense film covering the whole surface of the substrate. The substrates were tested in a standard deposition process, of which the parameters were:

- Substrate temperature of 1100 °C,
- DCS concentration of 1.2 % in H₂,
- B₃H₆ concentration on 13 ppm in H₂,
- Atmospheric pressure.

This standard process is an optimised process for deposition of monocrystalline silicon with DCS as precursor gas. The thickness of the deposited films was always in the range of 5 – 20 µm. Pretreatment procedures were adapted for each substrate. The effect of changing the deposition temperature was investigated. Series of samples per substrate material have been made at several deposition temperatures.

To gain some information about the nucleation of the film-silicon on these substrates, short depositions of 1 minute were carried out. Within this short time, no homogeneous reaction mixture can be obtained in the reactor. The volume of the bell jar is approximately 100 litres and the flows used are in the range of 70 to 100 slm. To purge the bell jar one time takes at least one minute. The rotation of the susceptor partly averages this mixture inhomogeneity. All samples were used in one run with a short deposition period to ensure equal exposure times of the samples to the reaction environment.

In the next paragraphs the results of the deposition of a film-silicon on the selected substrates are described. All deposited layers were checked whether they were compact and covered the whole area of the surface. Typical sizes of the samples were in the range of 20×25 to 60×60 mm².

3.3.1 Si/Al substrates

Figure 3.1 shows two SEM micrographs of f-Si that is deposited on the Si/Al substrates.
Figure 3.1: SEM micrographs of f-Si deposited on the Si/Al substrates.

A film consisting of large (up to 40 \( \mu \text{m} \)) irregular shaped grains was deposited. The coverage of the film was very poor, as can be observed from the SEM picture. Silicon films deposited on a Si/Al substrate that was covered with a LPCVD silicon carbide (SiC) showed a slightly more compact structure compared to layers deposited directly on the Si/Al substrate. SiC was used because of its potential to serve as barrier layer material. The porosity and roughness of the substrate had hardly changed since the thickness of the deposited SiC layer was 5 – 6 \( \mu \text{m} \).

Since the substrates are too porous to deposit a compact and dense film, no short depositions were carried out.

3.3.2 \textit{aps-Si substrates}

Figure 3.2 shows two SEM micrographs of f-Si that is deposited on the \textit{aps-Si} substrates.

Figure 3.2: SEM micrographs of f-Si deposited on the \textit{aps-Si} substrates.

On the \textit{aps-Si} substrate also large irregular grains (40 - 50 \( \mu \text{m} \)) were deposited, which could be compared to the deposits on the Si/Al substrate. Because the APS-Si substrate has a lower porosity compared to the Si/Al substrate, a closed film could be deposited, dependent on
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the deposition time and the size of the pores. The morphology of the deposited film was strongly determined by the surface structure of the substrate, which showed the highest roughness factor of all substrates.

Since the substrates are too porous and too rough for deposition of a compact and dense film, no short depositions were performed.

3.3.3 Alumina substrates

Figure 3.3 shows two SEM micrographs of f-Si that is deposited on the Al$_2$O$_3$ substrates.

![Surface view](image1)

![Cross section](image2)

**Figure 3.3:** SEM micrographs of f-Si deposited on the Al$_2$O$_3$ substrates.

On this substrate, a compact and dense film that covered the whole substrate area was deposited. The Al$_2$O$_3$ substrate shows a smooth surface and the lowest porosity. After deposition, the samples suffered from severe compressive stress, due to differences in the thermal expansion coefficients of the deposited f-Si and the substrate material.

Figure 3.4 shows two SEM micrographs of samples after a short deposition time of 1 minute on the Al$_2$O$_3$ substrate.

![10 μm](image3)

![10 μm](image4)

**Figure 3.4:** SEM micrographs of short depositions on the Al$_2$O$_3$ substrate.
These micrographs reveal that nucleation usually occurs at the grain boundaries at the surface of the substrates. This phenomenon has also been reported by [20].

### 3.3.4 Mullite substrates

Figure 3.5 shows two SEM micrographs of f-Si that is deposited on the mullite substrates.

![SEM micrographs of f-Si deposited on the mullite substrate.](image)

Figure 3.5: SEM micrographs of f-Si deposited on the mullite substrate.

On this substrate a compact layer of f-Si is formed. However, large pores in this substrate resulted in channel-like pinholes perpendicular to the surface and throughout the whole thickness of the film. Despite of the high porosity of the substrate, it appears that most of the pores in the substrate can be covered. Except for the pinholes, the morphology of the remainder of the deposited film of silicon can be compared with the layers deposited on the Al$_2$O$_3$ substrate: compact and dense. Compressive stress in the samples was observed visually since the samples were bent after the deposition. The 30% SiO$_2$ mullite substrates were less bent after deposition than the 28% SiO$_2$ mullite substrates. At lower deposition temperatures (850 °C), some spots with whiskers were observed on the samples.

Figure 3.6 shows two SEM micrographs of samples after a short deposition time of 1 minute on the Al$_2$O$_3$ substrate.
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Figure 3.6: SEM micrographs of short depositions on the mullite substrate.

The substrate has a fine polycrystalline structure compared to the polycrystalline Al₂O₃ substrates. It is not clear whether nucleation occurs at grain boundaries at the surface since the grain boundaries are not visible using SEM.

3.3.5 SiAlON based substrates

As mentioned in section 3.2.4 two types of SiAlON substrates have been used. The results of the depositions on these substrates will be presented in the next two paragraphs.

A) f-Si on Si/SiAlON substrates

The Si/SiAlON substrates exhibit large lumps of silicon on the surface, which results in a value of the surface roughness that is similar to the desired thickness of the film. These lumps of silicon are formed during the sintering process. During the sintering process, the silicon particles within the substrate melt. When the substrates are cooled down at the end of the sinter process, the molten particles in the bulk and at the surface of the substrate coalesce and recrystallize. As a result large spherical lumps of silicon are formed on the surface of the substrate. The diameter of these lumps can exceed 100 μm. Figure 3.7 and Appendix A show SEM micrographs of the surface of the as-sintered substrates, with the spherical silicon particles.
Figure 3.7: SEM micrograph of the surface of as-sintered Si/SiAlON substrate.

For our CVD process, this roughness is too large as it prevents compact f-Si, which can be used for solar cells. In order to reduce the roughness, the substrates were smoothened at ECN using a simple polishing procedure. The average roughness (Ra) could be reduced to \( \sim 2 \, \mu m \).

In the initial experiments, depositions on both rough and polished Si/SiAlON substrates resulted in whisker formation. Whiskers are needle-like, highly anisotropic crystals that are not desired. Figure 3.8 shows a SEM-micrograph of a deposition on polished Si/SiAlON substrate, which resulted in the typical whisker growth.

Figure 3.8: SEM micrograph of typical whisker growth on the Si/SiAlON substrate.

We have developed several methods to reduce the whisker formation. The developed methods were based on cleaning the
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substrates and can be divided into ex-situ and in-situ processes. Two ex-situ cleaning methods were found to reduce the whisker formation. The most effective method was immersing the substrates in boiling HNO₃ 65 % for a period of 10 minutes followed by rinsing with demiwater. Cleaning in boiling HNO₃ 65 % is a well-established cleaning method in IC technology, in which metallic particles and impurities are removed. Another ex-situ cleaning of the substrates is based on standard RCA cleaning agents as used in IC processing. RCA cleaning agents have derived their name from their institute of development: RCA laboratories [21]. Deposition on the substrates after RCA cleaning resulted in f-Si layers that are similar to the layers deposited on substrates that are cleaned in boiling HNO₃ 65 %. The exact composition and procedures of RCA cleaning are listed in Table 3.3.

Table 3.3: Description of the RCA cleaning agents used.

<table>
<thead>
<tr>
<th>Use</th>
<th>RCA 1</th>
<th>RCA 2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Removal of organic impurities</td>
<td>Removal of metallic impurities</td>
</tr>
<tr>
<td>Composition (parts)</td>
<td>H₂O</td>
<td>H₂O</td>
</tr>
<tr>
<td></td>
<td>H₂O₂ (30%)</td>
<td>H₂O₂ (30%)</td>
</tr>
<tr>
<td></td>
<td>NH₄OH (25%)</td>
<td>HCl (27%)</td>
</tr>
<tr>
<td>Procedure of cleaning</td>
<td>10 min. at 80 °C</td>
<td>10 min. at 80 °C</td>
</tr>
</tbody>
</table>

The RCA agent that is used for the removal of metallic impurities (RCA 2) appeared to reduce the whisker formation more effectively than the RCA agent that is used to remove organic contaminations (RCA 1).

Figure 3.9 shows a SEM micrograph of a cross section of a Si/SiAlON substrate covered with a f-Si layer. The substrate was cleaned with boiling HNO₃ 65 % for 10 minutes and thoroughly rinsed with demiwater. The size of the crystal grains at the top surface is typically in the range of 1 – 10 µm, dependent on the thickness of the film, since the grains are slightly V-shaped.
Figure 3.9: SEM micrograph of a f-Si layer deposited on a Si/SiAlON substrate, that was polished and cleaned ex-situ with boiling HNO$_3$ 65 %.

Besides the ex-situ cleaning procedures of substrates also in-situ cleaning procedures were developed. For this purpose, HCl was used at substrate temperature equal to the deposition temperature. The HCl in-situ cleaning procedure is commonly used for periodic etching of the susceptor in the reactor. During this process, silicon is etched at a rate of $\sim 6 \, \mu$m/min. For cleaning the Si/SiAlON substrates, the flows and etching periods have been adapted to more gentle conditions. The HCl concentration was 2.7% in H$_2$ and the etching period was 2 min. The in-situ cleaning procedure reduces the whisker formation, but is not so effective as the ex-situ cleaning procedures we mentioned. The in-situ cleaning procedure can result in large holes at the surface, since the infiltrated silicon particles are etched away.

The most effective method to reduce whisker formation is the ex-situ procedure with boiling HNO$_3$ 65 %. In some cases, however, e.g. when large-area samples (60 $\times$ 60 mm$^2$) are used, whisker formation was still noticed. A combination of the ex-situ cleaning procedure followed by the in-situ cleaning reduces the remaining whisker formation. The depositions on these large area samples resulted in smooth and compact layers of f-Si. SEM analysis showed that the size of the crystal grains in these films were slightly smaller compared to those in films deposited on substrates that were only treated with boiling HNO$_3$ 65 %.

Appendix B shows SEM micrographs of series of samples at different deposition temperatures. The size of the samples was 20 $\times$ 20 mm$^2$. It appeared that when boiling HNO$_3$ 65 % was used, the whisker formation could be reduced. For example, when no cleaning with HNO$_3$ was performed, whisker formation occurred during deposition at 1100
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°C. When the substrates were cleaned with boiling HNO₃, no whiskers were observed after a deposition at 1100 °C. However, when the deposition temperature was reduced and cleaned substrates were used, some whiskers were observed after a deposition at 1050 °C. When the temperature was reduced further, the whisker formation increased.

Despite the fact that silicon and SiAlON have almost similar thermal expansion coefficients, experiments in which depositions are carried out on Si/SiAlON substrates resulted in samples that could not be used for further processing, because the samples were bent too severely. The area of these samples was 30 × 30 mm², and the curvature was more than 1 mm. Also a heat treatment in the reactor (one cycle without deposition) resulted in bent substrates after these had cooled down to room temperature. Apparently, the Si/SiAlON samples do not relax to their original shape.

Figure 3.10 presents two SEM micrographs of the Si/SiAlON samples after a short deposition period of 1 minute.

![SEM micrographs](image)

**Figure 3.10:** SEM micrographs of short depositions on the Si/SiAlON substrate.

Nucleation on Si/SiAlON substrates results in irregular deposits. The SEM micrographs show small whiskers. Our results did not show whether a relation exists between the position of the observed clusters of whiskers and the infiltrated silicon in the substrate.

**B) f-Si on SiAlON substrates**

Depositions on SiAlON-based substrates mostly resulted in compact and dense layers of f-Si covering the whole substrate area. Simple cleaning methods are sufficient, e.g. rinsing with demiwater is enough when samples of 20 × 20 mm² are used. However, when the substrate area is increased to e.g. 60 × 60 mm², some whiskers were formed. The
in-situ cleaning procedure mentioned previously effectively reduces this whisker formation. Figure 3.11 shows a SEM micrograph of a cross section of a f-Si layer on a SiAlON substrate.

![SEM micrograph of cross section of a layer of f-Si deposited on a SiAlON substrate.](image)

Figure 3.11: SEM micrograph of cross section of a layer of f-Si deposited on a SiAlON substrate.

In Table 3.2, it was reported that the thermal expansion coefficients of silicon and SiAlON are almost similar. Deposition of silicon on the SiAlON substrate resulted in samples that were slightly bent. The curvature of samples with an area of $60 \times 60 \text{ mm}^2$ was less than 1 mm. At low deposition temperatures ($< 850 \, ^\circ\text{C}$), some spots with whiskers were noticed. Figure 3.12 presents two SEM micrographs of the SiAlON samples after a short deposition period of 1 minute.

![SEM micrographs of short depositions on the SiAlON substrate.](image)

Figure 3.12: SEM micrographs of short depositions on the SiAlON substrate.

Also this substrate reveals a fine polycrystalline structure. The nuclei density on the SiAlON substrate is higher compared to that on the mullite substrate.
3.4 Whisker formation

Whisker formation has been observed most distinctively on the Si/SiAlON substrates. Methods to reduce this whisker formation have been developed. In order to gain a better understanding of how to avoid whisker formation, more detailed information about the growth mechanism of these whiskers is necessary. The growth mechanism of whiskers in general has been a topic of intensive research for many years [22]. Silicon whisker growth is commonly described by the vapour-liquid-solid (VLS) mechanism. A general schematic presentation of a VLS mechanism is given in Figure 3.13.

![Figure 3.13: Schematic presentation of the VLS mechanism.](image)

In most reported cases a film of metal (Au, Ag, Pd, Ni) is deposited which will form the liquid phase during deposition, when relatively high temperatures are used. In the ideal case, the molten film coalesces to droplets and forms preferred sites for nucleation (I). The formed nucleus starts to grow until a whisker is formed with a droplet of liquid metal on top. (II). The formed whisker starts to grow preferentially in one direction. At the sides of the whisker epitaxial deposition occurs directly from the gas phase (III). The deposition rate of the epitaxial process is in general much lower than the deposition rate at the liquid-solid interface (IV). Four principal steps can be distinguished: ① mass transport in the gas phase, ② chemical reactions on the vapour-liquid interface, ③ diffusion in the liquid phase and ④ incorporation of the material in a crystal lattice. According to Givargizov et al. [22] step ④
is the rate-determining step. The deposition rate of silicon at the liquid-solid interface in the VLS system is higher than the deposition rate of the epitaxial process \( \odot \), which results in the elongated structure of the whisker.

From our experiments we can confirm that the VLS mechanism for the whisker formation occurs during the CVD process with Si/SiAlON substrates. Figure 3.14 shows a SEM micrograph of a whisker grown at 950 °C and on 900 °C on a polished Si/SiAlON substrate. The deposition time was 10 minutes. The substrates were cleaned with boiling HNO\(_3\) 65 % for 10 minutes and rinsed with demineralised water.

\[ \text{Figure 3.14: SEM micrographs of a whisker on a Si/SiAlON substrate grown at (a) 950 °C and (b) 900 °C.} \]

At higher temperatures the whisker growth disappears and at lower temperatures the whisker growth is very strong. Appendix B gives an overview with SEM micrographs of depositions on the Si/SiAlON substrates at several temperatures. On the top of the whisker a rough globule of unknown material is present. This globule is often not present during analysis, due to evaporation or due to loss during the cooling down process. The whisker is crystalline, since a faceted shape is often observed. A hexagonal structure is often observed, which implies that the main growth direction of the whisker is [111], which is known to be the direction of slow growth. Since the base of the whisker is thicker than the top region of the whisker, the longitudinal whisker growth is expected at top of the whisker and not at the base. Evaluating the structure of whiskers with globule, a VLS growth mechanism according to the VLS theory can be expected.
Substrates for film-silicon thermal chemical vapour deposition

Additional evidence for VLS growth mechanism is the observed periodic instability [22]. Figure 3.15 shows a SEM micrograph of a whisker with a periodic instability.

![SEM micrograph of whiskers with periodic instability deposited on a Si/SiAlON substrate.](image)

**Figure 3.15:** SEM micrograph of whiskers with periodic instability deposited on a Si/SiAlON substrate.

This characteristic periodic instability is most distinctly observed in silicon whiskers grown with gold or gold-based alloys as liquid-forming impurities [22]. The whisker consists of a row of knots and necks with approximately equal distances between them. This periodic instability is of a self-oscillatory nature, driven by vapour supersaturation and surface forces.

From the observation of globules and the periodic instabilities, it can be assumed that the whisker growth on the Si/SiAlON substrate during the CVD process follows the VLS mechanism. However, this theory implies the presence of a liquid phase. Often metals are used in processes in which silicon whiskers are grown. In our system, no liquid-forming phases are added. Therefore, it must be assumed that the substrate supplies this ‘liquid phase’ with or without aid from reactive species from the vapour phase e.g. Si or Cl.

Two chemical analysis methods, energy-dispersive X-ray spectroscopy (EDX) and Auger electron spectroscopy (AES) used on the globule and whisker revealed that both parts consist of pure silicon. The detection limit of both analysis methods is in the range of 0.1 – 1 at%.
3.5 Deposition rates

The deposition rates of f-Si at several deposition temperatures were compared with each other. Figure 3.16 shows deposition rates of film-silicon for different substrates as a function of the deposition temperature.

![Deposition rates graph](image)

**Figure 3.16:** Deposition rates of f-Si at several temperatures.

Thermally oxidized wafers (SiO$_2$) and monocristalline wafers (sc-Si) were included as a reference system. Since ten samples could be placed in the reactor, the whole range of substrates could be used in one run at a certain deposition temperature. This ensures the same deposition conditions for all samples at one deposition temperature. The two regimes as described in Chapter 2 can be recognized. The deposition rate of f-Si on the SiO$_2$ and ceramic substrates in the diffusion-controlled regime shows similar values when compared with the deposition of f-Si on monocristalline wafers. The deposition rates in the temperature-controlled regime are lower compared to the deposition rates of f-Si on monocristalline wafers. Diffusion of reactive species on the substrate surface plays a role in the kinetics of the deposition process in this temperature regime. Since the surface of the samples is different in every case, the difference in deposition rate can be
attributed to the surface properties of the substrates, e.g. material, porosity and to the crystal orientation of the deposited silicon.

3.6 Conclusions

All selected substrates have been tested on their suitability to serve as substrate in the f-Si thermal CVD process. The main requirement that compact dense films covering the whole surface of the substrate should be deposited. The Si/Al and aPS-Si substrates have a porosity and surface roughness that is too high to get a compact film on the substrate. On the Al₂O₃, mullite, SiAlON and Si/SiAlON substrates, compact and dense films could be deposited. Table 3.4 presents the overview of f-Si deposition on the different substrates in terms of the porosity, surface roughness and the structure of the deposited film.

Table 3.4: Comparison of f-Si deposition results on substrates with different porosities and average surface roughness. The thickness of the deposited film was 10 μm.

<table>
<thead>
<tr>
<th>Substrate</th>
<th>Porosity [%]</th>
<th>Roughness [Ra]</th>
<th>Compact layer</th>
</tr>
</thead>
<tbody>
<tr>
<td>aPS-Si</td>
<td>15</td>
<td>5.6</td>
<td>-</td>
</tr>
<tr>
<td>Si/Al</td>
<td>49</td>
<td>4.3</td>
<td>-</td>
</tr>
<tr>
<td>SiAlON</td>
<td>3</td>
<td>3.0</td>
<td>+</td>
</tr>
<tr>
<td>Si/SiAlON</td>
<td>3</td>
<td>4.5</td>
<td>+</td>
</tr>
<tr>
<td>Al₂O₃</td>
<td>5</td>
<td>0.5</td>
<td>+</td>
</tr>
<tr>
<td>Mullite</td>
<td>22</td>
<td>1.0</td>
<td>+</td>
</tr>
</tbody>
</table>

Porosity does not include the size of the pores, but presents a ratio of the empty volume in the defined substrate volume. The size of the pores at the surface influences the surface roughness directly. Therefore conclusions about a direct relation between porosity and surface roughness must be drawn carefully. A high porosity does not mean that the pores are large.

In Table 3.4 some trends can be observed. At low roughness values some porosity of the substrates can be accepted. This is limited by the size of the pores at the substrate surface, as is observed with the mullite samples. When the pores' size is too large, no complete coverage of the
pores can be achieved. Complete coverage of pores also depends on the thickness of the deposited layer.

Large pores will also increase the surface roughness. At higher roughness values, low porosity of the substrates is necessary. The maximum roughness value is dependent on the step coverage of the f-Si layer and on the thickness of the deposited layer.

Several samples were bent after the deposition process, which means that stress is present in the base structure, which consists of the substrate with the deposited film-silicon. For samples that were bent enormously, e.g. Al₂O₃ and mullite, the difference in the thermal expansion coefficients of substrate and film is one of the major causes of the stress. An increase of the silicon oxide concentration in the mullite substrate to 30 % resulted in less bent samples. Despite the improvement, the difference in thermal expansion coefficient is still too large. In the next chapter, more detailed information on stress caused by the difference in thermal expansion coefficient is presented.

Most substrates are thermally sufficiently stable, except for the Si/SiAlON. Due to the composition of the substrate, there was weak thermal relaxation. During the process a substrate will bend slightly due to the systematic difference in temperature across the sample, as indicated in Figure 3.17:

![Figure 3.17: Schematic presentation of the typical systematic difference in temperature across the substrate at deposition temperature.](image)

In an ideal case, the sample will relax to its original shape when cooling down to room temperature during a heat-up and cool down process. The Si/SiAlON substrates do not relax completely to their original shape. This substrate material is a SiAlON matrix in which silicon particles are incorporated. Silicon and SiAlON show slightly different thermal expansion coefficients, which causes different internal strains resulting in some changes of the material properties when exposed to high temperatures. This problem with thermal relaxation was not observed with the rest of the substrate materials.
The process compatibility can be evaluated by the occurrence of whisker formation during growth. Most of the substrates show a good compatibility with the deposition process used at the standard deposition temperature of 1100 °C. Mullite and SiAlON show some whisker formation at a deposition temperatures of 850 °C and lower. Increasing the SiAlON substrate area also resulted in whisker formation, which could easily be eliminated using cleaning processes. Apparently the size of the substrate area influences the process compatibility. The Si/SiAlON substrate shows very bad process compatibility. Severe whisker formation is observed; the whiskers can only be reduced using the cleaning procedures as described in Section 3.3.5. It is possible to grow compact f-Si layers on the Si/SiAlON substrates at temperatures above 1000 °C after the application of a proper pre-treatment procedure. Despite the cleaning procedures, severe whisker formation is still observed at lower deposition temperatures.

No impurities in the globule and whisker could be detected using the elemental analysis methods EDS and AES. The detection limit of both techniques is ~ 0.1 at%. However, an evaluation of cleaning methods shows that the most effective ones are those that remove metallic impurities. Apparently metallic impurities play a role in the observed whisker growth.

Concerning the deposition rates at the different temperatures, we recommend to use deposition temperatures within the diffusion-limited deposition regime for all substrates. In this regime the highest deposition rates are achieved and the process compatibility is best. On the other hand, the influence of differences in thermal expansion coefficient is larger at higher temperatures. Therefore it is necessary to use substrate material with a thermal expansion coefficient similar to silicon. At lower temperatures the deposition rates are influenced by the surface, since lower deposition rates are observed compared to those in the ideal case of the monocristalline substrate. Additional, more whisker formation occurred at lower deposition temperatures.

In the rest of this research some of the substrates will not be used. Only the substrates on which a compact and dense layer could be deposited were selected for further research. A brief overview of the deposition results is presented in Table 3.5, which takes into account the properties of the substrates.
Table 3.5: Brief overview of the results of the depositions on the initially selected substrates. The last column presents the substrates selected for further research.

<table>
<thead>
<tr>
<th>Substrate</th>
<th>Deflection after deposition</th>
<th>Influence of initial surface roughness on deposition</th>
<th>Process compatibility</th>
<th>Thermal relaxation</th>
<th>Resistivity [Ω·cm]</th>
<th>Compact layer of f-Si</th>
<th>Selected for further research</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si/Al</td>
<td>-</td>
<td>+</td>
<td>+</td>
<td>+</td>
<td>0.05</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>aps-Si</td>
<td>-</td>
<td>+</td>
<td>+</td>
<td>+</td>
<td>1.5</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Mullite</td>
<td>++ (c)</td>
<td>-</td>
<td>+</td>
<td>+</td>
<td>10^{13}</td>
<td>+</td>
<td>+</td>
</tr>
<tr>
<td>Al_{2}O_{3}</td>
<td>+++ (c)</td>
<td>-</td>
<td>++</td>
<td>+</td>
<td>10^{13}</td>
<td>+</td>
<td>+</td>
</tr>
<tr>
<td>SIAION</td>
<td>-</td>
<td>-</td>
<td>+/-^{3}</td>
<td>+</td>
<td>10^{5}</td>
<td>+</td>
<td>+</td>
</tr>
<tr>
<td>Si/SIAION</td>
<td>+ (t)</td>
<td>+^{2}</td>
<td>+/-^{3}</td>
<td>-</td>
<td>1-6</td>
<td>+</td>
<td>+</td>
</tr>
</tbody>
</table>

1) c = compressive, t = tensile
2) Can be improved by polishing procedures
3) Can be improved by suitable cleaning procedures
4) Pre-treatments included in process

3.7 References


Chapter 4

Stress and structure of thin polycrystalline silicon films

4.1 Introduction
4.2 Stress in film-silicon on ceramic substrates
4.3 X-ray diffraction on film-silicon on ceramic substrates
4.4 Crystal morphology of film-silicon: TEM analysis
4.5 Discussion
4.6 Conclusions
4.7 References

This chapter discusses the crystallographic structure and stress in the film-silicon layers deposited on several ceramic substrates. Both substrate material and deposition temperature appeared to influence the stress and the crystallographic structure.
4.1 Introduction

In the previous chapter, ceramic substrates were selected for further research. The criteria for this selection were mainly the capacity to obtain a compact and dense f-Si layer using thermal CVD. In this chapter a more detailed study on stress and crystallographic structure of the deposited f-Si layer is presented. The influence of the deposition temperature and substrate material on the stress and crystallographic structure was analysed and evaluated with X-ray diffraction and transmission electron microscopy.

To study the influence of the substrate, f-Si was deposited on Al₂O₃, mullite and SiAlON substrates. To investigate the influence of the deposition temperature on stress and crystallographic structure, series of f-Si samples were prepared at deposition temperatures 900 °C, 1000 °C and 1100 °C on SiAlON substrates. The deposition time was adjusted in order to obtain layers with a similar thickness, which was ~ 10 μm.

4.2 Stress in film-silicon on ceramic substrates

The results described in Chapter 3 demonstrate that in every case stress was observed in the sample after deposition. This stress could be observed visually, since the samples were bent after the deposition process at room temperature. This bending is undesired since it can hinder the subsequent process steps, in which the base structure will be processed into a working photovoltaic device.

The stress that is present in the film-silicon base structures after deposition at room temperature is called residual stress. This residual stress is often described as the elastic biaxial stress parallel to the specimen surface, which is equal to the sum of thermal stress, \( \sigma_{th} \), and growth stress, \( \sigma_{gr} \) [1,2]. A difference in thermal expansion coefficient of the substrate material and deposited silicon leads to thermal stress when both layers cool down from deposition temperature \( (T_{\text{deposition}}) \) to room temperature \( (T_{\text{room}}) \). In case the thin layer, which is assumed to be isotropic, elastically absorbs all misfits, thermal stress is given by [1,2]:
\[ \sigma_{th} = \frac{E}{1 - \nu} (\alpha_s - \alpha_f) (T_{room} - T_{deposition}) \]  

(4.1)

where \( \alpha_s \) and \( \alpha_f \) are the linear thermal expansion coefficients of the substrate and the deposited film respectively, \( E \) is Young’s modulus and \( \nu \) is Poisson’s ratio of the deposited film. A difference in thermal expansion or shrinkage caused by differing thermal expansion coefficients can result in two different states of stress: tensile or compressive stress. Figure 4.1 shows a schematic representation of the development of these two states of stress when a f-Si layer is deposited on a substrate.

<table>
<thead>
<tr>
<th>At deposition temperature</th>
<th>f-Si layer</th>
<th>No stress</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>At room temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \alpha_{\text{silicon}} &gt; \alpha_{\text{ceramic}} )</td>
</tr>
<tr>
<td>Tensile stress</td>
</tr>
</tbody>
</table>

| \( \alpha_{\text{silicon}} < \alpha_{\text{ceramic}} \) |
| Compressive stress |

**Figure 4.1:** Thermal stress in a f-Si layer on a substrate structure after cooling from deposition temperature. At the deposition temperature the f-Si layer and substrate are assumed to be stress free. The difference in thermal expansion coefficients leads to stress.

The exact cause of growth stress is often not exactly known. In the overview of Hoffman et al. [2] several elementary causes that may produce growth stress are proposed:

1. Incorporation of atoms, e.g. residual gases or chemical reactions,
2. Differences of the lattice spacing of the substrate material and the film material in the case of epitaxial growth,
3. Variation of the interatomic spacing within the crystal,
4. Recrystallization processes,
5. Microscopic voids and special dislocation arrangements,
6. Phase transformation.
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The contribution from either thermal stress or growth stress is tension or compression [2]. Compressive growth stress occurs in dense layers, while tensile growth stresses are found in porous layers. The total residual stress is temperature dependent, since both contributions are also temperature dependent. In Figure 4.2 we consider an ideal case of a film that is deposited on a substrate and finally cooled down to room temperature.

![Stress vs Deposition Temperature Graph]

**Figure 4.2:** Schematic representation of the residual stress as a sum of the contributions from thermal and growth stress according to [2].

The contribution of thermal stress is dependent on the materials used, as described with Equation 4.1. In general, thermal expansion coefficients are temperature dependent. Enough data about the thermal expansion coefficient of crystalline silicon is available [3]. The thermal expansion coefficients of the ceramic materials used for this research are kept constant. The growth stress is often a decreasing function of the temperature, so that the resulting residual stress in the film may have a minimum at some intermediate temperature.

A common method to analyse stress is the X-ray diffraction (XRD) method. With this method, two types of stress fields in materials can be analysed defined as *macro stress* and *micro stress*. Macro stresses change slowly over macroscopic lengths along at least one dimension. In an X-ray analysis, the macro stress is measured by investigating lattice spacing changes, which are observed by a shift of position of the diffraction line. Therefore, the measured stress is often referred to as *lattice stress* instead of macro stress. In this thesis we will refer to macro stress instead of lattice stress. Macro stresses can relax, when for example the sample is cut into smaller pieces. Micro stress, and the related micro deformation, vary widely from point to point in a
microscopic domain of the samples and are inhomogeneously distributed. Micro stresses can relax only after sample annealing at higher temperatures. In an X-ray analysis, micro stresses can be derived from the broadening of the diffraction line. The previously described residual stress is the sum of the macro and micro stress measured with XRD [4].

4.3 X-ray diffraction on film-silicon on ceramic substrates

The X-ray diffraction analysis was carried out on an automatic powder diffractometer URD-6 with a Bragg-Brentano goniometer using CuKα radiation (\(\lambda = 0.154178 \text{ nm}\)). In the Bragg-Brentano configuration, the diffracting set of lattice planes is parallel to the surface. Ceramic Al₂O₃ from National Institute for Standards and Testing, USA, was used as an instrumental standard. Because no monochromator was used, the Kα₂ radiation had to be removed by means of approximation of experimental profiles using a Pearson VII profile.

Using the normal Bragg-Brentano geometry the lattice spacing was measured from the peak intensity versus scattering angle \(2\theta\) according to Bragg's law,

\[ 2d \sin \theta = \lambda \]  \hspace{1cm} (4.2)

where \(\lambda\) is the wavelength of the X-ray radiation, \(\theta\) is the angle between the sample and the incident beam, \(d\) is the measured lattice spacing of the sample material. Figure 4.3 presents a schematic drawing of the Bragg-Brentano geometry.

![Diagram](image)

**Figure 4.3:** Schematic presentation of the Bragg-Brentano geometry.
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The X-ray diffraction patterns were collected by varying 2θ with a constant step of 0.02 degrees and with a constant counting time of 20 seconds at each step. For theoretical calculations of the reference positions of the individual diffraction lines for polycrystalline Si, \( d_0 \), we used the standard lattice parameter \( a = 0.54309 \) nm (ICDD Standard Reference Material - SRM 640 b). The computer programme APX 63 STRUC was used to carry out these calculations. Appendix C presents the results of these calculations. Besides the position of the diffraction lines also relative intensities and interplanar spacing of polycrystalline silicon with randomly oriented crystallites were calculated.

The state of stress can be analysed by measuring of the lattice spacing according to Bragg’s law (Equation 4.2). In the stressed state of the specimen, its measured lattice spacing \( d \) will deviate from the value in the unstressed state \( (d_0) \). To analyse the macro stress in the polycrystalline films, the \( \sin^2 \psi \) method is commonly used [4,8]. For this method, the lattice spacing is measured according to Bragg’s law at varied angles \( \psi \) of the sample. The angle \( \psi \) is the angle between the surface of the sample and the plane of diffraction. However, the \( \sin^2 \psi \) method could hardly be applied, due to the very strong preferred orientation and due to the relatively thin films, the intensity is too low for correct determination of the line position at diffracting angles in sample positions with \( \psi \neq 0 \) degrees. Therefore the determination of the macro stress was carried out using a procedure proposed by Šutta [5] using the Bragg-Brentano configuration (\( \psi = 0 \)). This method is adapted from the \( \sin^2 \psi \) method. If the stress is homogeneous and isotropic (in thin films of material characterized by a cubic unit cell it is mostly satisfied) the macro stress can be determined from the shift of a diffraction line according to [5]:

\[
\sigma_{11} + \sigma_{22} = \frac{E}{\nu} \frac{d_{\text{exp}} - d_0}{d_0} \quad (4.3)
\]

where \( E \) is Young’s modulus, \( \nu \) is Poisson’s ratio, \( d_{\text{exp}} \) is the lattice spacing obtained from the experimental data, and \( d_0 \) is the unstressed lattice spacing, which is calculated from the structure model for the strain-free reference state. We determined the sum of the main stresses \( (\sigma_{11} + \sigma_{22}) \) in the plane of the layer according to Equation 4.1, using a
value of $165.9 \times 10^9$ Pa for Young’s modulus and 0.217 for Poisson’s ratio [6].

In the deposited thin polycrystalline silicon layers the preferential orientation (texture) is observed in the directions [111] and [110]. Therefore, it is sufficient in the first approximation to determine the ratio of intensities of (220) and (111) diffraction lines. For a completely random orientation of the grains, this ration is about 0.68. The comparison of the intensities of two most intense lines is only a very rough texture evaluation. For a complete texture analysis, it is necessary to record pole figures, but the goniometer we used was not suitable for this purpose.

The results of XRD measurement for all layers are summarized Table 4.1.

**Table 4.1:** The preferential orientation ($I_{220}/I_{111}$), the lattice parameter and the macro stress of the f-Si layers deposited on various substrates and at different deposition temperatures.

<table>
<thead>
<tr>
<th>Substrate</th>
<th>Deposition temperature [°C]</th>
<th>$I_{220}/I_{111}$</th>
<th>Macro stress ($\sigma_{11} + \sigma_{22}$) [Mpa]</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiAlON</td>
<td>900</td>
<td>13.1</td>
<td>553</td>
</tr>
<tr>
<td>SiAlON</td>
<td>1000</td>
<td>1.80</td>
<td>384</td>
</tr>
<tr>
<td>SiAlON</td>
<td>1100</td>
<td>0.85</td>
<td>315</td>
</tr>
<tr>
<td>Al$_2$O$_3$</td>
<td>1100</td>
<td>0.20</td>
<td>-1790</td>
</tr>
<tr>
<td>Mullite</td>
<td>1100</td>
<td>0.42</td>
<td>-594</td>
</tr>
</tbody>
</table>

In the XRD scans it was observed that all deposited f-Si layers are polycrystalline and no amorphous phase is present, since no diffraction intensity was observed between the diffraction lines of f-Si and of the substrate material.

In Figure 4.4 presents the scans with the (111) and (220) diffraction lines of the f-Si layers on SiAlON deposited at different temperatures.
Stress and structure of thin polycrystalline silicon films

![XRD scans of (111) and (220) diffraction lines](image)

**Figure 4.4:** XRD scans of the (111) and (220) diffraction lines of the f-Si layers on SiAlON deposited at different temperatures. $S_0$ refers to the angle of the strain-free state.

We observe a decrease of preferential orientation in [111] direction with increasing deposition temperature in the films deposited on the SiAlON substrate. The diffraction line at $\theta \approx 27^\circ$ is a line from the substrate, which can serve as an internal calibration reference. From the shifts of the peak position of the lines in reference to the theoretical values, we calculated the values for the macro stress according to Equation (4.3). The stress observed is tensile (positive sign of the macro stress) and decreases when the deposition temperature is increased.

The influence of the substrate material on diffraction lines is demonstrated in Figure 4.5.

![XRD scans of (111) and (220) diffraction lines](image)

**Figure 4.5:** XRD scans of the (111) and (220) diffraction lines of the f-Si layers on mullite, Al$_2$O$_3$ and SiAlON. $S_0$ refers to the angle of the strain-free state.

The substrate has a strong influence on the macro stress, as demonstrated in Figure 4.5 by a shift of the peak position of the lines in
reference to the theoretical values. In the f-Si layers deposited on mullite and Al₂O₃ compressive stress is observed (negative sign of the macro stress). It is interesting to note that the compressive stress in the layer on Al₂O₃ is one order of magnitude larger than the stress in the film on mullite (Table 4.1). The stress in the f-Si layer on Al₂O₃ could also be observed visually because the samples were bent. In the f-Si layers on SiAlON, the macro stress decreases with increasing deposition temperature. The intensities of (1 1 1) lines are not changed while the intensity of (2 2 0) lines is reduced in case of mullite and alumina. The calculation of the macro stress was done from the position of the (5 3 1) diffraction line, for which the theoretical calculated angle position 2θ is equal to 114.094 degrees.

Besides the macro stress and the preferential orientation we also determined the micro stress and the average grain size from the lines in the XRD scans of the f-Si layer. Most of these parameters were determined using a method proposed by Langford [7] and Delhez et al. [8].

Micro stress and the average grain size can be analysed from the broadening of the diffraction lines. The measured profile of the diffraction line, \( h \), of the specimen can be described as the outcome of a convolution of the structurally broadened profile \( f \), which is desired, and the profile \( g \) incorporating the broadening due to instrumental effects and the wavelength distribution. It is assumed that the shape of the \( h, g \) and \( f \) profiles conforms to a Voigt function, which is a convolution of Cauchy and Gaussian components [8]. To analyse the micro stress and average grain size, it is necessary to obtain the pure profile \( f \) and to separate it on the Gaussian and Cauchy parts. Micro stress is related to the integral breadth \( \beta \) and full width at half maximum \( 2w \) of the Gaussian part of the profile \( f \). The average grain size is equal to the integral breadth and full width at half maximum of the Cauchy part of the profile \( f \). The integral breadth is defined as

\[
\beta = \frac{A}{I_0} \tag{4.4}
\]

where \( A \) is the integrated intensity of the diffraction line and \( I_0 \) the intensity at its maximum. The integral breadths of the Gaussian and
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components of the Voigt function (of profile \( \beta \)), \( \beta_{\phi}^{I} \) and \( \beta_{\phi}^{II} \), respectively, are obtained from its \( 2w \) and \( \beta \) values according to [8]:

\[
\frac{\beta_{\phi}^{I}}{\beta} = 0.6420 + 1.4187 \left( \frac{2w}{\beta} - \frac{2}{\pi} \right)^{0.5} - 2.2043 \left( \frac{2w}{\beta} \right) + 1.8706 \left( \frac{2w}{\beta} \right)^2 \tag{4.5}
\]

\[
\frac{\beta_{\phi}^{II}}{\beta} = 2.0207 - 0.4803 \left( \frac{2w}{\beta} \right) - 1.7756 \left( \frac{2w}{\beta} \right)^2 \tag{4.6}
\]

Micro stress can be derived from the relation \( \sigma_{\mu} = \varepsilon_{\mu}E \) (Hook’s law), in which \( \varepsilon_{\mu} \) is the micro strain and \( E \) is the Young’s modulus. The average micro strain \( <\varepsilon_{\mu}> \) estimates are obtained from the Gaussian integral breadth of the \( f \) profile as follows:

\[
<\varepsilon_{\mu}> = \frac{\beta_{\phi}^{I}}{4 \tan \theta} \tag{4.7}
\]

The Gaussian integral breadth, \( \beta_{\phi}^{I} \), has to be taken in radians. The mean values for the micro strains in the grains of all \( f \)-Si layers are low and lie in the range of \( 10^5 \) to \( 10^4 \). From these low values it can be assumed that micro stress is negligible and that macro stress mainly contributes to the measured stress. Eventually, the measured macro stress can be defined as the residual stress in this system.

The average grain size \( <D> \) estimates are obtained from the Cauchy integral breadth of the \( f \) profile as follows:

\[
<D> = \frac{\lambda}{\beta_{\phi}^{I} \cos \theta} \tag{4.8}
\]

where \( \lambda \) is X-ray wavelength used (in our case CuK\( \alpha_1 \) radiation, \( \lambda = 0.154056 \) nm). The Cauchy integral breadth, \( \beta_{\phi}^{I} \), has to be taken in radians. The average grain size, \( <D> \), is analysed as described above for all deposited layers. The results of XRD analysis suggest that all investigated layers have relatively large grains. The layers deposited at 1100 \( ^{\circ} \)C have a width of the diffraction line comparable with the width of the used standard. A determination of the average grain size is therefore inaccurate, which means that an additional method has to be used to determine the grain size. Nevertheless it does mean that the average grain size in the perpendicular direction to the substrate is
several microns in these films. The average grain size of the f-Si layers deposited on SiAlON varies dramatically with the deposition temperature. The average grain size of 0.15 microns was determined for the layer deposited at 850 °C, 0.5 micron for the layer deposited at 900 °C, and 8.7 micrometer for the layer deposited at 1000 °C.

**4.4 Crystal morphology of film-silicon: TEM analysis**

The Transmission Electron Microscope (TEM) revealed more detailed information about the crystal grain structure of the layers. From each sample a cross section was prepared and analysed with a Philips CM30T transmission electron microscope operating at 300 kV. Cross sections of the layers were thinned to electron transparency by argon ion milling.

First we describe the temperature series on the SiAlON samples. Figure 4.6 shows representative TEM images of cross-sections of f-Si deposited on the SiAlON substrates at different deposition temperatures of 900 °C, 1000 °C and 1100 °C.

![Figure 4.6: TEM micrographs of f-Si on SiAlON substrates at several deposition temperatures.](image)

Further TEM analysis also showed that the deposited films are polycrystalline and that no amorphous regions are present. We observe from Figure 4.6 that at lower deposition temperature (900 °C), thin elongated crystals are grown in V-shaped regions. The crystals do not
Stress and structure of thin polycrystalline silicon films

grow fully across the layer thickness. At higher temperatures, the crystals grow more perpendicular to the substrate surface and the structure is more columnar. The crystals are present across the whole layer thickness. At 1100 °C all grains show a columnar structure. In summary, the width of the crystals increases with the deposition temperature and at the highest deposition temperature an average crystal size of 1-2 μm is estimated.

Several types of defects are observed in the f-Si layers. The type of defect that is observed most frequently is a twinned pair. Figure 4.7 shows a TEM photograph with a diffraction pattern of twin structures.

Figure 4.7: TEM photograph and diffraction pattern of area in f-Si with twinned pairs. f-Si layer is deposited on SiAlON at 900 °C.

The analysis of the TEM results has revealed that the amount of twinned pairs is higher at lower deposition temperatures. The opposite relation is observed for other defects such as dislocations. The film deposited at 1100 °C showed some sub grain boundaries and cracks.

The crystals in the f-Si layers on Al₂O₃ are elongated and present across the whole thickness of the deposited film. The morphology is columnar, comparable with the morphology of the films deposited on SiAlON at 1100 °C. The grains of the f-Si layers on the mullite substrate show an irregular structure. The crystals are elongated and their surface is rough, but there is no indication that the crystals are present throughout the whole thickness of the film. A summary of all TEM results is presented in Table 4.2.
Table 4.2: Summary of TEM results of the deposited f-Si layers. The grain size is just an indication.

<table>
<thead>
<tr>
<th>Substrate</th>
<th>Deposition temperature [°C]</th>
<th>Grain size (width x length) [μm x μm]</th>
<th>Grain shape</th>
<th>Defects</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiAlON</td>
<td>900</td>
<td>0.5 x 10 – 0.5 x 1.5</td>
<td>V-shaped and small columnar</td>
<td>+++</td>
</tr>
<tr>
<td>SiAlON</td>
<td>1000</td>
<td>2 x 10 – 1 x 2</td>
<td>Small V-shaped and columnar</td>
<td>++</td>
</tr>
<tr>
<td>SiAlON</td>
<td>1100</td>
<td>0.5 x 7 – 2 x 11</td>
<td>Columnar</td>
<td>+</td>
</tr>
<tr>
<td>Al₂O₃</td>
<td>1100</td>
<td>0.2 x 7 – 2 x 7</td>
<td>Columnar</td>
<td>+</td>
</tr>
<tr>
<td>Mullite</td>
<td>1100</td>
<td>0.3 x 6 – 2 x 6</td>
<td>V-shaped</td>
<td>+</td>
</tr>
</tbody>
</table>

4.5 Discussion

The method used for the determination of the macro stress is a simple method to apply when compared to the sin²ψ method. A drawback is the reduced accuracy of the obtained value for the macro stress. Therefore the method is mainly used to compare stress in different samples and to evaluate trends in stress evolution. For this purpose the trend of thermal stress on the deposition temperature was calculated for the SiAlON substrate according to Equation 4.1 and compared with the experimental value of the stress in the f-Si layers deposited at several temperatures on the SiAlON substrate. Figure 4.8 shows two graphs, in which both stresses are presented.
Stress and structure of thin polycrystalline silicon films

\[ \alpha_{\text{SiAlO}} = 4 \times 10^4 \text{ K}^{-1} \]
\[ \alpha_{\text{Si}} \text{ from EMIS dataviews, INSPEC} \]
\[ E_{\text{Si}} = 165.9 \times 10^9 \text{ Pa} \]
\[ \nu_{\text{Si}} = 0.217 \]

Figure 4.8: (a) Calculated values of thermal stress at room temperature with a model consisting of a film of monocrystalline silicon on a SiAlON substrate at different deposition temperatures according to Equation 4.1, (b) Measured values of macro stress with XRD of f-Si layers on SiAlON substrates deposited at varied temperatures.

The same values for Young’s modulus and Poisson’s ratio are used in the calculations of the thermal stress and in the calculations of the measured stress from the shifts of the peaks of the diffraction lines in the scan. The dependence of the thermal expansion coefficient of SiAlON on temperature was assumed to be small and is kept constant in the calculations. The values for Young’s modulus and Poisson’s ratio used in the calculations for the macro stress and thermal stress are those for monocrystalline silicon. We recalculated the values for the stresses with a Young’s modulus and Poisson’s ratio of very fine polycrystalline material \((E = 113 \text{ MPa}, \nu = 0.42 \text{ [9]}).\) The stresses shift to lower values but the trends as suggested by Figure 4.8 hold. The calculated values presented in Figure 4.8a approach the theoretical trend presented in Figure 4.2 most closely. As demonstrated in Figure 4.8b, the temperature dependence of the calculated thermal stress is opposite to the temperature dependence of the measured stress. At lower deposition temperatures the effect of thermal stress is lower, which suggests that the growth stress is higher and probably dominant at these temperatures in our samples. At higher temperatures the difference between the thermal and growth stress becomes less, indicating that the growth stress decreases at higher temperatures.
Similar calculations were performed for the f-Si layers deposited at several substrates at 1100 °C. Figure 4.9 presents the results of these calculations and the measured macro stress.

![Stress Graph](image)

**Figure 4.9:** Measured macro stress and calculated thermal stress of f-Si on different ceramic substrates. The deposition temperature for all three samples was 1100 °C.

The signs of both thermal stress and total stress are in the same direction. The method used for the determination of the macro stress suggests that the sign of the growth stress is also equal to the sign of thermal and total stress (Figure 4.9). However, using a Young's modulus and a Poisson's ratio of very fine polycrystalline material results in a change of the sign for growth stress for the f-Si layer on the Al₂O₃ substrate. The interpretation of the absolute values is inaccurate, but trends for the residual stress dependency on deposition temperature and substrate material still hold.

We expect that the growth stress in our samples is caused by a combination of several items listed in paragraph 4.2, some of which we observe in our f-Si layers, like twinned pair structures. The exact contribution of each item to the total growth stress remains unknown. The twinned pairs that are observed in the TEM analysis are assumed to be one of the contributions to the growth stress.

The XRD and TEM analyses demonstrate that with increasing deposition temperature the grain size increases, which leads to a
Stress and structure of thin polycrystalline silicon films
decreased grain boundary area per volume. This can indicate that the
amount of grain boundaries per volume also affects the growth stress. It
has been reported that an elimination of grain boundaries in
recrystallization experiments reduces the observed stress [2]. We also
observe a lower value for the measured macro stress at higher
deposition temperatures, at which larger grains are deposited.

The exact values for the grain size are difficult to determine, since
the grain size is not homogeneous across the thickness of the f-Si films.
The largest crystals are in the upper part of the film and the smallest
ones are at the interface with the substrate. In the upper part of the film,
crystal sizes up to several micrometers have been observed.

4.6 Conclusions

The structure of the f-Si layers deposited by thermal CVD on the
ceramic substrates (SiAlON, Al₂O₃, and mullite) was investigated. The
silicon films on all substrates are compact and uniform.

The type of substrate strongly influences the stress and the texture of
the films. In the silicon films deposited on SiAlON substrate tensile
stress is observed, while in the films deposited on mullite and alumina
substrates compressive stress is present. In all deposited films the
observed stress is higher than the thermal stress, which has been
determined from the differences in the thermal expansion coefficients
of the film and substrate materials. We observe in the films grown on
SiAlON substrate that the total stress decreases with increasing
deposition temperature, which implies a reduction of the growth stress
in the films. We ascribe the reduction of the growth stress to a lower
defect formation at higher deposition temperatures. The observed
twinned pairs represent one of the main contributions to the growth
stress. Other contributions to the growth stress are grain boundaries,
void formation, and expected recrystallization during growth. The
silicon films exhibit a texture, which reduces at higher deposition
temperatures. We also observe that at higher deposition temperatures
the crystallite size is larger and the crystal growth is columnar.
4.7 References


Stress and structure of thin polycrystalline silicon films
This chapter reports on a simulation study on film-silicon solar cells. Computer simulations have been used to gain more understanding of device design issues and physics of a film-silicon solar cell. The computer program PC1D has been used to carry out solar cell simulations.
5.1 Introduction

In this chapter we discuss results of a computer simulation study of f-Si solar cells. Computer simulations can be very helpful to design the solar cell. To gain more understanding in designing the device, knowledge about the effect of several device and material parameters on the photovoltaic conversion efficiency is necessary. We used a commercially available computer programme, PC1D version 5.3, for this purpose [1]. This programme is especially developed for the simulation of mono- and multi-crystalline silicon solar cells. It includes models that describe the dependencies of material properties on temperature, dopant concentration and electric fields in the device. Some discussion whether the same models can be used to describe the f-Si material is necessary. The main difference between the f-Si material and the mono- and multi-crystalline silicon material is the average grain size of the material. The average grain size in the as-deposited CVD material is in the range of 1–5 μm. When recrystallization methods like ZMR are used, the grain size can be increased to sizes comparable to the grains in multi-crystalline silicon. The size of the grains directly influences the electronic properties of the material. Parameters like the carrier mobility and the minority carrier lifetime are influenced by the size of the grains. The PC1D programme needs values for the carrier mobility and for the lifetime of minority carriers. These values are obtained experimentally. The values for these parameters used for simulation of polycrystalline f-Si solar cells cannot be seen as values of pure material parameters, but must be seen as effective values that also depend on physical device parameters. E.g. variations and gradients in the electronic properties due to crystallographic variations across the layer are included in the effective values.

The computer simulations were carried out in order to gain understanding of the behaviour of the solar cell on several material and device parameters. Since no exact values for the minority carrier lifetime of f-Si are known, we used values from an interval in which the minority carrier lifetime of f-Si is expected. The results of the calculations can be used to obtain starting values for solar cell processing, like thickness of the base layer and dopant concentrations.
5.2 PC1D

PC1D is a computer program written for IBM-compatible computers that solves the fully coupled time-dependent non-linear equations for the one-dimensional (1D) transport of electrons and holes in crystalline semiconductor devices with particular applications to photovoltaic devices. The program has played an important role in enhancing the understanding of the device physics of solar cells, especially monocrystalline silicon solar cells, and has become a world standard for modelling of photovoltaic devices based on crystalline semiconductors, such as silicon, germanium and gallium arsenide. The program is supported and distributed by the Photovoltaics Special Research Centre at the University of New South Wales in Sydney, Australia [1].

The device model of PC1D is based on the two-carrier semi classical semiconductor transport equations. These equations are derived from the Boltzmann transport equation with the following assumptions: the two carriers flow independently (no carrier-carrier scattering), both carrier populations remain in thermal equilibrium with the surrounding crystal lattice (no hot carriers), the mobility of carriers is isotropic, the structure of the energy levels available to electrons is not significantly affected by excitation (rigid bands). The effect of magnetic fields and the device temperature are assumed to be uniform [2]. Both the bulk recombination model and the surface recombination model are based on a single adjustable energy level within the band gap using SRH statistics.

PC1D calculates the photo-generation rate within the device. At each incident wavelength, after accounting for incident-surface reflection, the light absorption in the silicon is calculated. Optical confinement is included within the device model of PC1D. A texture at the front surface can be defined and the internal reflection at both the front and backside can be defined to introduce light capturing in the silicon layer.

Only one-dimensional structures can be simulated within PC1D. The basic device structure used for the calculations is schematically drawn in Figure 5.1.
Device structure analysis

Figure 5.1: Schematic drawing of the simulated solar cell.

The base layer is a p-type layer of silicon deposited on the substrate. The emitter is applied by diffusion of phosphorus in the base layer. The *pn-junction* is formed at the interface of the p-type base layer and the n-type emitter at the top region of the base layer.

The next sections will present the calculations and evaluate several important device parameters. Since we are working on film-silicon solar cells, the thickness of the active layer is a very important parameter to be evaluated. The emitter is in general very thin, so the thickness of the active layer is approximately equal to the thickness of the base layer. The thickness of the base layer will be evaluated with respect to the quality of the material, which is described by the diffusion length of the minority carriers in this base layer. A CVD method to deposit the base layer gives us the possibility to control of thickness accurately. This way we can adjust the thickness in relation to the carrier lifetime to get the highest conversion efficiency possible.

The emitter will be diffused into the silicon layer from the front surface using a phosphorus source. Since the structure of the silicon material is different from the mono- or multicrystalline silicon, evaluation of several parameters of the emitter is useful. These simulations are mainly performed to get basic understanding about the behaviour of the photovoltaic conversion efficiency on variation in the emitter parameters, such as the depth of the diffusion and the donor concentration.

At the back surface the silicon is in direct contact with the ceramic substrate or a barrier layer. Such interfaces are usually characterized by high surface recombination velocities. A highly doped layer at the back surface can prevent recombination of the generated carriers. Parameters of such a highly doped layer that are investigated during the calculation
are the thickness, the acceptor concentration, the back surface recombination velocity and the carrier lifetime.

The minority carrier diffusion length is related to the minority carrier lifetime. Since no exact values for the minority carrier lifetime are known, we have chosen the minority carrier lifetime as a parameter in the simulations. The value of the minority carrier lifetime was varied from 0.01 µs to 10 µs. In the device simulator PC1D the influence of the dopant concentration and device temperature on the carrier lifetime (τ), the carrier mobility (μ) and the surface recombination velocity (S) are incorporated. The temperature of the device is kept constant within this study and the influence of the temperature variation is not considered in detail. Since the dopant concentration influences the carrier lifetime and the carrier mobility, the minority carrier diffusion length will be changed. Figure 5.2 shows the calculated diffusion length as function of the acceptor concentration. \( L_0 \) is the initial diffusion length when no influence of dopants is present. The same relation is used for donor atoms. The chosen values are just examples and the related minority carrier lifetime is within the range mentioned above.

![Diagram showing calculated diffusion length with acceptor concentration](image)

**Figure 5.2:** Calculated relation of the minority carrier diffusion length with the acceptor concentration.

We only illustrate the influence of the acceptor concentration on the diffusion length, because this is a very important parameter within this study. The values for the remainder of the mentioned input parameters represent the initial values \((μ_0, ν_0, S_0)\), which do not depend on the
Device structure analysis

dopant concentration and the device temperature, unless indicated otherwise.

A basic set of parameters used during the calculations is presented in Table 5.1.

**Table 5.1**: Parameters used for calculations. Most of these are the same as those used for a standard crystalline silicon solar cell.

<table>
<thead>
<tr>
<th>Device:</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Area 100 cm$^2$</td>
</tr>
<tr>
<td>• Shunt conductivity: 3.3 Ω$^{-1}$.cm$^{-1}$</td>
</tr>
<tr>
<td>• Series resistance: 0.015 Ohm</td>
</tr>
<tr>
<td>• Reflection/shadow loss at front surface: 10 %</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Emitter:</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Peak donor concentration $1 \times 10^{20}$ P/cm$^3$</td>
</tr>
<tr>
<td>• Junction depth 0.5 μm</td>
</tr>
<tr>
<td>• Type of diffusion: erfc in monocrystalline silicon</td>
</tr>
<tr>
<td>• Reflection on the inner emitter surface, 10 %</td>
</tr>
<tr>
<td>• Reflection on the external emitter surface, 10 %</td>
</tr>
<tr>
<td>• Surface recombination velocity at the emitter, $1 \times 10^6$ cm/s</td>
</tr>
<tr>
<td>• Front surface texture depth 3 μm</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Base layer:</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Thickness 20 μm</td>
</tr>
<tr>
<td>• Base acceptor concentration $1 \times 10^{17}$ B/cm$^3$</td>
</tr>
<tr>
<td>• Bulk lifetime range 0.001 μs – 10 μs</td>
</tr>
<tr>
<td>• Carrier mobility model as used in PC1D with $\mu_{\text{electrons}}^{\text{max}} = 200$ cm$^2$/Vs and $\mu_{\text{holes}}^{\text{max}} = 100$ cm$^2$/Vs</td>
</tr>
<tr>
<td>• Reflection on the inner back surface, 70 % diffuse</td>
</tr>
<tr>
<td>• Surface recombination velocity at the back surface, $1 \times 10^5$ cm/s</td>
</tr>
</tbody>
</table>

### 5.3 Calculations

#### 5.3.1 Ideal pn-junction

For a general view on the dependence of the photovoltaic conversion efficiency on variation of the base layer thickness and the minority carrier diffusion length, we will first consider an ideal pn-junction solar cell. A schematic presentation of the ideal pn-junction solar cell is presented in Figure 5.3.
Figure 5.3: Schematic presentation of the ideal pn-junction solar cell. \( N_A \) and \( N_D \) are the acceptor and donor concentrations, \( L_e \) and \( L_h \) de diffusion length of the minority carriers of electrons and holes respectively, \( S_e \) and \( S_h \) are the surface recombination velocities for electrons at the back and holes and at the front surface respectively, \( W_N \) and \( W_P \) represent the thickness of respectively the emitter (n-region) and the base layer (p-region). The thickness of the base layer is in most cases approximately equal to \( W_P \) since \( W_N \) is usually very small.

The current-voltage characteristic of such an ideal illuminated pn-junction solar cell is defined as [3]:

\[
I(V) = I_0 \left( \exp \left( \frac{qV}{kT} \right) - 1 \right) - I_L
\]  

(5.1)

where \( V \) is the applied voltage, \( I_L \) is the light generated current and \( I_0 \) the diode saturation current, which is given by:

\[
I_0 = A \left( \frac{qn_e^2 D_e}{N_A L_e} + \frac{qn_h^2 D_h}{N_D L_h} \right)
\]  

(5.2)

where \( D_e \) and \( D_h \) is the diffusion coefficient of the minority carriers and \( A \) the area of the solar cell. The diffusion length of a minority carrier is related to the minority carrier lifetime and the diffusion coefficient according to:

\[
L_{\text{diffusion}} = \sqrt{D \tau}
\]  

(5.3)

where the diffusion coefficient of minority carriers, \( D \), is determined by the carrier mobility of the minority carriers, \( \mu \), via the Einstein relation:

\[
D = \frac{\mu kT}{e}
\]  

(5.4)
An important external parameter of a solar cell is the photovoltaic conversion efficiency. This conversion efficiency of a photovoltaic device is defined [3] by the following equation:

\[
\eta = \frac{V_{oc}I_{sc}FF}{P_{in}}
\]  

(5.5)

with \( P_{in} \) the total power of the incident light, \( FF \) the fill factor of the \( I(V) \) characteristic, the \( I_{sc} \) the short-circuit current and \( V_{oc} \) the open circuit voltage. The short circuit current is defined from Equation 5.1 at an applied voltage of 0V which makes \( I_{sc} = I_L \). The \( V_{oc} \) is defined as:

\[
V_{oc} = \frac{kT}{q} \ln \left( \frac{I_L}{I_0} + 1 \right)
\]  

(5.6)

The model used for the ideal case implicitly assumes that the solar cell extends an unlimited distance on either side of the junction. This is never the case with actual devices. To adjust the ideal model for the finite dimensions of the solar cells a geometry factor is added which incorporates the thickness of the p- and n-type regions, the minority carrier lifetimes in both regions and the surface recombination velocities at the surfaces according to:

\[
I_o = A \left( \frac{q \eta D_L G_p}{N_A L_e} + \frac{q \eta D_L G_n}{N_D L_n} \right)
\]  

(5.7)

and \( G_p \) and \( G_n \) are the geometry factors for the p-type and n-type regions, respectively and are defined as follows [3]:

\[
G_p = \frac{\left( \frac{S_h L_e}{D_e} \right) + \tanh \left( \frac{W_p}{L_e} \right)}{1 + \left( \frac{S_h L_e}{D_e} \right) \tanh \left( \frac{W_p}{L_e} \right)} \quad \quad G_n = \frac{\left( \frac{S_h L_e}{D_e} \right) + \tanh \left( \frac{W_p}{L_e} \right)}{1 + \left( \frac{S_h L_e}{D_e} \right) \tanh \left( \frac{W_n}{L_e} \right)}
\]  

(5.8)

In case of f-Si solar cells, where the thickness of the silicon layer is several times smaller than that in mono- and multi-crystalline silicon solar cells, the geometry factor plays an important role.

The influence of the geometry factor on the total diode saturation current of the solar cell will be illustrated. The contribution of the emitter must not be neglected, but is more complicated since the emitter
always has a non-uniform donor concentration profile. The geometry factor of the base layer, $G_p$, calculated from Equation 5.4, is presented in Figure 5.4:

![Figure 5.4: Geometry factor of the base layer as a function of the base thickness/diffusion length relationship.](image)

If the thickness of the base layer is larger than twice the diffusion length of the minority carriers, then the surface recombination no longer has an effect on the dark current. The geometry factor is always 1 (Region I). However, if the thickness of the base layer is less than twice the diffusion length of the minority carriers, the dark current is dependent on the surface recombination (Region II). Only when the geometry factor is smaller than 1, the dark current decreases, the circuit voltage increases according to Equation 5.7 and the photovoltaic conversion efficiency of the solar cell is increased. This means that the surface recombination must be as low as possible.

### 5.3.2 Acceptor concentration in the base layer

During the fabrication of the base structure it is important to know the optimal acceptor concentration. Therefore calculations in which the acceptor concentration is evaluated for the highest photovoltaic conversion efficiency are indispensable. Figure 5.5 presents the results of calculations in which the minority carrier lifetime and the acceptor concentration in the base layer were varied.
Figure 5.5: Contour plot with calculated efficiencies as function of the acceptor concentration in the base layer and minority carrier lifetime. The minority carrier diffusion length is also presented. The thickness of the base layer was 20 μm and the back surface recombination velocity $10^5$ cm/s.

From Figure 5.5 it can be concluded that an acceptor concentration around $2 \times 10^{17}$ B/cm$^3$ can be considered as an optimum. This optimum for the acceptor concentration stays at this value for the range of base layer thicknesses from 5 μm to 50 μm. It is important to note that when the minority carrier lifetime in the base layer is lower than 0.1 μs, the efficiency of the solar cell becomes less sensitive to the acceptor concentration in the base layer.

### 5.3.3 Thickness of the base layer

In the next section, we analyse the dependence of the photovoltaic conversion efficiency of film-silicon solar cells on the thickness and the minority carrier diffusion length with PC1D. Within these calculations both the minority carrier lifetime and thickness of the base layer are varied.

It has already been proven that film-silicon solar cells can give efficiencies that can be compared with the convention crystalline silicon solar cells [4]. Because thin films of silicon are used for solar cells, the
The electronic quality of the film can be less high. Since the thickness of the film-silicon solar cell is smaller than that of the present generation of crystalline silicon solar cells, it is expected that the diffusion length of the minority carrier can be shorter.

In paragraph 5.3.1 we presented the dependence of the diode saturation current on the thickness and the surface recombination in an ideal pn-junction solar cell. The optimal thickness of a certain f-Si material therefore depends on the surface recombination velocity, the electron diffusion coefficient and the minority carrier diffusion length. The optimal thickness is determined for a base layer material that is characterized by a particular minority carrier diffusion length that gives the maximum photovoltaic conversion efficiency. In the following calculations, the relation between the optimal thickness, the minority carrier diffusion length and the surface recombination velocities is analysed. First we will consider the influence of the back surface recombination velocity on the photovoltaic conversion efficiency. Figure 5.6 shows the calculated efficiencies at varied back surface recombination velocities at different minority carrier diffusion lengths.

![Graph showing efficiency vs. back surface recombination velocity](image)

**Figure 5.6** Calculated efficiencies with PC1D at varied recombination velocities at the back and front surface. No BSF layer was applied. The base layer thickness is kept constant at 10 \( \mu \text{m} \).

The calculations show that at lower surface recombination velocities the conversion efficiency is higher. A back surface recombination velocity lower than 100 cm/s is necessary for highly efficient solar cells. Two
Device structure analysis

regions can be distinguished in which the conversion efficiency is almost independent of variation of the back surface recombination velocity. These regions are below 100 cm/s and above $10^5$ cm/s. For basic understanding of the behaviour of the solar cell, it is sufficient to determine the dependencies of the photovoltaic conversion efficiency on the minority carrier diffusion length and the thickness of the base layer at two values for the back surface recombination velocity.

The following calculations in which the thickness and carrier lifetime are varied were carried out in two limiting situations with a high and a low back surface recombination velocity, respectively $10^5$ and 10 cm/s. Both values for the back surface recombination velocity are in the regions where the photovoltaic conversion efficiency is independent of the back surface recombination velocity. Figure 5.7 presents graphs of calculated efficiencies at varied base layer thickness and two different minority carrier diffusion lengths.

![Graph](image)

**Figure 5.7:** Calculated efficiencies with PC1D at varied base layer thickness and different minority carrier diffusion lengths. The acceptor concentration in the base layer was $1 \times 10^{17}$ B/cm$^3$.

For both values of the back surface recombination velocity, an optimal thickness can be found for each minority carrier diffusion length, which results in the maximum efficiency. This means that there is an optimal base layer thickness for each combination of $L_e$ and $S_e$, which yields the highest possible efficiency of a f-Si layer. Figure 5.8 shows the relation of the optimal thickness of the base layer as function of the minority carrier diffusion length for two back surface recombination velocities.
The thickness of the base layer is kept within the range of 1 – 100 μm. In the upper graph the calculated maximal efficiency that corresponds to the optimal thickness of the base layer is presented.

![Graph](image)

**Figure 5.8:** Calculated relation of the optimal thickness of the base layer with the carrier diffusion length and its efficiency at two values for the back surface recombination velocity.

This graph gives information about the optimal thickness that should be used when deposited f-Si material is characterized by a particular minority carrier diffusion length. In the upper graph the corresponding efficiency can be found. When we analyse the relation of the minority carrier diffusion length with the optimal thickness of the base layer we roughly observe a linear relation. When the back surface recombination velocity is low ($S_e = 10$ cm/s), the optimal thickness is smaller than the minority carrier diffusion length (factor $\sim 0.6$). When the value for the back surface recombination velocity is high ($S_e = 10^5$ cm/s), the optimal thickness is approximately three times the value of the minority carrier diffusion length and the obtained efficiency is lower at the same minority carrier diffusion length. This means that when there is a surface with a low recombination velocity, less silicon is needed to get the same efficiency with the material of the same electronic quality.
5.3.4 Emitter

Besides knowledge about the effect of several parameters of the base layer on the solar cell performance, similar information about the emitter is required. The emitter is usually very thin, but since it is the region closest to the front surface, where the absorption of light is very high, the optimal design of the emitter is important in order to prevent large recombination of the photo-generated carriers. The high absorption at the front of the solar cell is demonstrated by the generation profile, which is presented in Figure 5.9.

![Generation rate profile](image)

**Figure 5.9:** The generation rate profile in the f-Si solar cell with a thickness of 20 µm calculated with PC1D (AM 1.5 spectrum).

In most crystalline silicon solar technologies, the pn-junction is obtained by forming an n-type layer at the top surface of the p-type base. To create this n-type layer, phosphorus is diffused into the base layer using gaseous or paste-like sources containing phosphorus. Phosphorus is an electron donor in silicon. These conventional techniques are also applicable for the f-Si solar cell. The consideration about the influence of the geometry factor of the base layer can also be applied for the emitter. Since the emitter does not have a uniform donor concentration profile, the situation is more complicated, than that for the base layer, which has a uniform acceptor concentration profile. The diffusion length, the front surface recombination velocity and the “depth” of the emitter determine the effectiveness of the emitter. In an efficient emitter in monocrystalline silicon solar cells, the generated
carriers in the emitter are not completely lost due to recombination in
the bulk or at the surface. The most important parameters of the emitter
are:

- The concentration profile
- The peak donor concentration at the surface \(N_0\)
- The front surface recombination velocity \(S_f\).

The concentration profile used in the calculations is the Erfc function:

\[
N(x) = N_0 \text{erfc} \left( \frac{x - x_p}{x_d} \right)
\]  

(5.9)

where \(x_d\) is the depth factor, and \(x_p\) is the peak position of the dopant
concentration, all of which are adjustable. In our case \(x_p\) is set to zero,
because the source of dopant atoms is assumed to be at the surface,
which is true for all conventional emitters.

Both the peak donor concentration and the diffusion profile of the
emitter are two parameters of which the influence on the efficiency
needs to be evaluated. In the PC1D device model the peak
concentration at the surface and depth factor were varied. The depth
factor is used to control the “depth” of the emitter and so the junction
depth of the formed diode. The junction depth is defined as the depth at
which the concentration of both donor and acceptor atoms is equal.
Figure 5.10 presents the junction depth at different peak dopant
centrations of the emitter as function of the depth factor.

![Figure 5.10: Relation of the depth factor with the junction depth of the
diffused emitter for different peak donor concentrations. The
acceptor concentration of the base layer was \(1 \times 10^{17} \text{ B/cm}^3\).

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Calculated concentration profiles used within this chapter are presented in Figure 5.11. The dopant concentration of the boron atoms in the base layer is also included.

![Diagram showing dopant concentrations](image)

**Figure 5.11:** Dopant concentrations of both phosphorus and boron atoms in the base layer. The phosphorus atoms are diffused into the base layer from the front surface. The peak donor concentration was $2 \times 10^{20} \text{ P/cm}^3$.

The junction depths in conventional crystalline solar cells are typically in the range of 0.2 - 0.5 μm [3]. The average junction depth in f-Si solar material will be larger, since preferential diffusion of the donor atoms along the grain boundaries occurs [5].

The efficiency of the solar cell was calculated for several depth factors and several peak donor concentrations. The results of the calculations are presented in Figure 5.12.
Figure 5.12: Contour plot with calculated efficiencies for different depth factors and donor concentrations of the emitter. The acceptor concentration of the base layer was $1 \times 10^{17}$ B/cm$^3$ and the front surface recombination velocity was $1 \times 10^6$ cm/s. The thickness of the base layer and $L_0$ were both 20 μm.

The highest efficiencies are obtained with very shallow emitters. The optimal peak donor concentration shifts to lower concentrations when the diffusion depth of the emitter is increased.

The influence of the peak donor concentrations and the penetration depth on the photovoltaic efficiency has been evaluated for one value of the front surface recombination velocity. Similar to the thickness of the base layer, the surface recombination at front surface is of importance. Near this front surface, most excess carriers are generated, so the front surface recombination is very important. Figure 5.13 presents the results of efficiency calculations for different donor concentrations and front surface recombination velocities. Both the thickness of the base layer and the initial minority carrier diffusion length $L_0$, which is independent of the dopant concentration, were 20 μm.
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Figure 5.13: Calculated efficiencies of the film-silicon solar cell at different peak donor concentrations of the emitter and at different front surface recombination velocities. The thickness of the base layer and $L_e$ were 20 $\mu$m.

The efficiency increases when the front surface recombination is reduced. This change in efficiency is also observed for all calculations with different depth factors. It can be concluded that the front surface recombination velocity of $10^3$ cm/s or lower is sufficiently low for an optimal efficiency.

The effect of lowering the front surface recombination can also be illustrated with the quantum efficiency. The quantum efficiency of a photovoltaic device is determined for radiation with light of different wavelengths. Since the short wavelength light (blue light) is predominantly absorbed in the emitter, the current that is generated in this region can show very clearly the influence of the front surface recombination velocity. Figure 5.14 shows the calculated internal quantum efficiencies for two different front surface recombination velocities.
Figure 5.14: Calculated internal quantum efficiencies of film-silicon solar cells for different front surface recombination velocities. Peak donor concentration: $2 \times 10^{20}$ P/cm$^3$, depth factor: 0.2 \( \mu \text{m} \) (!), The thickness of the base layer and $L_n$ are 20 \( \mu \text{m} \).

In case of a high surface recombination velocity, the quantum efficiency at short wavelengths is reduced. In case of a low front surface recombination velocity, the quantum efficiency is hardly affected. Most of the generated holes reach the pn-junction and are collected. The depth factor in these calculations was decreased from 0.5 to 0.2 to demonstrate the effect of the front surface recombination velocity on the quantum efficiency of a solar cell. In practice the emitter will be larger.

All presented calculations assumed that the junction depth of the emitter is the same for the whole area of the cell. However, when polycrystalline silicon material is used, preferential diffusion along the grain boundaries in the f-Si material will result in a non-uniform emitter [6]. Phosphorus spikes along the grain boundaries are present. These spikes can stretch far below the rest of the emitter. Preferential phosphorus diffusion need not be detrimental to the performance of the solar cell, however. The vertical junctions which are created by preferential diffusion cause that the effective area of the emitter increases, which can enhance the collection of generated free carriers [7].
5.3.5 Back surface field

It has been demonstrated that recombination at the front and back surfaces is one of the sources of efficiency losses. With respect to the base structure of a film-silicon solar cell, silicon is deposited directly on a ceramic substrate or barrier layer material. The interface between the ceramic material and the deposited surface usually shows very high recombination velocities. A way to reduce the influence of the back surface recombination velocity is using a back surface field (BSF), which can be formed in a junction between highly and lightly doped silicon materials of the same dopant type. To create such a high-low junction in f-Si solar cells, a highly doped f-Si layer is deposited on the substrate, which will be referred to as the back surface layer (BSL). On top this layer the less doped base layer is deposited and the high-low junction is formed. The device structure with a BSL is schematically drawn in Figure 5.15.

![Diagram of a device structure with a back surface field layer](image)

Figure 5.15: Schematic drawing of the device structure with a back surface field layer as used in the calculations.

This structure is also used for the calculations with the device simulator program.

Since deposition occurs at a relatively high temperature, diffusion of acceptor atoms from the BSL into the base layer can be expected. A diffusion profile in the base layer where the BSL as the source for diffusion is incorporated in the model. A band diagram of a f-Si solar cell that consists of a 10 μm base layer on a 1 μm BSL is drawn in Figure 5.16.
Figure 5.16: Energy bands of a f-Si solar cell with a back surface field. The thickness of the base layer is 20 \( \mu \text{m} \) and the thickness of the BSF layer is 5 \( \mu \text{m} \). The diffusion profile of both the emitter atoms and the boron atoms from the BSL into the base layer is Erfc.

The BSF causes a repulsion of minority carriers that diffuse from the base layer towards the BSL. On the other hand, carriers that are generated in the field of the high-low junction will be pushed into the base layer by the electric field. The generated carriers in the BSL that are able to reach the high-low junction by diffusion will drift into the base layer.

The most important parameters for the BSL are:
- The thickness \( (W_{BSL}) \),
- The acceptor concentration \( (N_A^{BSL}) \),
- The minority carrier lifetime of the electron,
- The back surface recombination.

To analyse the parameters of the BSL, we will consider an abrupt high-low junction, so one without the diffusion of acceptor atoms. An effective surface recombination velocity, \( S_{\text{e,eff}} \), can be introduced at the edge of the BSF as a substitution of the complete BSL, including all of its parameters. In case of the abrupt high-low junction, \( S_{\text{e,eff}} \) is approximately positioned at the interface of the high-low junction. In Figure 5.17 a schematic drawing of the simplified approach is presented.
Godlewski et al. [8] derived an expression for the effective recombination velocity of a homogeneously doped BSL. For the exact derivation of the expression for $S_{e\text{eff}}$, see reference [8]. $S_{e\text{eff}}$ is defined as:

$$S_{e\text{eff}} = \frac{N_{A}^{\text{base}}}{N_{A}^{\text{BSL}}} D_{\text{BSL}} G_{\text{BSL}}$$  \hspace{1cm} (5.10)$$

with $N_{A}^{\text{BSL}}$ the acceptor concentration in the BSL, $L_{\text{BSL}}$ and $D_{\text{BSL}}$ respectively the minority carrier diffusion length and the electron diffusion coefficient in the BSL and $G_{\text{BSL}}$ the geometry factor of the BSL, which is expressed as:

$$G_{\text{BSL}} = \frac{\left(\frac{S_{e}L_{\text{BSL}}}{D_{\text{BSL}}}\right) + \tanh \left(\frac{W_{\text{BSL}}}{L_{\text{BSL}}}\right)}{1 + \left(\frac{S_{e}L_{\text{BSL}}}{D_{\text{BSL}}}\right)tanh \left(\frac{W_{\text{BSL}}}{L_{\text{BSL}}}\right)}$$ \hspace{1cm} (5.11)$$

where $W_{\text{BSL}}$ is the width (or thickness) of the BSL and $S_{e}$ the back surface recombination velocity. The expression for the geometry factor of the BSL, $G_{\text{BSL}}$, is similar to Equation 5.8 with same values as presented in Figure 5.4. To include the effect of band gap narrowing, $\Delta E_{g}$, the acceptor concentration of the BSL will replaced by an effective acceptor concentration, $N_{A,\text{eff}}^{\text{BSL}}$ and is expressed as [9]:

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\[ N_{\text{eff}}^{\text{BSL}} = N_{\text{A}}^{\text{BSL}} \exp \left( \frac{\Delta E_{\text{g}}}{kT} \right) \]  
(5.12)

The effective recombination velocity is now expressed as:

\[ S_{v,\text{eff}} = \frac{N_{\text{A}}^{\text{base}}}{N_{\text{A,eff}}^{\text{BSL}}} \frac{D_{\text{BSL}}}{L_{\text{BSL}}} G_{\text{BSL}} \]  
(5.13)

The \( S_{v,\text{eff}} \) in fact describes a virtual surface recombination at the surface base layer and is dependent on all parameters of the BSL, including the actual back surface recombination velocity \( S_v \). As an example we will consider a f-Si solar cell with a back surface recombination of \( 10^5 \text{ cm/s} \).

The effective surface recombination velocity can be calculated according to Equation 5.13 and is presented in Figure 5.18 for different thicknesses of the BSL and different acceptor concentrations. Note that we consider an abrupt high-low junction and that \( S_{v,\text{eff}} \) is calculated at a distance equal to the thickness of the BSL from the back surface!

![Figure 5.18](image)

**Figure 5.18:** Calculated effective surface recombination velocities at the edge of BSL at varied acceptor concentrations and thicknesses of the BSL. The back surface recombination velocity was \( 10^5 \text{ cm/s} \).

For an effective BSL, the effective surface recombination must always be lower than the actual back surface recombination velocity: \( S_{v,\text{eff}} < S_v \). The calculated effective recombination velocity in Figure 5.18 (which is at the edge of the abrupt high-low junction) is in every case smaller than the actual back surface recombination velocity for the range acceptor concentrations. In this situation the back surface field is
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effective enough and will result in an increase in efficiency. The most effective BSF will be formed when \( S_{\text{eff}} \) is minimal (see Figure 5.18). This optimal acceptor concentration changes to higher values when the thickness of the base layer becomes thinner. It can also be observed that an effective BSL is thin.

Since \( S_{\text{e,eff}} \) is dependent on \( S_e \), a crossover point can be determined where \( S_{\text{e,eff}} \) equals \( S_e \). For an abrupt high-low junction, a value for \( S_{\text{e,cross}} \) is given by:

\[
S_{\text{e,cross}} = \left( \frac{N_{\text{base}}}{N_{\text{A,eff}}} - 1 \right) + \sqrt{\left( 1 - \frac{N_{\text{base}}}{N_{\text{A,eff}}} \right)^2 + 4 \frac{N_{\text{base}}}{N_{\text{A,eff}}} \tanh^2 \left( \frac{W_{\text{BSL}}}{L_{\text{BSL}}} \right)}
\]

\[
2 \frac{L_{\text{BSL}}}{D_{\text{BSL}}} \tanh \left( \frac{W_{\text{BSL}}}{L_{\text{BSL}}} \right)
\]

When \( S_e \) is higher than \( S_{\text{e,cross}} \) the effective surface recombination velocity will always be lower than the actual back surface recombination velocity (\( S_{\text{e,eff}} < S_e \)). Only in this situation a BSF layer will be effective. When the actual back surface recombination velocity is below the \( S_{\text{e,cross}} \), a BSL will have a negative effect on the photovoltaic conversion efficiency. In Figure 5.19 \( S_{\text{e,cross}} \) is calculated using Equation 5.14 as a function of the acceptor concentration. The acceptor concentration of the base layer was \( 1 \times 10^{17} \) B/cm\(^2\), \( L_0 = 21.2 \) \( \mu \)m. Values for the bandgap narrowing and diffusion length were obtained from the models used for PC1D.

![Figure 5.19](image)

**Figure 5.19:** Calculated values of \( S_{\text{e,cross}} \) where Equation 5.14 is used as a function of the acceptor concentration in the BSF layer. \( N_{\text{A,base}} = 1 \times 10^{17} \) B/cm\(^2\), \( L_0 = 21.1 \) \( \mu \)m, \( W_p = 20 \) \( \mu \)m.
The calculated values for $S_{c\text{\,cross}}$ are in most cases much lower than the actual value for the back surface recombination velocity $S_c$, because values for $S_c$ of $10^4$ cm/s and higher are usually present at such interfaces. This means that in most practical situations, application of a BSL will have a positive effect on the photovoltaic conversion efficiency. In cases where $S_c$ is lower than 1000 cm/s, the application of a BSL is not effective at all.

The effect of a BSL can also be demonstrated by comparing the internal quantum efficiencies in the different situations. In this case we consider a BSF layer with a thickness of 1 μm and an acceptor concentration of $1 \times 10^{19}$ B/cm$^3$. The actual back surface recombination velocity is $10^5$ cm/s. The thickness of the base layer is 20 μm. Using Figure 5.18 we find an $S_{c\text{\,eff}}$ of 3000 cm/s for the BSL with a thickness of 1 μm at an acceptor concentration of $1 \times 10^{19}$ B/cm$^3$. According to what is described above, the situation with the defined BSL should give efficiencies that are comparable to those of the situation without a BSL but with a back surface recombination velocity of 3000 cm/s. In Figure 5.20 we compare the quantum efficiency curves of the three situations described above. For comparison, the quantum efficiency curve of a solar cell without a BSL and with a high recombination velocity, $S_c$, of $10^5$ cm/s is added.

![Figure 5.20: Comparison of the quantum efficiency of a p-Si solar cell without a BSL and a back surface recombination velocity of $10^5$ cm/s and 3000 cm/s and with a 1 μm thick BSL and a back surface recombination velocity of $10^5$ cm/s.](image-url)
Device structure analysis

The quantum efficiency curves of the solar cell with a BSL closely approaches the quantum efficiency curve of the solar cell without a BSL but with $S_e = S_{e, \text{eff}}$. When the BSL is thicker, the quantum efficiency curves deviates more at higher wavelengths, as is demonstrated in Figure 5.21 for a BSL with a thickness of 10 μm. From Figure 5.18 an $S_{e, \text{eff}}$ of 730 cm/s for a BSL with a thickness of 10 μm at an acceptor concentration of $1 \times 10^{19}$ B/cm$^3$ is found.

![Figure 5.21: Comparison of the quantum efficiency of a f-Si solar cell without BSL and a back surface recombination velocity of $10^5$ cm/s and 730 cm/s and with a 10 μm thick BSL and a back surface recombination velocity of $10^5$ cm/s.](image)

To explain the difference between the internal quantum efficiencies we first summarise briefly the definition of internal quantum efficiency [10]. The internal quantum efficiency as used in previous section is defined as the external quantum efficiency of the solar cell corrected for the reflection at the front surface:

$$QE_{\text{int}}(\lambda) = \frac{QE_{\text{ext}}(\lambda)}{1 - R(\lambda)} \quad (5.15)$$

The external quantum efficiency, $QE_{\text{ext}}(\lambda)$, is the parameter that is measured directly. The external quantum efficiency is defined as the actual number of carriers collected (from all layers) per incident photon at each wavelength. The external quantum efficiency is dependent on the optical quantum efficiency, $QE_{\text{opt}}(\lambda)$, the electrical quantum efficiency, $QE_{\text{el}}(\lambda)$, and the generation quantum efficiency $\eta_g$ according to:
\[ QE_{ex} (\lambda) = \sum_{\text{layers}} QE_{\text{opt}} (\lambda) \eta_s QE_{el} (\lambda) \] (5.16)

The optical quantum efficiency is defined as the probability of a photon being absorbed in a specific layer of the solar cell per incident photon. The optical quantum efficiency is determined by integrating the generation rate profile in the specific layer. The generation quantum efficiency is the number of electron hole pairs generated by one absorbed photon. This is normally assumed to be unity. A generation quantum efficiency of one means that the generation rate profile is equal to the absorption profile. The electrical quantum efficiency is defined as the probability of a photo-generated carrier in a specific layer being collected.

In Figure 5.17 we have presented the two solar cells that are compared. The first situation is the solar cell with a BSL and a high back surface recombination velocity. The second situation is the solar cell without a BSL but with an equivalent low back surface recombination velocity. First we will consider the electrical quantum efficiency for both situations followed by the optical quantum efficiency. The electronic parameters \( \mu, \tau \) and \( N_{\text{dopant}} \) of the emitter and base layer in both situations are set equal. In the situation without a BSL an effective surface recombination is taken which is equivalent to the presence of the BSL in the other situation. The value of \( S_{\text{eff}} \) is based on calculation using the electronic parameters \( \mu, \tau, N_{\text{dopant}} \) and \( S_e \) of the situation with a BSL. Therefore the electrical quantum efficiencies of the emitter and of the base layer in both situations are assumed to be equal. The electrical quantum efficiency of the BSL is assumed to be zero, since the minority carrier lifetime in this material is very low. Photo generated free carriers recombine almost immediately after generation.

The total optical quantum efficiency for the first situation is described as:

\[ QE_{\text{opt}}^1 (\lambda) = QE_{\text{emitter} \ 1} (\lambda) + QE_{\text{base} \ 1} (\lambda) + QE_{\text{BSL}} (\lambda) \] (5.17)

For the second situation the total optical quantum efficiency is:

\[ QE_{\text{opt}}^2 (\lambda) = QE_{\text{opt}}^2 (\lambda) + QE_{\text{BSL}}^2 (\lambda) \] (5.18)
Device structure analysis

Assume that the reflection at the back surface is the same for both situations. Because the solar with a BSL is thicker, \( QE_{\text{opt}}^1(\lambda) \) will be higher than \( QE_{\text{opt}}^2(\lambda) \). The electrical quantum efficiency of the BSL layer is assumed to be zero. Therefor, we can leave out \( QE_{\text{opt}}^{\text{BSL}}(\lambda) \) and compare only the optical quantum efficiencies of the emitter and of the base layer in both situations. In situation 2 reflection of light occurs directly at the back surface of the base layer. In situation 1 photon will not be reflected at the interface between BSL and base layer, but travel through the BSL to reach the back surface solar cell. Photons that travel trough the BSL can be absorbed and can be (partly) reflected at the back surface back into the BSL or even into the base layer. As a result fewer reflected photons would be absorbed in the base layer, when comparing with situation 2. In case fewer reflected photons are absorbed in the base layer, the optical absorption profile and thus the generation rate profile will be lower. This will result that the optical quantum efficiency of the base layer of situation 1 is lower compared to situation 2: \( QE_{\text{opt}}^{\text{base}}^1(\lambda) < QE_{\text{opt}}^{\text{base}}^2(\lambda) \). The difference between the optical quantum efficiencies of the emitters in both situations is assumed to be negligible. When equation 5.15 is applied to both situations described above, the absolute internal quantum efficiency in the situation with a BSF layer will be lower when compared to the situation with an equivalent low back surface recombination velocity. The difference between the internal quantum efficiency of both solar cells is only visible at higher wavelengths (~700 nm and beyond). At these wavelengths the reflection of photons from the back surface become to play an important role.

### 5.3.6 Optical confinement

As indicated in Chapter 1, light-trapping methods are needed to achieve high efficiencies with f-Si solar cells. When the thickness of a silicon solar cell is decreased, less light is absorbed. The total number of photogenerated carriers will be lower, resulting in a lower current and lower efficiency of the solar cell. To maintain a high absorption of light while the thickness of the solar cell is reduced, light-trapping techniques are necessary. Light trapping is dependent on the internal reflection at the front and back surface. The internal reflection at the back surface depends on the materials on both sides of the interface of substrate and silicon and on the texture of the interface. In the following
calculations, the effect of internal reflection at the back surface is demonstrated only, thus now fill light trapping occurs. For this purpose internal quantum efficiencies were calculated with PC1D for different values of the internal reflection at the back surface. The results of f-Si solar cells with and without BSL are presented in Figure 5.22 and Figure 5.23 respectively. The BSL was 2 µm thick and the reflectance at the inner side at the back surface of the solar cell was varied.

![Graph with data points representing internal quantum efficiency vs. wavelength for different reflection rates.](image)

**Figure 5.22:** Calculated internal quantum efficiencies of a film-silicon solar cell without a BSL at varied internal reflections at the back surface ($R_{\text{rew}}$); the thickness of base layer and $L_e$ were both 10 µm. $S_e = 10^5$ cm/s.

![Graph with data points representing internal quantum efficiency vs. wavelength for different reflection rates.](image)

**Figure 5.23:** Calculated internal quantum efficiencies of a film-silicon solar cell with a BSL at varied internal reflections at the back surface ($R_{\text{rew}}$); the thickness of base layer and $L_e$ were 10 µm. $S_e = 10^5$ cm/s, the thickness of the BSL is 2 µm.
Device structure analysis

Considering the absorption spectrum of monocrystalline silicon [11], the optical path length of light with a wavelength higher than 700 nm must be larger than the thickness of the solar cell, which is 10 μm. This means that light with a wavelength of 700 nm and higher will reach the back surface of a solar cell with a thickness of 10 μm and will be lost in case no reflection occurs. To increase the absorption of light with a wavelength higher than 700 nm while using a cell thickness of 10 μm, the optical path length must be increased. Increasing the reflection at the back surface is one way to increase the optical path length. When the back surface of the solar cell reflects this light back into the base layer, it will contribute to the photocurrent of the solar cell. This increase in photocurrent expresses itself by an increase of the internal quantum efficiency in the range of 700 – 1200 nm. In order to reach a more efficient photovoltaic conversion, an increase of the internal reflection at the front side and texturing of the surfaces of both the front and backside of the f-Si solar cell is necessary.

5.4 Conclusions

Calculations with the device simulator PC1D give us useful information for the design of a f-Si solar cell structure. The simulated device structure is a two-sided contacted solar cell. Several issues of the device have been analysed.

The photovoltaic conversion efficiency appears to be moderately dependent on the acceptor concentration in the base layer. An acceptor concentration of approximately $2 \times 10^{17}$ B/cm$^3$ is a good choice for most cases. When the minority carrier lifetime becomes short enough the efficiency depends even less on the acceptor concentration.

The optimal thickness appears to be dependent on the minority carrier lifetime of the f-Si material and the back surface recombination velocity. When the minority carrier diffusion length of the deposited f-Si material and the actual back surface recombination velocity are known, the thickness can be adjusted to an optimal thickness, at which the maximum efficiency is obtained. The adjustment of the thickness towards an optimal value can be seen as an advantage of film-silicon solar cell technology. At high back surface recombination velocities the thickness of the base layer needs to be larger than the minority carrier diffusion length (approximately a factor of 3). When this recombination
velocity is very low, $S_e < 10^3$ cm/s, the thickness of the base layer is less than the minority carrier diffusion length. This information is of importance when cost per efficiency per volume of silicon used is an important consideration.

For a transparent emitter, relatively shallow emitters are necessary. The peak donor concentration may not be too high, since the reduction of minority carriers and the increase of the junction depth will make the emitter less transparent. Similar relations are found for mono- and multicrystalline silicon solar cells [12]. Surface passivation techniques are necessary to decrease the surface recombination velocity, preferably to values below $10^3$ cm/s. It is not yet exactly known whether enhanced diffusion along the grain boundaries can increase the efficiency, due to an enhanced collection capability. On the contrary, this enhanced diffusion can result in a short circuit in the solar cell.

Engineering towards a lower back surface recombination velocity is very difficult. The introduction of a BSF layer in a f-Si solar cell is a way to increase the efficiency as this makes the efficiency less dependent on the back surface recombination velocity. A back surface field layer will be useful in almost every case, but the effectiveness of the BSF layer must be analysed. The optimal acceptor concentration of the BSL depends on the thickness of the BSL. When the back surface recombination is low enough, no BSL should be applied.

Light trapping is necessary to obtain efficient silicon solar cells, since thin layers of silicon are not able to absorb the incident light efficiently. Light trapping is dependent on the internal reflections of light in the device and on the texture of both front and back surface of the solar cell. Internal reflections can be observed by measuring the quantum efficiency of the f-Si solar cell, since it will give an increase in the quantum efficiency at wavelengths in the range of 700 – 1200 nm.

5.5 References


Chapter 6

Film-silicon solar cells

6.1 Introduction
6.2 Base structure
6.3 Solar cells
6.4 Discussion
6.5 Conclusions
6.6 References

THIS CHAPTER reports on the first results of film-silicon solar cells that were fabricated using the f-Si layers on ceramic substrates described in Chapter 3.
6.1 Introduction

As described in Chapter 1, the work presented in this thesis is part of research to develop film-silicon solar cells. The starting point for making a solar cell is a base structure, which consists of one or more film-silicon layers deposited on a ceramic substrate. The selection of substrates and the deposition process of f-Si on the ceramic substrates is described in the previous chapters. In this chapter we describe a first approach to make solar cells from the base structures that are produced using the ceramic substrates and deposition methods we described in previous chapters. This approach to make solar cells is only to check if the produced base structures are suitable for making solar cells.

6.2 Base structure

The ceramic substrate that is a part of the base structure can be conductive or insulating. The conductivity of the substrate determines the design of the structure of the f-Si solar cells. In our work we used SiAlON and mullite substrates, which are insulating, and Si/SiAlON substrates, which are conductive. Use of an insulating substrate like SiAlON and mullite leads to a one-sided contacted solar cell structure. A conductive substrate, like Si/SiAlON, allows us to fabricate a two-sided contacted solar cell. For two-sided contacted solar cells a standard crystalline solar cell technology can be applied. Examples of both types of solar cell structures are given in Figure 6.1.

![Diagram of solar cell structures](image)

*Figure 6.1:* Schematic drawings of two device structures for film-silicon solar cells: (a) the two-sided contacted solar cell, (b) the one-sided contacted solar cell.
All solar cells were fabricated from a three-layer base structure: a highly doped p-type f-Si layer (p⁺-layer) deposited on the substrate, followed by the deposition of a moderately doped p-type f-Si layer (p-layer). The base structure Figure 6.2 presents a schematic drawing of the base structure as used within this research.

![Diagram of the base structure](image)

**Figure 6.2:** Schematic drawing of the base structure as used for both types of solar cell devices.

The highly doped p⁺-layer acts as a back surface field and will be referred to as the BSF layer. The moderately doped p-type f-Si layer will be referred to as the active base layer. In order to enhance the electronic quality of the active base layer, one can recrystallise the BSF layer using zone-melting recrystallization (ZMR) before the deposition of the moderately doped p-layer. The effect of ZMR of the BSF layer has been investigated for mullite and SiAlON substrates. The f-Si layers for the base structure were deposited at atmospheric pressure at 1100 °C by the thermal CVD process described in Chapter 2 and 3. The dopant concentration of the BSF layer was \( \sim 1 \times 10^{18} \) B/cm³. This dopant concentration was the maximum we could achieve with the available CVD reactor configuration. All dopant concentrations reported are measured on the films deposited on the monocrystalline reference (n-type) wafer, which was included in the actual deposition process.

Compact and dense films were deposited on the SiAlON and the mullite substrates without using a special surface treatment. The thickness of the deposited BSF layer was varied. The re-crystallization process demands a thickness of \( \sim 20 \mu m \). After the process the re-crystallized layer is always thinner, since some of the re-crystallized silicon is etched. For the samples without re-crystallization the thickness of the BSF layer was approximately 5 or 10 \( \mu m \). The average crystal grain size in the f-Si layers was 1 to 2 \( \mu m \). The area of the samples was \( 60 \times 60 \) mm² for both the SiAlON and mullite substrate.

The deposition of f-Si on the Si/SiAlON substrates was strongly influenced by the infiltrated Si particles, which formed large
Film-silicon solar cells

irregularities on the substrate surface. Further, severe whisker formation occurred during the deposition process. The Si/SiAlON substrates required a thorough surface treatment (polishing and cleaning) before compact and dense f-Si layers could be deposited. Compact layers as shown in Chapter 3 could be deposited on substrates with an area of 30 × 30 mm².

In Chapter 1 we discussed the influence of contamination of the f-Si layer by impurities from the substrate on the photovoltaic efficiency. The introduction of a barrier layer between the ceramic substrate and the deposited f-Si layer was proposed as a solution to reduce the contamination of the deposited f-Si layer. Within this work, a barrier layer was introduced in one solar cell on the SiAlON substrate. This barrier layer is a double layer consisting of subsequently 2 μm of TiN and 2 μm SiC. Both layers were deposited with a low-pressure CVD method (Everest Coatings, Delft). The thickness of the BSF and base layer was kept constant and no re-crystallization was carried out.

Most solar cells were made from the as-deposited f-Si material, which has a fine polycrystalline structure. To enhance the electronic quality of this as-deposited material, zone-melting re-crystallization (ZMR) is often used. The ZMR method [1] was used for re-crystallization of the BSF layer of some of the samples. Figure 6.3 shows a schematic drawing of the ZMR system.

![Figure 6.3](image)

**Figure 6.3**: Schematic drawing of the zone-melting re-crystallization (ZMR).

ZMR is carried out using a lamp-heated system. In this system a focussed beam with the shape of a line scans over the substrate. To minimize the thermal stresses, additional lamps are used which heat the substrate from the rear. In the focussing mirror a CCD camera is fitted
to monitor the re-crystallization process. The samples are placed on a quartz plate in a quartz tube (not shown in the figure). The thickness of the deposited f-Si layer was 20 µm, which is necessary for a proper recrystallization.

Before re-crystallization an LPCVD silicon-oxide capping layer was deposited on top of the BSF f-Si layer (Everest Coatings, Delft). After re-crystallization the capping layer was removed (etching with HF solution) and the samples were given a short etch (HF:HNO₃:HAc 1:7:2) to remove the highly defected surface of the silicon layer. During the re-crystallization process, interference with substrate material took place, resulting in holes and other defects in the film. Figure 6.4 shows SEM photographs of such defects, which were formed during the ZMR process of the BSF f-Si layer deposited on mullite and SiAlON substrates, respectively.

![Figure 6.4: SEM photographs of defects induced by ZMR in f-Si (BSF layer) on (a) mullite substrate and (b) SiAlON substrate.](image)

After the ZMR process the active base layer was epitaxially grown at 1100 °C with the thermal CVD process on the re-crystallized BSF layer. The dopant concentration of the active base layer was ~ 1 × 10¹⁷ B/cm³. Figure 6.5 shows the top surface of the final base structure: a re-crystallized BSF f-Si layer deposited on a SiAlON substrate and an epitaxially grown f-Si layer. Similar base structures were obtained using mullite substrates.
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Figure 6.5: Surface of a base structure with re-crystallized f-Si on a SiAlON substrate. Both the BSF and active base layers are deposited. The size of the sample is $60 \times 60$ mm$^2$.

The width of the crystals in the re-crystallized f-Si layers reached values of several millimetres, while the length of the crystals ranged from several millimetres to almost the length of the substrate. At the edges of the sample, fine polycrystalline silicon is still present. Figure 6.6 presents SEM photographs of the surface of the final base structures with ZMR layers.

Figure 6.6: SEM photographs of the surface of base structures with ZMR f-Si on (a) mullite and (b) SiAlON substrate. Both the BSF and active base layers are present.

Some of the structural defects induced by the ZMR process resulted in large holes in the f-Si layers of the base structure. We expect that these holes lead to shunts in the final solar cell device, causing a reduction in solar cell performance.
6.3 Solar cells

6.3.1 One-side contacted solar cells

Two different processes were used to produce one-sided contacted solar cells using the base structures described in the previous paragraph. Both processes were carried out in the laboratories of IMEC in Leuven, which have dedicated solar cell processes available. These processes are developed for experimental usage and not for industrial application. They are developed to study the solar cells in detail, so as to determine the factors that limit device performance and this knowledge can be used to improve the solar cells. The techniques that are used in the procedures such as photolithography and vacuum evaporation provide a high degree of control, accuracy and reproducibility.

The first process to produce the solar cells is the side-contacted mesa process (SCMP). This process is used for base structures with a smooth surface and is the simplest of the two processes used for the fabrication of solar cells in this work. A schematic drawing of the final device structure is presented in Figure 6.7. The p-layer is the base layer and the $p^+$-layer is the BSF layer of the f-Si solar cell.

![Figure 6.7: Schematic drawing of the solar cell structure produced with the side-contacted mesa process (SCMP) at IMEC, Leuven, Belgium [2].](image)

The second process used is the side-contacted planar process (SCPP). This process was applied on samples of which the surface was too rough to apply the SCMP. The drawbacks are that this processing procedure involves more steps and the alignment method used during the photolithographic steps is more complex. Within this process no mesa etching takes place. An extra diffusion is necessary to create
highly doped p'-regions under the contacts with the base layer. Figure 6.8 presents a schematic drawing of the solar cell structure produced with the SCPP solar cell processes.

![Schematic drawing of the solar cell structure](image)

**Figure 6.8**: Schematic drawing of the solar cell structure produced with the side-contacted planar process (SCPP) at IMEC, Leuven, Belgium [2].

In both f-Si solar cell processes the surface passivation is carried out by deposition of a plasma nitride, which takes place after the hydrogenation step in the same microwave induced plasma system. The deposited nitride layer will also act as an antireflection coating. There are 12 devices per $5 \times 5$ cm$^2$ and the active area of a solar cell is 1 cm$^2$. For a more detailed description of the f-Si solar cell processes see reference [2]. Reference cells were fabricated from monocrystalline f-Si (5 µm deposited on highly doped p-type wafer) and from polycrystalline silicon deposited on a thermally oxidized silicon wafer.

### 6.3.2 Two-side contacted solar cells

The base structure with the Si/SiAlON substrate was used to produce two-sided contacted solar cells. The device structure is comparable with the schematic drawing in Figure 6.1a. The process used is derived from an existing industrial-like process for multicrystalline silicon solar cells and was carried out at ECN, Petten, the Netherlands.

The emitter was created with a diffusion process in which phosphorus paste was applied with a roller. After removal of the phosphorus glass with 25% HF, metal contacts were screen-printed on both the front and the rear side of the sample. Since the samples were bent, it was necessary to remove the edges of the samples in order to reduce cracking during the printing process. After cutting, the size of the Si/SiAlON samples was $20 \times 20$ mm$^2$. No hydrogenation steps and no anti-reflection coatings were applied.
6.3.3 Solar cell results

Table 6.1 presents an overview of the external parameters of the fabricated solar cells.

<table>
<thead>
<tr>
<th>Thickness of BSF</th>
<th>ZMR of BSL</th>
<th>Thickness of base</th>
<th>$J_{sc}$ [mA/cm$^2$]</th>
<th>$V_{oc}$ [mV]</th>
<th>FF [%]</th>
<th>Eff. [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mono Si</td>
<td>no</td>
<td>5</td>
<td>23.5</td>
<td>632</td>
<td>81</td>
<td>12.1</td>
</tr>
<tr>
<td>SiO$_2$</td>
<td>no</td>
<td>20</td>
<td>17.1</td>
<td>381</td>
<td>49</td>
<td>3.2</td>
</tr>
<tr>
<td>Mullite* A</td>
<td>no</td>
<td>20</td>
<td>12.8</td>
<td>291</td>
<td>32</td>
<td>1.2</td>
</tr>
<tr>
<td>B</td>
<td>yes</td>
<td>32</td>
<td>21.2</td>
<td>479</td>
<td>53</td>
<td>5.4</td>
</tr>
<tr>
<td>SiAlON* A1</td>
<td>no</td>
<td>20</td>
<td>13.5</td>
<td>248</td>
<td>33</td>
<td>1.1</td>
</tr>
<tr>
<td>A2</td>
<td>no</td>
<td>29</td>
<td>16.7</td>
<td>409</td>
<td>34</td>
<td>2.4</td>
</tr>
<tr>
<td>B</td>
<td>yes</td>
<td>32</td>
<td>23.3</td>
<td>491</td>
<td>36</td>
<td>3.8</td>
</tr>
<tr>
<td>C</td>
<td>no</td>
<td>20</td>
<td>17.1</td>
<td>368</td>
<td>53</td>
<td>3.4</td>
</tr>
<tr>
<td>Si/SiAlON</td>
<td>10</td>
<td>20</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>~1.0</td>
</tr>
</tbody>
</table>

*: A) as-cvd deposited BSF layer
    B) ZMR BSF layer
    C) with barrier layer LPCVD TiN/SiC 2 μm/2 μm

We also listed the one-sided contacted reference solar cells on monocristalline silicon and silicon dioxide substrates. The monocristalline sample was added to monitor the solar cell processing. The measured external parameters of the monocristalline solar cells indicated that he solar cell process was carried out reasonable within specifications. The solar cells on SiO$_2$ were added as a reference on an amorphous substrate. Two types of solar cells were fabricated on a mullite substrate. The main difference between the mullite samples is the application of the ZMR process of the BSL for the mullite B sample. The solar cells with the recrystallized BSL show the highest efficiency of all samples. On SiAlON four types of solar cells were fabricated. The BSL layer of the SiAlON B sample is recrystallized and can be compared with the mullite B sample. Except for the fill factor all external parameters of the mullite B sample are higher than of the SiAlON B sample. The SiAlON A1 sample can be compared with the
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mullite A sample since it has the same thicknesses for both the BSL and base layer. The difference between the SiAlON A1 and A2 samples are the thicknesses of both the BSL and base layer. The SiAlON C sample is the only one with a barrier layer. The barrier layer consisted of a 2 μm thick TiN layer covered with a 2 μm thick SiC layer. The solar cells fabricated on this barrier layer can be compared with the SiAlON A1. The measured external parameters of the SiAlON C solar cells are higher than of the SiAlON A1 solar cells. The solar cells on the Si/SiAlON hardly reached a photovoltaic conversion efficiency of 1%.

Some of the solar cells were characterized by spectral response measurements. In Figure 6.9 the internal quantum efficiency (IQE) curves of some of the f-Si solar cells on ceramic substrates are presented. Also a fit of the experimental data with the computer programme PC1D is included.

![Figure 6.9](image.png)

**Figure 6.9:** The measured and fitted internal quantum efficiency (IQE) curves of some of the f-Si solar cells on ceramic substrates (measured at IMEC, Leuven).

The IQE curves all exhibit a shoulder at 800 nm and beyond.

We have tried to fit the experimental internal quantum efficiency curves with PC1D. The fitting of the data is not performed to get an exact fit of the measured data but to find some qualitative relations between material and device parameters. It appeared that it was necessary to divide the film-silicon layer (base layer and back surface field layer) into multiple regions, which indicates that the silicon layers do not have constant properties as a function of depth. A fit with only regions appeared to be inadequate. In this case a model with five regions as is illustrated in Figure 6.10 is used to fit the experimental data.
Figure 6.10: Schematic drawing of the device structure with five regions as is used for the fitting of the measured data. The grey scale relates to the dopant concentrations.

For each region the minority carrier lifetime, carrier mobility and the thickness of the regions were varied. In Table 6.2 the internal and external parameters of the fitted solar cell and some of the experimental external data are presented.

Table 6.2: Values of the input parameters of PC1D to fit that were used to fit the measured internal quantum efficiency curves.

<table>
<thead>
<tr>
<th>Region</th>
<th>SiAlON A2</th>
<th>SiAlON B</th>
<th>Mullite B</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minority carrier lifetime (us)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0.5</td>
<td>5</td>
<td>0.1</td>
</tr>
<tr>
<td>2</td>
<td>5.0E-03</td>
<td>0.2</td>
<td>0.07</td>
</tr>
<tr>
<td>3</td>
<td>1.0E-03</td>
<td>0.2</td>
<td>0.02</td>
</tr>
<tr>
<td>4</td>
<td>1.0E-03</td>
<td>0.2</td>
<td>0.02</td>
</tr>
<tr>
<td>5</td>
<td>1.0E-03</td>
<td>0.1</td>
<td>0.02</td>
</tr>
<tr>
<td>Carrier mobility (cm²/Vs)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>80</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>2</td>
<td>50</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>3</td>
<td>20</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>4</td>
<td>10</td>
<td>70</td>
<td>100</td>
</tr>
<tr>
<td>5</td>
<td>10</td>
<td>70</td>
<td>100</td>
</tr>
<tr>
<td>Thickness (μm)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>5</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>2</td>
<td>10</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>3</td>
<td>10</td>
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<td>7</td>
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</tr>
<tr>
<td>5</td>
<td>10</td>
<td>10</td>
<td>10</td>
</tr>
</tbody>
</table>

The thickness of region 5 of both ZMR samples was set to 10 μm instead of the deposited 20 μm. During the ZMR process some of the recrystallised BSF material is etched. The loss is assumed to be approximately 10 μm.
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Only by using more than one region, the experimental curves could be reasonably approached. In all cases the minority carrier lifetime is shorter nearby the substrate and is longer in regions closer to the top surface. The minority carrier lifetime varies 1 order of magnitude for the ZMR material (SiAlON B and mulite B) and almost 3 order of magnitude for the fine polycrystalline material (SiAlON A2). The average minority carrier lifetime of the recrystallised f-Si material is always larger compared to the as-deposited f-Si material. The carrier mobility of the as-deposited f-Si material varied much more across the five regions, when compared to the recrystallised f-Si material.

6.4 Discussion

The purpose of this discussion is not a detailed evaluation of the solar cell parameters but to make general remarks on the suitability of the substrates with f-Si layers in a solar cell process. For this purpose we will reconsider the basic steps of the fabrication of the base structure and of the solar cell processing. The production of the ceramic substrate is not included in this consideration. No statistic analysis was performed since the number of solar cells was limited. Not all produced cells worked, since cracking or short circuits occurred very often. A discussion about the external parameters will therefore be mainly qualitative.

In the production of the BSL, which is the first layer on the ceramic, several parameters are important. For the deposition process, the dopant concentration must be relatively high. From the results of the simulations in Chapter 5 it was concluded the dopant concentration must be in the range of $1 \times 10^{19}$ and $1 \times 10^{20} \text{ B/cm}^3$. The maximum concentration obtained with the current reactor set-up was around $1 \times 10^{18} \text{ B/cm}^3$, which was measured on the f-Si layer deposited on the monocrystalline silicon reference wafer. This reduction in dopant concentration will result in a lower built-in electric field, and as a result the influence of the rear surface recombination is still large. In addition, the lower concentration will result in a higher resistivity of the BSL. In a one-side contacted solar cell, this layer is responsible for the transport of collected electrons from the active area of the solar cell to the side contacts. An increase in the resistivity of the BSL will result in an increased loss of efficiency by this series resistance. The thickness of the BSL plays also an important role. The optimal thickness is dependent on the minority carrier lifetime and the back surface
recombination velocity. In addition, a thicker layer will lower the resistance of the BSF layer and will therefore lower losses by series resistance in a one-side contacted solar cell. However, in a two-side contacted solar cell, a thicker layer will increase the series resistance.

The thickness of the BSL should be related to the minority carrier diffusion length in the layer and the rear surface recombination (see paragraph 5.3.4). Since the minority carrier diffusion length in the BSL and the back surface recombination are not exactly known it is difficult to determine whether the thickness of the BSL is optimal. Concerning the results of Chapter 5 we expect that the thickness of the BSL is not optimal.

The electronic quality of the silicon was previously related to the lifetime of the generated free carriers in the bulk of the base layer. In Chapter 5 it was reported that the efficiency of a film silicon solar cell increases with increasing the minority carrier lifetime or diffusion length. Concerning the polycrystalline structure of the deposited material; the lifetime or diffusion length depends on several properties of the polycrystalline material, like the crystal grain size, the defect density and the presence of impurities of the substrate. Increasing the crystal grain size by using e.g. ZMR can increase the effective lifetime of carriers in the base layer, since the area of grain boundary per volume is reduced. In this way the amount of recombination and trapping possibilities for the generated free carriers is reduced. The enlargement of the crystal size will therefore result in higher efficiencies, which is also described by Bergmann [3]. An increase of the efficiency when ZMR is used has been observed with the solar cells on both SiAlON and mullite substrates as described in this chapter.

The ZMR process appeared to generate extra defects in the deposited film. The defects, which are present throughout the whole thickness of the BSF layer, can be continued in the subsequently deposited base layer (see e.g. Figure 6.6b). These kinds of defects can result in increased shunting possibility of the final solar cell device. The created shunting defects are a result of interaction between the substrate material and the film during the ZMR process. After processing part of the solar cells as described in this chapter appeared to be completely shunted. Optimisation of the ZMR process and substrates is therefore necessary.
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The minority carrier diffusion length in the f-Si layer is dependent on the concentration of impurities that diffuse from the substrate during the deposition or solar cell processing. The introduced impurities in the layer can react as recombination or trapping centres. Application of a barrier layer on the substrate before depositing the silicon can reduce contamination of the silicon by diffusion of elements from the substrate, which can increase the electronic quality of the film. The difference of the efficiencies of the solar cells on the SiAlON substrate, A1 and C, confirm this.

The thickness of the base layer in the f-Si solar cell is one of the main parameters in this research. The results in Chapter 5 show that the optimal value for the thickness strongly depends on the minority carrier lifetime of the generated free carriers in the base layer. In most cases an increased thickness results in an increased efficiency. This effect can be observed from the results in Table 6.1 (compare solar cells on mullite, A and B, and solar cells on SiAlON, A1 and B).

The quality of both the BSF layer and the base layer depends strongly on the fabrication of the base structure, which includes the fabrication of the substrates, the deposition processes and a possible ZMR process. During the one-side contacted solar cell processes, in which the base structures are used, the electronic quality is improved by means of hydrogenation in a hydrogen plasma. During the hydrogenation step the grain boundaries are passivated with hydrogen, resulting in a decrease of the number of recombination centres at the grain boundaries and in the bulk of the crystals. The parameters of this process step are of course dependent on the properties of the film to be hydrogenated, e.g. thickness of the film, crystal size, defect density, etc. Therefore it is expected that this process can be optimised further.

In the case of two-side contacted solar cells, cracking of the devices occurs during the solar cell processing. This cracking is mainly observed for the Si/SiAlON substrate base structures. These base structures bend due to the low thermal relaxation of the substrate (as described in Section 3.6) and due the difference in thermal expansion coefficients. This bending in combination with a low mechanical strength of the Si/SiAlON material easily causes cracking of the base structures during the solar cell process. This cracking can be reduced by optimisation of the substrate properties or by optimisation of the solar cell processing.
The IQE curves of the f-Si solar cells show a tail at the range of 800 nm and beyond. The onset of the shoulder can be calculated roughly \((1/\alpha(\lambda)) = \text{total thickness of the solar cell}\). In all cases the calculated wavelength is approximate to the onset of the shoulder in the IQE curves. The raise in efficiency can be explained by reflection of light at the rear surface of the cell. When we evaluated this effect with PC1D, we observed a similar raise in the same range as described in Section 5.3.6. Except for the monocrystalline reference cell, this increase in efficiency is observed in every f-Si solar cell on a substrate, indicating that reflection occurs at the interface of f-Si and the ceramic material.

The results on fitting the measured internal quantum efficiency with PC1D show that for several electronic properties are not uniform across the thickness of the f-Si layer. The electronic quality of the material is worse in the region closest to the substrate. The lower electronic quality could be due to a higher impurity concentration or due to a smaller crystal size in regions close to the substrate. The lower electronic quality due to a smaller crystal grain size could be expected considering the results as presented in Chapter 4. The crystal size varies across the thickness of the f-Si layer. The largest crystal diameters are at the top surface of the deposited layer. Larger crystals mean fewer grain boundaries, which is beneficial to obtain long minority carrier diffusion lengths. Also differences between the ZMR and the as-deposited f-Si layer material are observed. The as-deposited fine polycrystalline material shows the largest differences in the values for the minority carrier lifetime and the carrier mobility. The ZMR f-Si material shows better electronic properties than the as-deposited fine polycrystalline material.

Despite the lack of optimised processes for deposition and solar cell processing, the efficiency of the solar cells we made using mullite substrates was still 5.4%. Also the f-Si solar cell on SiAlON showed an efficiency of 3.8%. On both substrates, ZMR was used for the solar cells with the highest photovoltaic conversion efficiency. In most cases no barrier layers are present between the f-Si layers and substrates. Diffusion of elements from the substrate into the deposited f-Si layer cannot be excluded. In one case, a barrier layer was included in a base structure using a SiAlON substrate. The efficiency was higher (3.5%) than that of the cell without a barrier layer (1.1%). The difference can be explained by the effect of the barrier layer.
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It must be noted that the obtained efficiencies are not maximal; S. Bourdais et al. [4] already obtained 8.2 % efficiency with a similar type of solar cell on mullite. To reach these efficiency, more pure substrates and more optimised ZMR and solar cell processes could be used.

6.5 Conclusions

Although not fully optimised procedures were used, film-silicon solar cells on the insulating mullite and SiAlON substrates were realized. Zone-melting recrystallization of BSF f-Si layers resulted in solar cells with higher efficiencies than those of solar cells made from as-deposited f-Si layer material. The substrate material interacts with the recrystallization process, which results in structural defects in the f-Si layer. Efficiencies of 5.4 % have been achieved with 50 μm thick f-Si layers on the bare mullite substrate.

The results on fitting the internal quantum efficiency of the experimental data show that a gradient for several electronic parameters across the thickness of the f-Si layer must be present.

Beside ZMR of the BSF layer, introduction of a barrier layer in the solar cell on the SiAlON substrate appeared to be beneficial to the efficiency. The increased efficiency can be explained by a reduction of the diffusion of impurities from the substrate into the deposited silicon.

These results demonstrate that thermal CVD f-Si on mullite and SiAlON substrates can be an option for thin polycrystalline silicon-based solar cells on ceramic substrates. However, to obtain the highest efficiencies, ZMR and a barrier layer are necessary.

The conductive Si/SiAlON substrate offers us the possibility to use conventional crystalline solar cell processing methods. However, due to the mechanical strength of the material, dissimilar thermal expansion coefficients and the low thermal relaxation of the substrate material, cracking occurs frequently during the solar cell process. Optimisation of the solar cell process and/or improvement of the substrate are therefore necessary to make this type of substrate an option for future film-silicon solar cells.

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6.6 References


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Chapter 7

Conclusions

This chapter presents the final conclusions of this thesis.
Conclusions

• We investigated the deposition parameters of a high-temperature CVD process for growth of thin layers of silicon on newly developed ceramic substrates. Silicon wafers and oxidized silicon wafers were used as reference substrates. The suitability of different ceramic substrates to serve as a substrate was tested in a high-temperature CVD process. Using dichlorosilane as a source gas for silicon, a maximum deposition rate up to 0.8 μm/min was obtained on single crystalline silicon substrates at 1100 °C. A deposition rate of 0.6 μm/min at a deposition temperature of 1100 °C was obtained on the most suitable ceramic substrates.

• Suitable substrates for the high-temperature CVD process were selected on the criterion whether a compact thin silicon layer with a thickness up to 10 μm could be obtained using these substrates. Important parameters of the ceramic substrate that determine the deposition of silicon are the surface roughness, the porosity, the thermal expansion coefficient, the thermal stability and the whisker formation during deposition. Mullite and SiAlON are the most suitable substrate materials among all materials tested. Mullite shows an acceptable difference in thermal expansion coefficient with silicon while whisker formation during the deposition process hardly occurs. SiAlON shows the smallest difference in thermal expansion coefficient with silicon, but whisker formation during the deposition process did occur.

• Whisker formation depends on the substrate material and the deposition temperature. Whisker formation occurs mainly on the SiAlON based substrates. On the Si/SiAlON substrates the whisker formation is observed most extensively. Cleaning of the substrates reduces whisker formation. The developed cleaning procedures consisted mainly of ex-situ cleaning in HNO₃ 65 % or RCA2 solution, which are used to remove metallic impurities, or in-situ cleaning with HCl at 1100 °C.

Whisker formation is studied in more detail for Si/SiAlON substrates cleaned with boiling HNO₃ 65 %. At deposition temperatures above 1000 °C, whisker formation becomes less and can be reduced to almost zero. Although not proven by chemical analysis, the results indicate that substrate material and/or impurities from the substrate must be involved.
in the whisker formation process. The whiskers are formed according to the classical vapour-liquid-solid (VLS) mechanism.

When the SiAlON based substrates were used, we observed that the formation of whiskers also depends on the size of the sample. Increasing the sample area also leads to an increase in the formation of whiskers, which mostly occurs in the middle of the sample area.

- Structural analysis revealed that the type of substrate strongly influences the stress in the deposited silicon films. In the silicon films deposited on a SiAlON substrate tensile stress is observed, while in the films deposited on mullite substrates compressive stress is present. In all deposited films the observed stress is higher than the thermal stress, which is determined by the differences in the thermal expansion coefficients of silicon and substrate materials. Besides the thermal stress, growth stress is also present, as can be confirmed by the XRD experiments. The cause of this growth stress is the presence of the grain boundaries; several types of defects, among which twinned pairs, are most observed. Silicon films deposited on SiAlON substrates exhibit lower values for stress than silicon films deposited on mullite substrates.

- The deposition temperature mainly determines the crystallographic structure of f-Si layer. The largest crystals are obtained at 1100 °C and these have a columnar structure. At 1100 °C the average crystal size is 1 – 2 μm. At temperatures below 1100 °C the crystals are much narrower and organized in V-shaped regions. The crystallographic structure depends more on the deposition temperature than on the substrate material.

- The simulations demonstrate that the optimal thickness of the base layer depends on the diffusion length of the minority carriers and the back surface recombination velocity. The optimal thickness of the base layer when a high back surface recombination is present is two to three times larger than the minority carrier diffusion length. In the case of a low back surface recombination velocity, the thickness is less than the minority carrier diffusion length.
Conclusions

- The simulation results show that lowering the back surface recombination velocity to values below 10000 cm/s results in an increase of efficiency and a lower optimal value for the base layer thickness. To suppress the influence of the back surface recombination velocity in f-Si solar cell, a back surface field layer (BSL) can be deposited before the deposition of the active base layer. In case of a p-type base layer, the acceptor concentration for an effective BSL must be fairly high ($10^{19}$ B/cm$^3$ – $10^{20}$ B/cm$^3$) and the optimal BSL thickness is limited by the minority carrier diffusion length and by the back surface recombination.

- Simulation shows that of an optimal emitter the calculated maximum front surface recombination is 1000 cm/s. For silicon solar cells, this means that surface passivation methods are necessary. However, reducing the front surface recombination velocity to values below 1000 cm/s will hardly compensate the loss in the blue region of the solar spectrum due to the high average junction depth.

- Solar cells with an epitaxially grown f-Si layer on a recrystallized f-Si seed layer on mullite and SiAlON substrates show higher efficiencies than solar cells with as-CVD deposited f-Si material. However, zone-melting recrystallization of the f-Si seed layer created defects, which resulted in shunts in the final solar cell. These defects occur due to interaction of the substrate material with the recrystallization of the f-Si layer during the ZMR process. Optimisation of the ZMR process and ceramic substrates is therefore necessary. Despite the defects, solar cells with photovoltaic conversion efficiencies of 5.4 % were fabricated on mullite substrates and with efficiencies of 3.8 % on SiAlON substrates.
Appendices

Appendix A:
SEM photographs of the surface of the substrates used.

Si/Al  ps-Si

Al₂O₃  mullite

SiAlON  Si/SiAlON
Appendices

**Appendix B:**

Selection of SEM photographs of depositions on the Si/SiAlON substrate at various deposition temperatures at standard deposition conditions without dopants. All substrates were cleaned with boiling HNO₃ 65 %. The deposition time was adjusted to obtain a layer of ~ 10 μm thick.

<table>
<thead>
<tr>
<th>Temperature</th>
<th>Image 1</th>
<th>Image 2</th>
<th>Image 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>1100 °C</td>
<td><img src="#" alt="Image" /></td>
<td><img src="#" alt="Image" /></td>
<td><img src="#" alt="Image" /></td>
</tr>
<tr>
<td>1050 °C</td>
<td><img src="#" alt="Image" /></td>
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<td><img src="#" alt="Image" /></td>
</tr>
<tr>
<td>1000 °C</td>
<td><img src="#" alt="Image" /></td>
<td><img src="#" alt="Image" /></td>
<td><img src="#" alt="Image" /></td>
</tr>
<tr>
<td>950 °C</td>
<td><img src="#" alt="Image" /></td>
<td><img src="#" alt="Image" /></td>
<td><img src="#" alt="Image" /></td>
</tr>
<tr>
<td>900 °C</td>
<td><img src="#" alt="Image" /></td>
<td><img src="#" alt="Image" /></td>
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</tr>
<tr>
<td>850 °C</td>
<td><img src="#" alt="Image" /></td>
<td><img src="#" alt="Image" /></td>
<td><img src="#" alt="Image" /></td>
</tr>
</tbody>
</table>
Appendix C:

Calculated normalized positions and intensities of diffraction lines for polycrystalline silicon with a randomly oriented texture.

<table>
<thead>
<tr>
<th>Diffraction line (h k l)</th>
<th>Peak position</th>
<th>Relative intensity [%]</th>
<th>Interplanar spacings $d$ [nm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 1 1</td>
<td>28.443</td>
<td>100</td>
<td>0.313553</td>
</tr>
<tr>
<td>2 2 0</td>
<td>47.303</td>
<td>68</td>
<td>0.192011</td>
</tr>
<tr>
<td>3 1 1</td>
<td>56.123</td>
<td>40</td>
<td>0.163748</td>
</tr>
<tr>
<td>4 0 0</td>
<td>69.131</td>
<td>11</td>
<td>0.135772</td>
</tr>
<tr>
<td>3 3 1</td>
<td>76.377</td>
<td>17</td>
<td>0.124593</td>
</tr>
<tr>
<td>4 2 2</td>
<td>88.031</td>
<td>24</td>
<td>0.110858</td>
</tr>
<tr>
<td>3 3 3</td>
<td>94.954</td>
<td>14</td>
<td>0.104518</td>
</tr>
<tr>
<td>4 4 0</td>
<td>106.71</td>
<td>9</td>
<td>0.096006</td>
</tr>
<tr>
<td>5 3 1</td>
<td>114.094</td>
<td>19</td>
<td>0.091799</td>
</tr>
<tr>
<td>6 2 0</td>
<td>127.546</td>
<td>21</td>
<td>0.085870</td>
</tr>
<tr>
<td>5 3 3</td>
<td>136.896</td>
<td>13</td>
<td>0.082820</td>
</tr>
</tbody>
</table>

![Diagram showing the peaks and their normalized intensities]
The fabrication of solar cells based on thin, polycrystalline silicon films grown on low-cost substrates is considered to be an attractive approach to realize cheap and highly efficient solar cells. For this reason we investigated and optimised a high-temperature chemical vapour deposition method for depositing polycrystalline silicon films on ceramic substrates. Ceramic substrate materials like Al₂O₃, mullite, SiAlON and Si/SiAlON were tested for their suitability as substrates for the deposition of polycrystalline silicon layers. Important criteria for the selection of the substrates are porosity, surface roughness, thermal expansion coefficients, thermal stability, stress and whisker formation that can occur during the deposition process. Mullite and SiAlON appeared to be the most suitable substrate materials within this study.

The structural properties of the silicon films deposited on the ceramic substrates were evaluated. The average grain size of the layer depends on the deposition temperature. At 1100 °C the average grain size is 1 – 2 µm, but is smaller at lower deposition temperatures. The observed density of defects, which are mainly represented by twinned stacks, in a layer of silicon deposited at 1100 °C was lower than that in samples deposited at lower temperatures. Stress was observed in every silicon layer deposited on a ceramic substrate. In all cases this stress resulted in bent samples, which is not desired because it hinders the subsequent solar cell processing. The samples with a SiAlON substrate show less stress than samples with a mullite substrate. Using thicker substrates can decrease bending of the samples.

Whisker formation occurred during the deposition process and was most frequently observed on the SiAlON-based substrates. This is undesirable since it results in silicon having an irregular and non-compact structure. The mechanism of the whisker growth is the classical vapour-liquid-solid mechanism. Cleaning methods to suppress the whisker formation were developed.

The basic device structure of thin silicon solar cells was analysed by means of computer modelling, involving an investigation of several
Summary

device and material parameters, like the minority carrier lifetime, the thickness of the base layer and the surface recombination velocities.

Film silicon solar cells on mullite, SiAlON and Si/SiAlON were fabricated. First a highly doped seed layer was deposited on the ceramic substrates. The effect of zone melt recrystallization of the seed layer on the performance of the solar cells was investigated using mullite and SiAlON substrates. The active base layer was epitaxially grown on the seed layer. The highest efficiency of 5.4% was obtained with a 40 µm thick f-Si solar cell with a recrystallized seed layer on a bare mullite substrate.
Dunne films van polykristallijn silicium op goedkope substraten worden beschouwd als basis voor toekomstige goedkope en hoog efficiënte zonnecellen. Voor de fabriek van deze cellen is het nodig dat dunne films van silicium op de substraten aangebracht worden. Binnen het hier gepresenteerde onderzoek werd chemische opdampmethode bij hoge temperatuur onderzocht en geoptimaliseerd voor depositie van polykristallijn silicium op een selectie van keramische substraten. Keramische materialen als Al₂O₃, mulliet, SiAlON en Si/SiAlON werden getest op hun geschiktheid voor substraten voor de depositie van de silicium films. Belangrijke selectiecriteria voor de substraten waren de porositeit, de oppervlakte ruwheid, de thermische expansie coefficient, de thermische stabiliteit en het voorkomen van whisker groei tijdens het depositie proces. Mulliet en SiAlON substraten bleken de meest geschikte substraten te zijn.

Een aantal morfologische en structurele eigenschappen van de op de keramische substraten gedeponeerde silicium lagen zijn onderzocht. De gemiddelde korrelgrootte in de siliciumlaag is afhankelijk van de depositie temperatuur. Bij 1100 °C is de gemiddelde korrelgrootte 1 – 2 μm en is kleiner bij lagere depositie temperaturen. De waargenomen defectdichtheid, welke voornamelijk door tweeling structuren bepaald werd, in een silicium film gedeponeerd bij 1100 °C is lager vergeleken met lagen die gedeponeerd zijn bij een lagere depositie temperatuur. Stress is gemeten bij elke op een keramisch substraat gedeponeerd silicium laag. Deze stress resulteert in gekromde structuren, wat een opvolgend zonneel proces bemoeilijkt. De monsters met een SiAlON substraat vertonen minder stress in vergelijking tot monsters met een mulliet substraat. Het gebruik van dikkere substraten vermindert het buigen van de monster door stress.

Whiskers zijn voornamelijk waargenomen op de SiAlON gebaseerde substraten. Deze whiskergroei resulteert in een onregelmatige en een niet compacte structuur van de film. Het mechanisme van de whisker groei is het klassieke damp-vloeistof-vaste stof mechanisme.
Samenvatting

Schoonmaakmethoden om deze whiskergroei te onderdrukken zijn ontwikkeld.

Een zonnecel analyse is uitgevoerd aan de hand computer simulaties. Verschillende cel and materiaal parameters zoals levensduur van de minderheidsladingsdrages, de dikte van de basislaag and de oppervlakte recombinaat snelheid, zijn geanalyseerd.

Film-sillicium zonnecellen zijn gemaakt op mullite, SiAlON en Si/SiAlON substraten. Voor alle cellen werd als eerste een kiemlaag op het keramische substraat gedeponeerd. Het effect van ‘zone melt’ rekristallisatie van deze kiemlaag op de fotovoltaïsche conversie van de zonnecel is onderzocht. De actieve basislaag werd epitaxiaal gegroeid op de kiemlaag. De hoogst efficientie van 5.4 % is behaald met een 40 μm dikke f-Si zonnecel met een gerekristalliseerd kiemlaag op een mulliet substraat.
Acknowledgement

Having arrived at the end of this thesis I need to thank a lot of people who supported me and contributed to this thesis. I sincerely wish to thank all members of the Delft Institute of Microelectronics and Submicronotechnology (DIMES) and of the laboratory of Electrical Components, Technology and Materials (ECTM). In particular I wish to thank:

- Miro Zeman, who guided me pleasantly through the last five years.
- Prof. Kees Beenakker for support of any kind and maintaining the good working atmosphere in DIMES.
- Wim Metselaar for providing the right research environment and giving me the opportunity to do this research.
- All other people of the solar group, Rene, Ben, Amir, Arjan, Bas, Martin, Agnes, Lawrence, Joost.
- Alex van den Bogaard and Alfred Apon for their technical support. Keeping the Gemini reactor operational was sometimes quite difficult, but you always succeeded.
- All other technicians at DIMES, who supported and encouraged me. You are great.
- My roommates, Paul (also my coffee-mate), Ryoichi and Sylvana.
- All other PhD students at ECTM/DIMES.

Working at DIMES was always very enjoyable; guys keep up the good work!!

- During my research there was a close contact with the Netherlands Energy Research Foundation (ECN) in Petten. I would like to thank my second thesis supervisor, Prof. Wim Sinke, Kees Tool, Armin von Keitz, Sacha Schiermeier, John van Roosmalen, Hugo de Moor, Astrid Gutjahr and many more people from the solar group of ECN for their pleasant cooperation and fruitful discussions which all contributed to this thesis.
- I would like to thank Albert Goossens, Edward Maloney, Gijsbert Korevaar, Frank Witte and all other participants of Dutch film-silicon project.
Acknowledgement

- I would like to thank Guy Beaucarne, Jef Poortmans, Stephane Bourdais, Abdou Slouoi, Walter Zimmerman and all other participants of the European project on film-silicon solar cell.
- Many people contributed to the analyses within this research. Frans Tichelaar, thanks for all the work. Your diffraction pattern is on the cover. Pavol Šutta, who carried out the X-ray diffraction analysis. Thanks for the good work, discussions and hospitality. Also thanks to Lianne Doeswijk and Albert van den Berg, who gave me the possibility for some urgent Auger analysis.
- Mirjam Nieman, for correcting the English of this thesis.
- My friends for their moral support and understanding.
- Mijn ouders en familie voor hun begrip en ondersteuning.
- And last but not least, Wendie for her eternal support and understanding.

Thanks, Adje


Ad van Zutphen was born in Veghel, the Netherlands, on 16 July 1969 and was raised in Heeswijk-Dinther, Noord-Brabant. He obtained the gymnasium degree at Gymnasium Bernrode in Heeswijk-Dinther. He started his studies molecular sciences at the Wageningen Agricultural University in 1989. Within this study, he followed two graduating projects and one trainee ship on organic solar cells. The topics of his graduating projects all concerned the Dutch approach of a solid-state organic solar cell. The subject of his trainee ship was the Dye Sensitized Solar Cell also known as the Grätzel type solar cell and was carried out at the Netherlands Energy Research Foundation (ECN) in Petten. In November 1995 he obtained his university degree. In December 1995, he left the field of organic solar cells and has been working as a PhD student on film-silicon solar cells at the Delft Institute of Microelectronics and Submicronotechnology of the Delft University of Technology. This research was part of both several Dutch and European projects on thin-film crystalline silicon solar cells. December 2000 he joined ASM Europe in Bilthoven, to work on the development of IC fabrication equipment and processing.